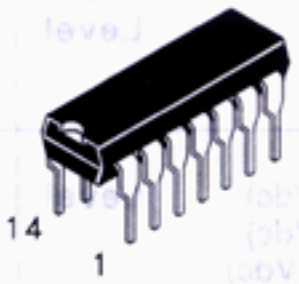
Dual D-Type Flip-Flop

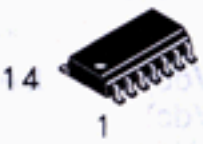
DV4013B

This device is a dual D-Type Flip-flop constructed with MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data, Set, Reset, and Clock inputs and complementary outputs.

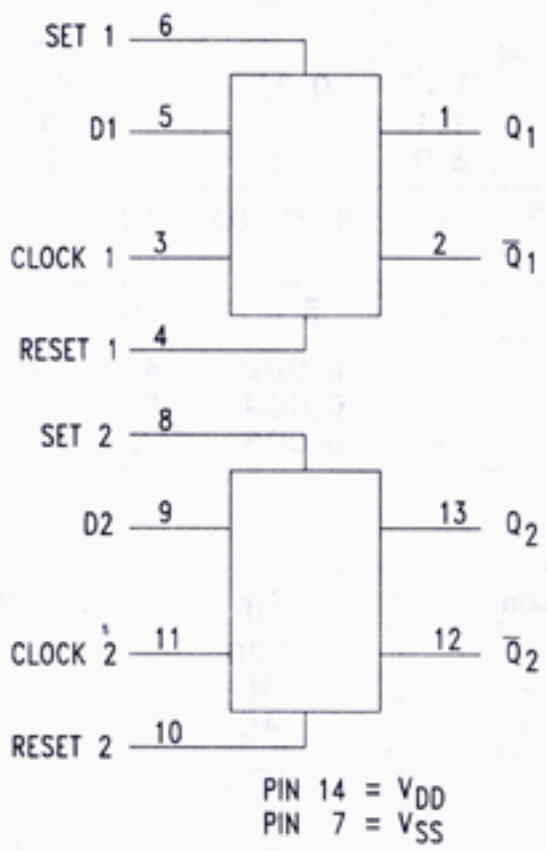
- **Supply voltage range = 3.0 Vdc to 18 Vdc**
- **All outputs buffered**
- **Capable of driving 4 Low Power TTL loads or one LS TTL load over the rated temperature range**
- **Diode protection on all inputs**
- **Highest noise immunity at 12V supply**



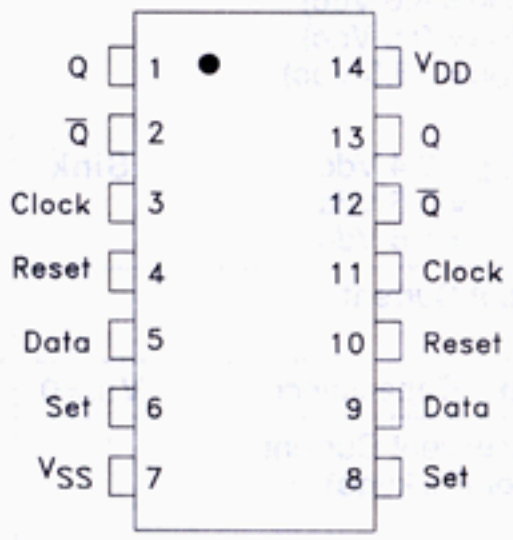
N Suffix
Plastic DIP
AVG-001 Case



D Suffix
Plastic SOP
AVG-002 Case



PIN ASSIGNMENT



TRUTH TABLE

Clock	D	Reset	Set	Q	$\overline{Q}$
↑	0	0	0	0	1
↑	1	0	0	1	0
↓	X	0	0	No Change	
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

↑ = Low to High Transition
↓ = High to Low Transition
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage (Referenced to V_{SS})	−0.5 to +18.0	V
V_{IN}, V_{OUT}	Input or Output Voltage	−0.5 to V_{DD}+0.5	V
I_{IN}, I_{OUT}	DC Current Into or Out of Any Pin	± 10	mA
P_D	Power Dissipation in Still Air, Derating: 12 mW/°C from 65° to 85°C	500	mW
T_{STG}	Storage Temperature Range	−65 to +150	°C
TL	Lead Temperature, (8 Second Soldering)	260	°C

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Parameter		V_{DD}	Guaranteed Limits							Unit
				-40°C		25°C			85°C		
				Min	Max	Min	Typ	Max	Min	Max	
V_{OL}	Output Voltage $V_{IN}=V_{DD}$ or 0	"0" Level	5.0 10 15	- - -	0.05 0.05 0.05	- - -	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	Vdc
V_{OH}	V_{IN}= 0 or V_{DD}	"1" Level	5.0 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.0 10 15	- - -	4.95 9.95 14.95	- - -	Vdc
V_{IL}	Input Voltage (V_O=4.5 or 0.5 Vdc) (V_O=9.0 or 1.0 Vdc) (V_O=13.5 or 1.5 Vdc)	"0" Level	5.0 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.50 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	Vdc
V_{IH}	(V_O=0.5 or 4.5 Vdc) (V_O=1.0 or 9.0 Vdc) (V_O=1.5 or 13.5 Vdc)	"1" Level	5.0 10 15	3.5 7.0 11	- - -	3.5 7.0 11	2.75 5.50 8.25	- - -	3.5 7.0 11	- - -	Vdc
I_{OH}	Output Drive Current (V_{OH} = 2.5 Vdc) (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	Source	5.0 5.0 10 15	−2.5 −0.52 −1.3 −3.6	- - - -	−2.1 −0.44 −1.1 −3.0	−4.2 −0.88 −2.25 −8.8	- - - -	−1.7 – 0.36 −0.9 −2.4	- - - -	mAdc
I_{OL}	(V_{OL} = 0.4 Vdc (V_{OL} = 0.5 Vdc (V_{OL} = 1.5 Vdc	Sink	5.0 10 15	0.52 1.3 3.6	- - -	0.44 1.1 3.0	0.88 2.25 8.8	- - -	0.36 0.9 2.4	- - -	mAdc
I_{IN}	Input Current		15	-	±0.3	-	±0.00001	±0.3	-	±1.0	µAdc
C_{IN}	Input Capacitance	V_{IN}=0	-	-	-	-	5.0	7.5	-	-	pF
I_{DD}	Quiescent Current (Per Package)		5.0 10 15	- - -	4 8 16	- - -	0.002 0.004 0.006	4 8 16	- - -	30 60 120	µAdc

SWITCHING CHARACTERISTICS (C_L=50 pF, T_A=25°C)

Symbol	Characteristics	V_{DD}	Min	Typ	Max	Unit
t_{TLH}, t_{THL}	Output Rise and Fall Time	5.0 10 15	- - -	100 50 40	200 100 80	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, Clock and Set to Q, $\overline{Q}$	5.0 10 15	- - -	175 75 50	350 150 100	ns
	Reset to Q, $\overline{Q}$	5.0 10 15	- - -	350 100 75	450 200 150	
t_{WL}, t_{WH}	Clock, Set and Reset Pulse Width	5.0 10 15	250 100 70	125 50 35	- - -	ns
f_{cl}	Clock Pulse Frequency	5.0 10 15	- - -	4.0 10 14	2.0 5.0 7.0	MHz
t_{TLH}, t_{THL}	Clock Pulse Rise and Fall Time	5.0 10 15	- - -	- - -	15 5 4	µs
t_{su}	Setup Time (Data must be valid for 250 ns with a 5V supply. 100 ns with 10V, and 70 ns with 15V)	5.0 10 15	40 20 15	20 10 7.5	- - -	ns

SWITCHING CHARACTERISTICS (Continued)

Symbol	Characteristics		V_{DD}	Min	Typ	Max	Unit
t_h	Hold Time (Data must be valid for 250 ns with a 5V supply. 100 ns with 10V, and 70 ns with 15V)		5.0 10 15	40 20 15	20 10 7.5	- - -	ns
t_{rem}	Removal Times	Set	5.0 10 15	80 45 35	0 5 5	- - -	ns
		Reset	5.0 10 15	50 30 25	−35 −10 −5	- - -	

SWITCHING WAVEFORMS