TITLE:

DV430FHM-NN0 Preliminary Product Specification

BEIJING BOE DISPLAY TECHNOLOGY

REVISION HISTORY

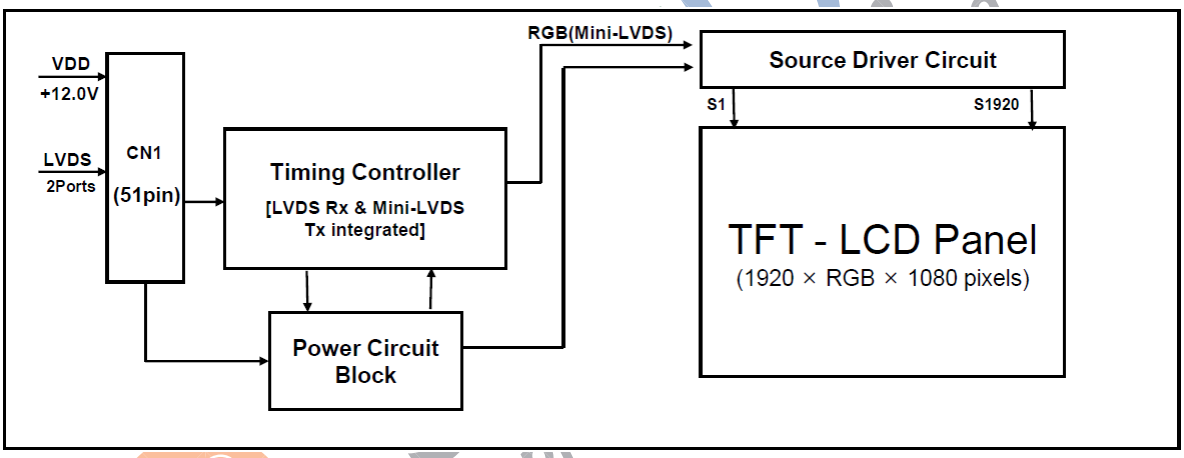
REV.	ECN NO.	DESCRIPTION OF CHANGES	DATE	PREPARED
P0	-	Initial Release	2015.12.24	Hao G.N
P1	-	Update	2016.01.31	Ye Heng

Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

DV430FHM-NN0 is a color active matrix TFT LCD MDL using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This MDL has a 42.5 inch diagonally measured active area with FHD resolutions (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M colors. The TFT-LCD panel is adapted for a low reflection and higher color type.



1.2 Features

- LVDS interface with 2 pixel / clock
- High-speed response
- Low color shift image quality
- 8-bit color depth, display 16.7M colors
- Narrow bezel and wide viewing angle, gate driver use GOA mode
- DE (Data Enable) only mode
- ADS technology is applied for high display quality
- RoHS compliant

1.3 Application

- Home Alone Multimedia TFT-LCD TV
- Display Terminals for Control System
- Ultra High Definition TV(UHD TV)
- AV application Products

1.4 General Specification

< Table 1. General Specifications >

Parameter	Specification	Unit	Remark
Active area	940.896(H) ×529.254(V)	mm	Array
Number of pixels	1920(H) ×1080(V)	pixels	
Pixel pitch	163.35(H) ×490.05(V)	㎛	Array
Pixel arrangement	Pixels RGB Vertical stripe		Array
Display colors	16.7M (8bits True)	colors	
Display mode®	Transmission mode, Normally Black		
Outline Dimension	961.7(H)x550.1(V)× 11.7(B)	mm	Mech
Weight	TBD(Typ)	Kg	Mech
Power Consumption	LED Driver:56.3W)	Watt	
Surface Treatment	Haze 1%		

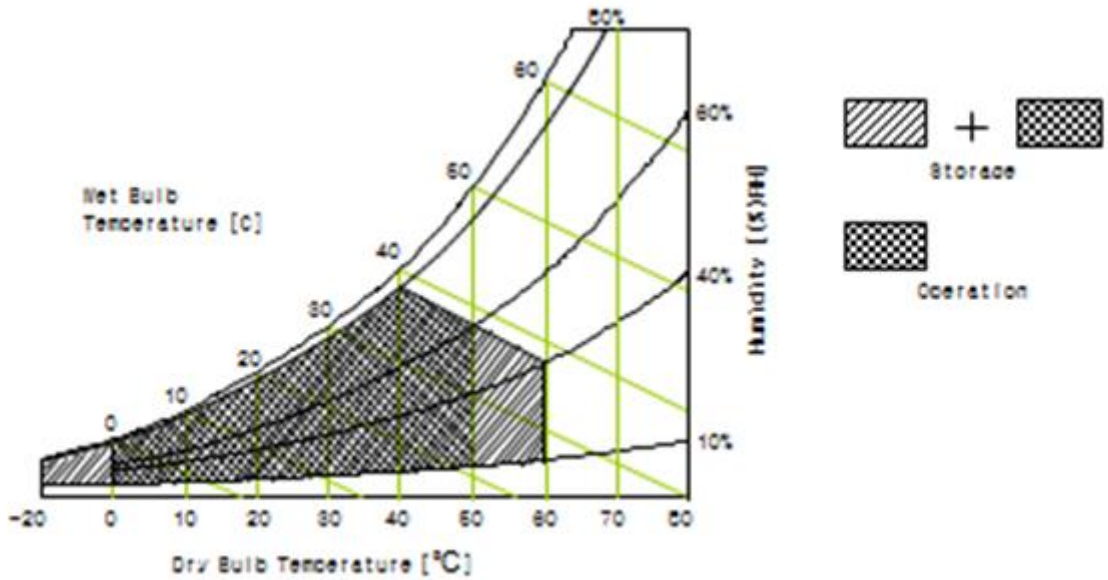
2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. LCD Module Electrical Specifications > [VSS=GND=0V]

Parameter		Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	LCD Module	VDD	VSS-0.3	13.5	V	Ta = 25 ℃
	Converter	VBL	VSS-0.3	26.4	V	
Operating Temperature		T_{OP}	0	+50	℃	Note 1
		T_{SUR}	-20	+60	℃	
Storage Temperature		T_{ST}	-20	+60	℃	
Operating Ambient Humidity		Hop	10	80	%RH	
Storage Humidity		Hst	10	80	%RH	

Note 1 : Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39 ℃ max. and no condensation of water.



3.0 ELECTRICAL SPECIFICATIONS

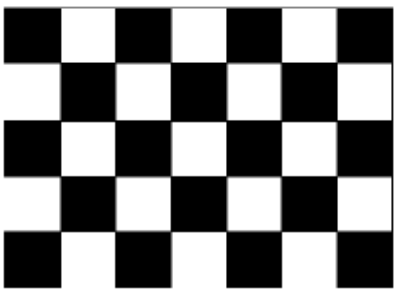
3.1 TFT LCD Open Cell

< Table 3. Open Cell Electrical Specifications > [Ta =25±2 ℃]

Parameter		Symbol	Values			Unit	Remark
			Min	Typ	Max		
Power Supply Input Voltage		VDD	10.8	12	13.2	Vdc	
Power Supply Ripple Voltage		VRP			300	mV	
Power Supply Current		IDD	-	0.5	0.95	A	Note 1
Power Consumption		PDD		6	11.4	Watt	
Rush current		IRUSH	-	-	3.0	A	Note 2
V by One Interface	Differential Input High Threshold Voltage	VLVTH	+100		+300	mV	
	Differential Input Low Threshold Voltage	VLVTL	-300		-100	mV	
	Common Input Voltage	VLVC	1.0	1.2	1.4	V	
	Terminating Resistor	Rt	90	100	110	ohm	
CMOS Interface	Input High Threshold Voltage	VIH	2.7	-	3.3	V	
	Input Low Threshold Voltage	VIL	0	-	0.6	V	

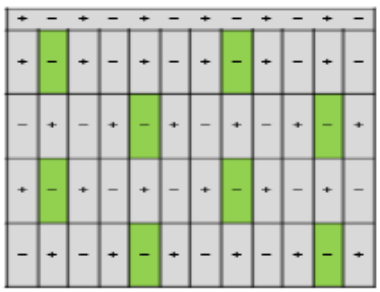
Note 1 : The supply voltage is measured and specified at the interface connector of LCM.
The current draw and power consumption specified is for VDD=12.0V,
Frame rate fV=60Hz and Clock frequency = 74.25MHz.
Test Pattern of power supply current

a) Typ : Mosaic 7X5 (L0/L255)



b) Max : Horizontal 1 Line (L0/L255))

c) Flicker Pattern



Note 2 : The duration of rush current is about 2ms and rising time of Power Input is 1ms(min)

3.2 LED Converter

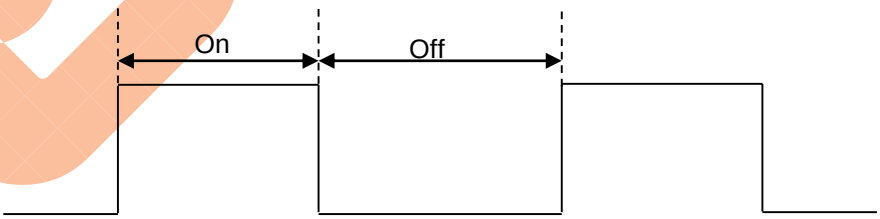
< Table 4. LED Converter Electrical Specifications >

[Ta =25±2℃]

Parameter	Symbol	Condition	Values			Unit	Note
			Min.	Typ.	Max.		
Input Voltage	VBL		23	24	25.2	V	
Input Current	IBL	V_{DIM}=3.3V		2.67		A	Note 1
Rush current	IRUSH	VBL= 24V		9.0		A	
Power Consumption	PBL	Typical Luminance		64		Watt	
B/L on/off control	$V_{ON/OFF}$	BL ON = High	2.8	3.3	5	V	
		BL OFF =Low	0	-	0.8	V	
Analog Dimming	V_{DIM}	Voltage	0		3.3	V	
	L_{DIM}	Luminance	20		100	%	
PWM Frequency	F_{PWM}		140	190	240	Hz	
PWM Level	High Level		2.8	3.3	5	V	
	Low Level		0	-	0.5	V	
PWM Duty	D_{PWM}		20	-	100	%	Note 2
Life Time			30k	-	-	Hrs	Note 3

Note 1:The specified current and power consumption are under the typical supply Input voltage, 24V. It is total power consumption.

Note 2 : High-duty = On/(On+Off) * 100



Note 3 : The life time of LED, 30,000Hrs, is determined as the time at which luminance of the LED is 50% compared to that of initial value at the typical LED current on condition of continuous operating at 25 ± 2°C.

4.0 INTERFACE CONNECTION

4.1 Open Cell Input Signal & Power

-LVDS Connector : PM.LVS.S040505101(UJC) or Equivalent.

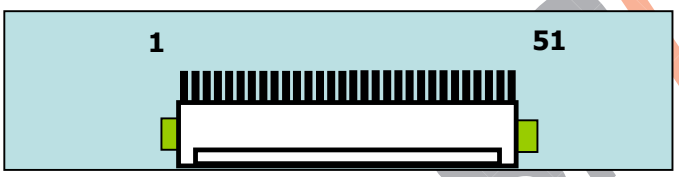
< Table 5. Open Cell Input Connector Pin Configuration >

Pin No	Symbol	Description	Pin No	Symbol	Description
1	NC	No connection	21	GND	Ground
2	SDA	I²C Data	22	CH1[3]-	First pixel negative LVDS differential data input. Pair3
3	SCL	I²C Clock	23	CH1[3]+	First pixel positive LVDS differential data input. Pair3
4	NC	Not Connected	24	NC	No connection
5	NC	Not Connected	25	NC	No connection
6	NC	Not Connected	26	NC	No connection
7	SELLVDS	High: JEIDA Low or Open: VESA	27	NC	No connection
8	NC	Not Connected	28	CH2[0]-	Second pixel negative LVDS differential data input. Pair0
9	NC	Not Connected	29	CH2[0]+	Second pixel positive LVDS differential data input. Pair0
10	NC	Not Connected	30	CH2[1]-	Second pixel negative LVDS differential data input. Pair1
11	GND	Ground	31	CH2[1]+	Second pixel positive LVDS differential data input. Pair1
12	CH1[0]-	First pixel negative LVDS differential data input. Pair0	32	CH2[2]-	Second pixel negative LVDS differential data input. Pair2
13	CH1[0]+	First pixel positive LVDS differential data input. Pair0	33	CH2[2]+	Second pixel positive LVDS differential data input. Pair2
14	CH1[1]-	First pixel negative LVDS differential data input. Pair1	34	GND	Ground
15	CH1[1]+	First pixel positive LVDS differential data input. Pair1	35	CH2CLK-	Second pixel negative LVDS clock
16	CH1[2]-	First pixel negative LVDS differential data input. Pair2	36	CH2CLK+	Second pixel positive LVDS clock
17	CH1[2]+	First pixel positive LVDS differential data input. Pair2	37	GND	Ground
18	GND	Ground	38	CH2[3]-	Second pixel negative LVDS differential data input. Pair3
19	CH1CLK-	First pixel negative LVDS clock	39	CH2[3]+	Second pixel positive LVDS differential data input. Pair3
20	CH1CLK+	First pixel positive LVDS clock			

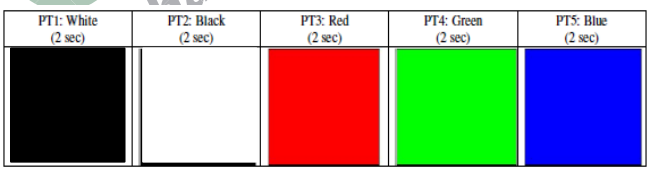
Pin No	Symbol	Description	Pin No	Symbol	Description
40	NC	Not Connected	46	GND	Ground
41	NC	Not Connected	47	NC	Not Connected
42	NC	Not Connected	48	VCC	Input Voltage +12V
43	NC	Not Connected	49	VCC	Input Voltage +12V
44	GND	Ground	50	VCC	Input Voltage +12V
45	GND	Ground	51	VCC	Input Voltage +12V

Notes : Notes : 1. NC(Not Connected) : This pins are only used for BOE internal operations.
2.Input Level of LVDS signal is based on the EIA-644 Standard.
3. LVDS_SEL: This pin is used for selecting LVDS signal data format.
If this Pin : High (3.3V) JEIDA LVDS format
Otherwise : Low(GND) or Open (NC) Normal NS LVDS format

Rear view of LCM



BIST Pattern



4.2 LED Converter Input Signal & Power

- Connector : CI0114M1HRL-NH (Cvilux) or equivalent

< Table 6. LED Converter Input Connector Pin Configuration >

CN1-14PIN-2.0

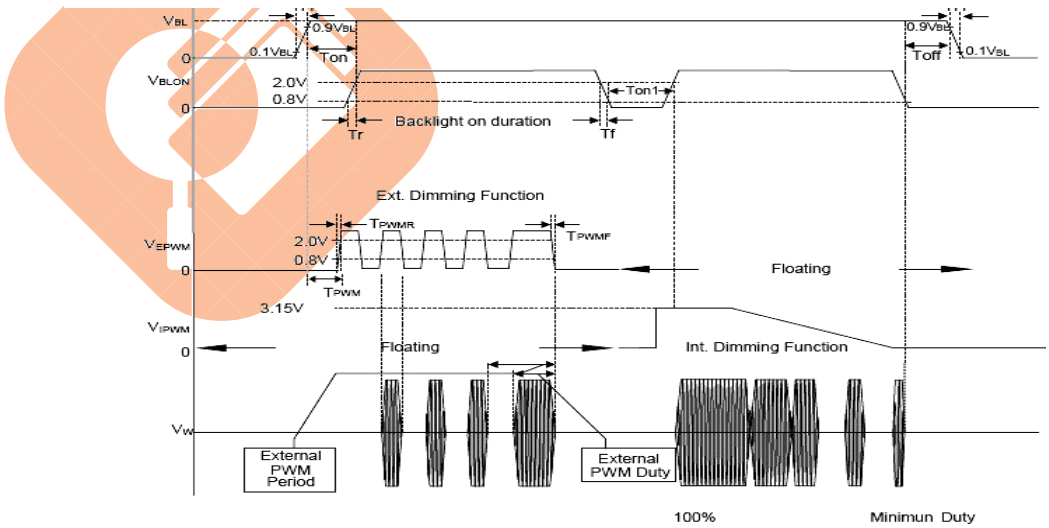
Pin No	Symbol	Description	
1	VBL	Power Supply +24V	
2	VBL	Power Supply +24V	
3	VBL	Power Supply +24V	
4	VBL	Power Supply +24V	
5	VBL	Power Supply +24V	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	GND	Ground	
11	NC	No Connection	
12	VBLON/OFF	BLU On-Off control	Max : 3.3V / Min : 0V
13	PWM 调光	0V:Min，3.3V:Max	On : 2.8V~5.0V/Off :0~0.8V
14	NC	NC	

Notice: 1. PIN 13:Extermal PWM Control .

2. While system is turned ON or OFF, the power sequences must follow as below descriptions:

Turn ON sequence: VBL-ON → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL-ON

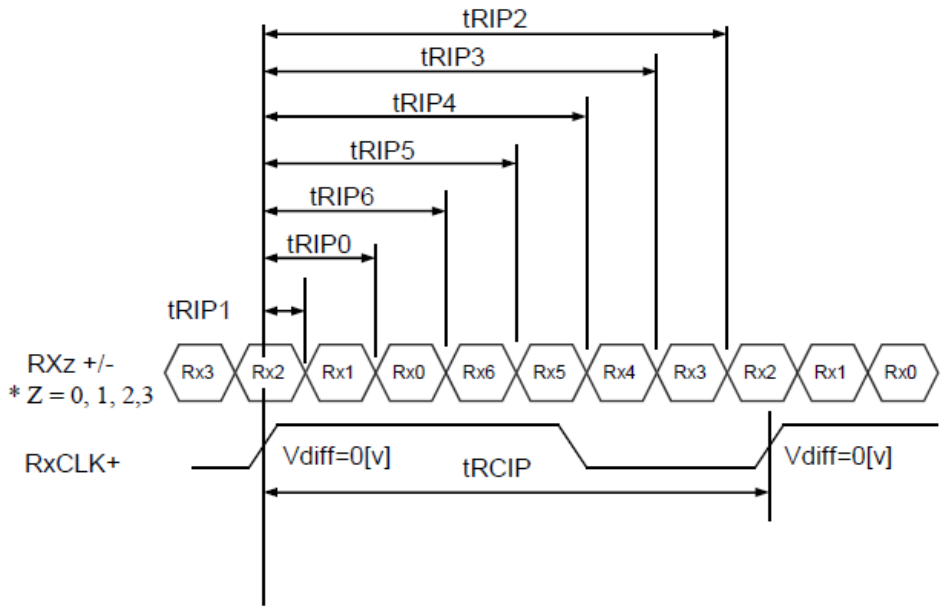


4.3 LVDS Interface

-LVDS Receiver : Timing Controller (LVDS Rx merged) / LVDS Data : Pixel Data

< Table 7. Open Cell Input Connector Pin Configuration >

Item	Symbol	Min	Typ	Max	Unit	Remark
CLKIN Period	tRCIP	10.31	13.47(10.78)	15.87	nsec	
Input Data 0	tRIP1	-0.42	0.0	+0.42	nsec	
Input Data 1	tRIP0	tRCIP/7-0.42	tRCIP/7	tRCIP/7+0.42	nsec	
Input Data 2	tRIP6	2 ×tRCIP/7-0.42	2 ×tRCIP/7	2 ×tRCIP/7+0.42	nsec	
Input Data 3	tRIP5	3 ×tRCIP/7-0.42	3 ×tRCIP/7	3 ×tRCIP/7+0.42	nsec	
Input Data 4	tRIP4	4 ×tRCIP/7-0.42	4 ×tRCIP/7	4 ×tRCIP/7+0.42	nsec	
Input Data 5	tRIP3	5 ×tRCIP/7-0.42	5 ×tRCIP/7	5 ×tRCIP/7+0.42	nsec	
Input Data 6	tRIP2	6 ×tRCIP/7-0.42	6 ×tRCIP/7	6 ×tRCIP/7+0.42	nsec	

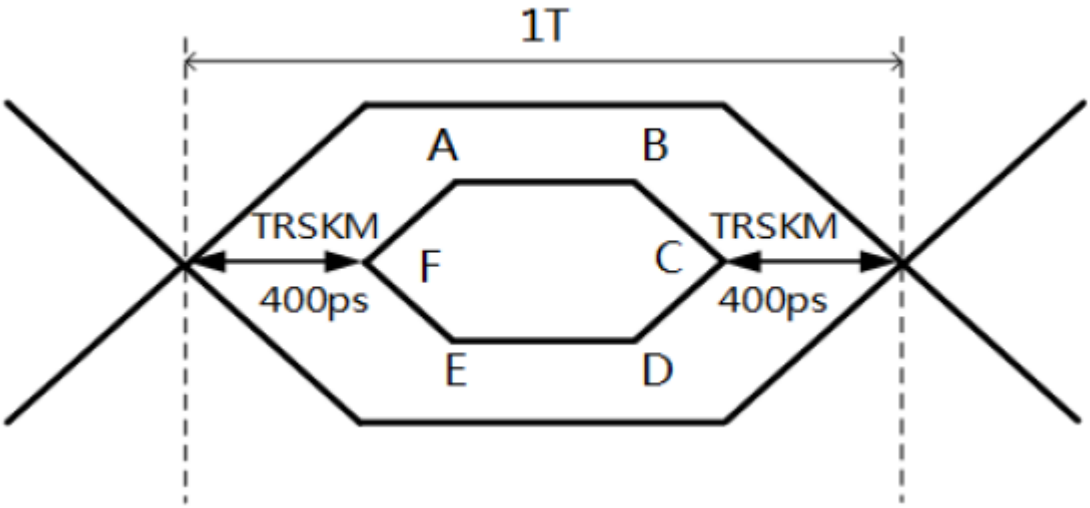


* Vdiff = (RXz+)-(RXz-),.... ,(RXCLK+)-(RXCLK-)

4.4 LVDS Rx Interface Eye Diagram

< Table 8. LVDS Rx Interface Eye Diagram>

Symbol	Min	Typ	Max	Unit	Note
A	—	100	—	mV	
B	—	100	—	mV	
C	—	0	—	mV	
D	—	-100	—	mV	
E	—	-100	—	mV	
F	—	0	—	mV	

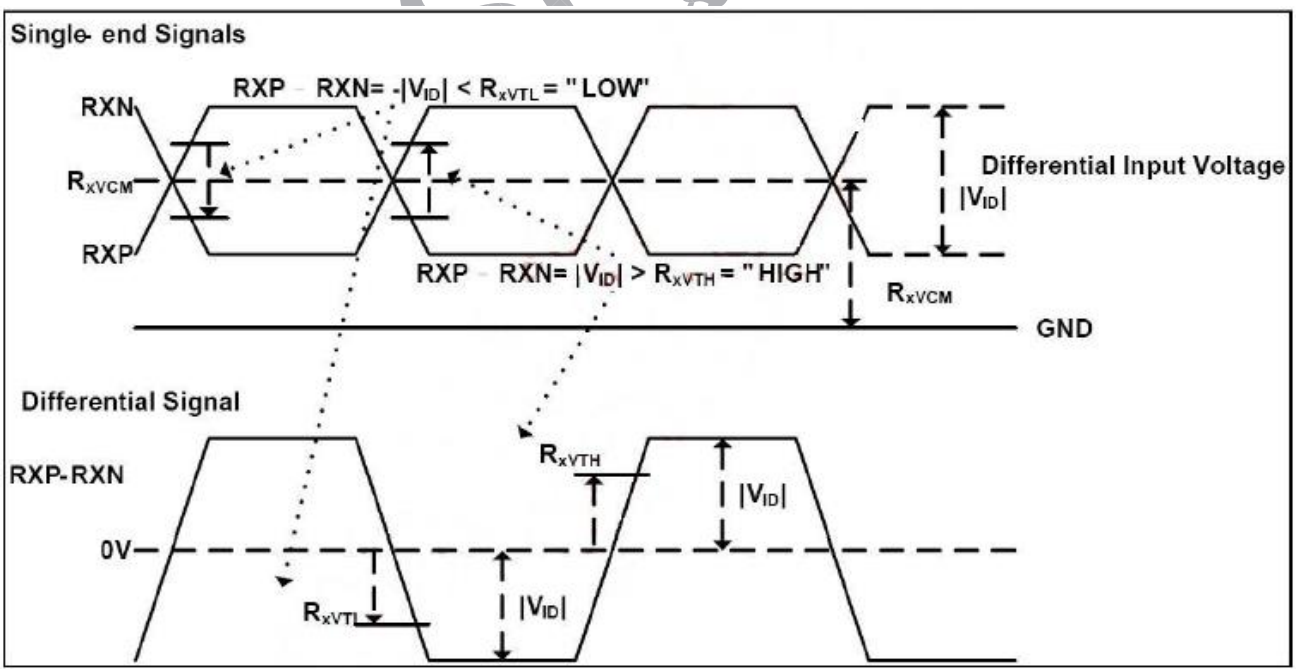


Notes:
1. Time F to A,B to C,C to D,E to F is 150p second.
2. LVDS clock=85Mhz.
3. The time A to B=1T−2*TRSKM−2*150ps.

4.5 LVDS Receiver Differential Input

< Table 9. LVDS Receiver Differential Input>

Symbol	Parameter	Min	Typ	Max	Unit	Condition
R_{xVTH}	Differential input high threshold voltage			+0.1v	V	RxVCM =1.2V
R_{xVTL}	Differential input low threshold voltage	-0.1V			V	
R_{XVIN}	Input voltage range (singled-end)	0		2.4	V	
R_{xVCM}	Differential input common mode voltage	$\lvert V_{ID} \rvert/2$		2.4-$\lvert V_{ID} \rvert/2$	V	
$\lvert V_{ID} \rvert$	Differential input voltage	0.1		0.6	V	



5.0 SIGNAL TIMING SPECIFICATION

5.1 Timing Parameters (DE only mode)

< Table 10. Timing Table >

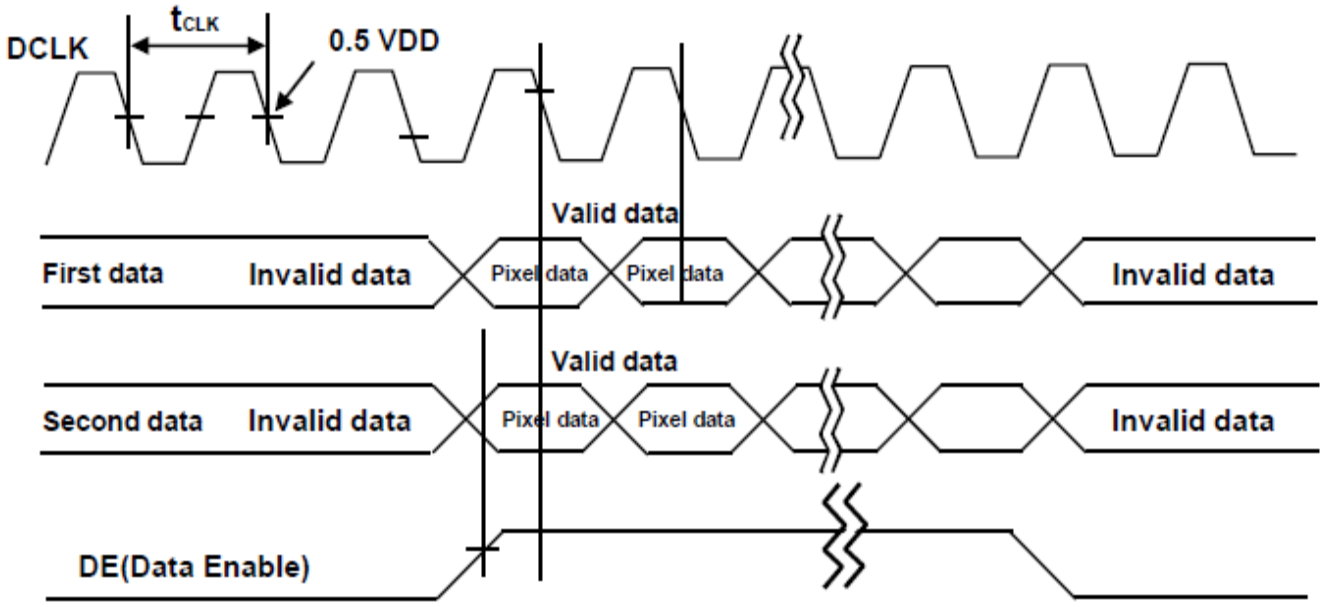
Item		Symbols		Min	Typ	Max	Unit
Clock	Frequency	1/Tc		60	74.25	78	MHz
	High Time	Tch		-	4/7Tc	-	
	Low Time	Tcl		-	4/7Tc	-	
Frame Period		Tv		1100	1125	1149	lines
				48.5	60	63	Hz
Horizontal Active Display Term		Valid	t_{HV}	-	960	-	t_{CLK}
		Total	t_{HP}	1060	1100	1200	t_{CLK}
Vertical Active Display Term		Valid	t_{VV}	-	1080	-	t_{HP}
		Total	t_{VP}	1100	1125	1149	t_{HP}

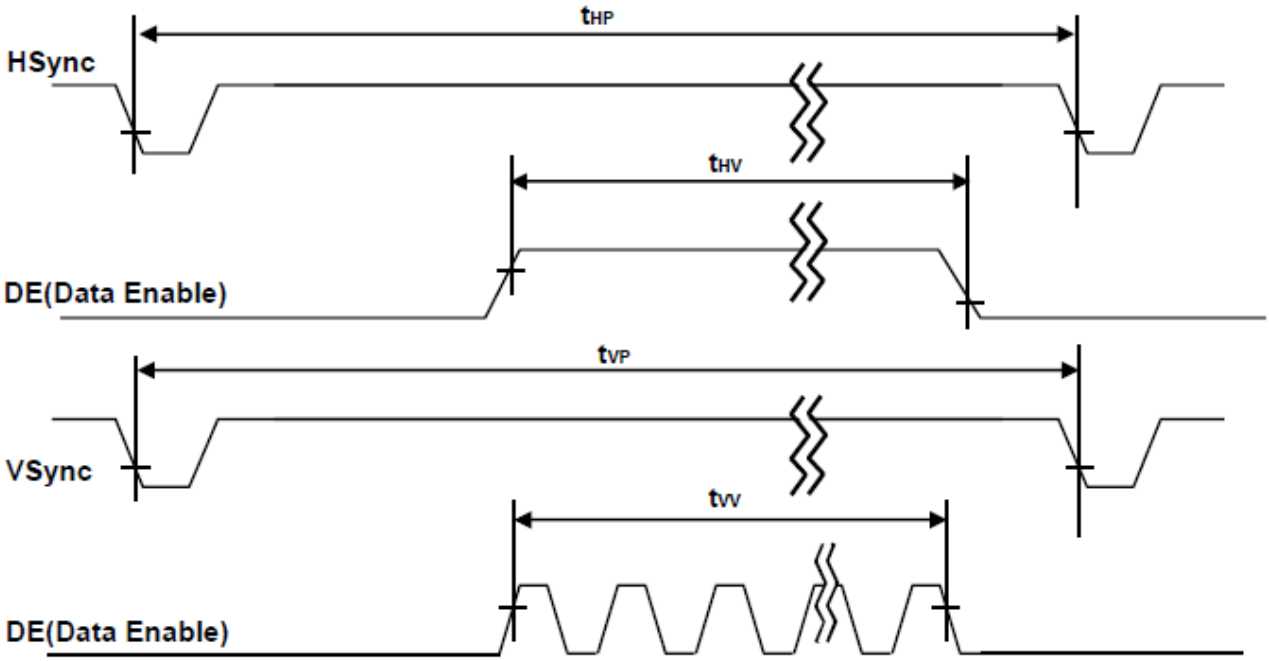
Notes: This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

< Table 11. LVDS Input SSCG>

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F	LVDS Input frequency	-	60	74.25	78	MHz
T_{LVSK}	LVDS channel to channel skew	F=100MHz V_{IC}=1.2V V_{ID}=±400mV	-380	-	+380	ps
F_{LVMOD}	Modulating frequency of input clock during SSC		60	-	85	KHz
F_{LVDEV}	Maximum deviation of input clock frequency during SSC		-3	-	+3	%
T_{CY-CY}	Cycle to Cycle jitter		-	-	100	ps

5.2 Signal Timing Waveform





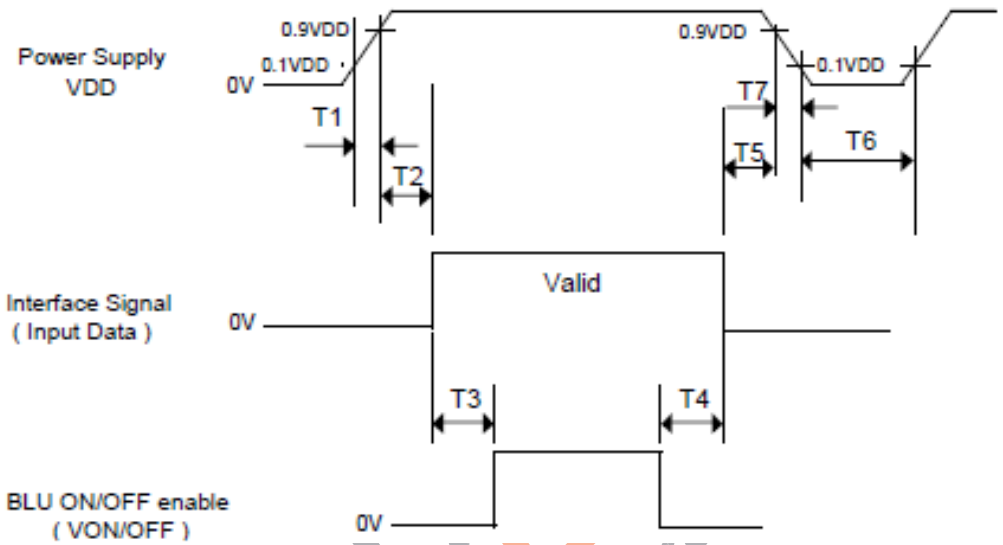
5.3 Input Signals, Basic Display Colors and Gray Scale of Colors

< Table 12. Input Signal and Display Color Table >

Color & Gray Scale		Input Data Signal																							
		Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▽	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	▽	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Gray Scale of White	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1
	▽	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

5.4 Power Sequence

To prevent a latch-up or DC operation of the Open Cell, the power on/off sequence shall be as shown in below



< Table 13. Sequence Table >

Parameter	Values			Units
	Min	Typ	Max	
T1	0.5	-	20	ms
T2	10	-	100	ms
T3	200	-	-	ms
T4	200	-	-	ms
T5	0	-	-	ms
T6	1	-	-	s

Notes: 1. Back Light must be turn on after power for logic and interface signal are valid.
2.Even though T1 is out of SPEC, it is still ok if the inrush current of VDD is below the limit.
3. When VDD<0.9VDD(Typ.),Power off.
4. T7 decreases smoothly, if there were rebounding voltage, it must smaller than 5 volts.

6.0 OPTICAL SPECIFICATIONS

The test of optical specifications shall be measured in a dark room (ambient luminance 1 lux andtemperature=25 2℃) with the equipment of Luminance meter system (Goniometer system and PR730) and test unit shall be located at an approximate distance 180cm from the LCD surface at a viewing angle of Θ and Φ equal to 0 . We refer to ΘØ=0(=Θ3) as the 3 o'clock direction (the "right"), ΘØ=90(= Θ12) as the 12 o'clock direction ("upward"), ΘØ=180(= Θ9) as the 9 o'clock direction ("left") and ΘØ=270(= Θ6) as the 6 o'clock direction ("bottom"). While scanning Θ and/or Ø, the center of the measuring spot on the Display surface shall stay fixed. The measurement shall be executed after 30 minutes warm-up period. VDD shall be 12.0V at 25 C. Optimum viewing angle direction is 6 'clock.

< Table 14. Optical Table >

[VDD = 12.0V, Frame rate = 60Hz, Ta =25±2 ℃]

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle	Horizontal	Θ_3	CR > 10		89		Deg.	Note 1
		Θ_9			89		Deg.	
	Vertical	Θ_{12}			89		Deg.	
		Θ_6			89		Deg.	
Color Temperature				9000	10,000	11,500	K	
Color Gamut				70	72	-	%	
Contrast ratio		CR	Θ = 0° (Center) Normal Viewing Angle	1000:1	1200:1	-		Note 2
Luminance of White		Y_w			380	-	cd/m^2	Note 3
White luminance uniformity		ΔY		70	75		%	Note 4
Reproduction of color	White	W_x		TYP. - 0.03	0.280	TYP. + 0.03		Note 5
		W_y			0.290			
	Red	R_x			TBD			
		R_y			TBD			
	Green	G_x			TBD			
		G_y			TBD			
	Blue	B_x			TBD			
		B_y			TBD			
Response Time	G to G	T_g		-	8	10	ms	Note 6
Gamma Scale				2.0	2.2	2.4		

Note：

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The vie wing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of = 0 and at the ce nter of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See Figure1 shown in App endix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The color chromaticity coordinates specified in Table 9.shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Me asurements shall be made at the center of the panel. The BLU is used by BOE.
4. Response time Tg is the average time required for display transition by switchin g the input signal as below table and is based on Frame rate fV =60Hz to optimi ze.Each time in below table is defined as Figure 2and shall be measured by swit ching the

Measured Response Time		Target																
		0	15	31	47	63	79	95	111	127	143	159	175	191	207	223	239	255
Start	0																	
	15																	
	31																	
	47																	
	63																	
	79																	
	95																	
	111																	
	127																	
	143																	
	159																	
	175																	
	191																	
	207																	
	223																	
	239																	
	255																	

5. Definition of Transmittance (T%) :
Module is with white(L255) signal input

$$\text{Transmittance} = \frac{\text{Luminance of LCD Module}}{\text{Luminance of BLU}} \times 100\ \%$$

7.0 MECHANICAL CHARACTERISTICS

7.1 Dimensional Requirements

Figure 4 (located in Appendix) shows mechanical outlines for the model DV430FHM-NN0. Other parameters are shown in Table 15.

< Table 15. Dimensional Parameters >

Parameter	Specification	Unit
Dimensional outline	961.7(H)x550.0(V)× 11.7(B)	mm
Weight	*(Typ)	Kg
Active area	940.896(H) ×529.254(V)	mm
Pixel pitch	163.35(H) ×490.05(V)	mm
Number of pixels	1920(H) ×1080(V) (1 pixel = R + G + B dots)	pixels
Back-light	E-LED Backlight	

7.2 Mounting

See Figure 5. (Shown in Appendix)

7.3 Anti-Glare and Polarizer Hardness

The surface of the LCD has an Anti-glare coating to minimize reflection and a coating to Reduce scratching.

8.0 RELIABILITY TEST

The Reliability test items and its conditions are shown in below.

< Table 16. Reliability Test Parameters >

No	Test Items	Conditions
1	High temperature storage test	Ta = 60 ℃, 240 hrs
2	Low temperature storage test	Ta = -20 ℃, 240 hrs
3	High temperature & high humidity operation test	Ta = 50 ℃, 80%RH, 240hrs
4	High temperature operation test	Ta = 50 ℃, 240hrs
5	Low temperature operation test	Ta = 0 ℃, 240hrs
6	Thermal shock	Ta = -20 ℃ ↔ 60 ℃ (0.5 hr), 100 cycle
7	Vibration test (non-operating)	Frequency : 10 ~ 300 Hz, Random Gravity / AMP : 1.0 Grms Period : X, Y, Z 30 min/axis
8	Shock test (non-operating)	Gravity : 50G Pulse width : 11msec, Sine wave ±X, ±Y, ±Z Once for each direction
9	Electro-static discharge test	Air : ±15kV ,150pF/330Ω ,100Point ,1time/Point Contact : ±8kV ,150pF/330Ω ,100Point ,1time/Point Non operation Contact: ±4KV~±6KV,150pF/330Ω,100Point, Input connector Pin, 3 times/pin with no function loss

9.0 PRODCUT SERIAL NUMBER

1		2	3	4		5	6				7						
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

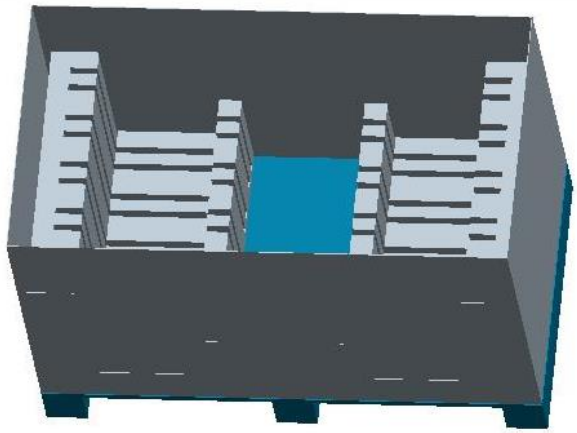
1. Control Number
2. Rank / Grade
3. Line Classification
4. Year (2011 : 11, 2012 : 12, …)
5. Month (1,2,3, … , 9, X, Y, Z)
6. Internal Use
7. Serial Number

10.0 PACKING INFORMATION

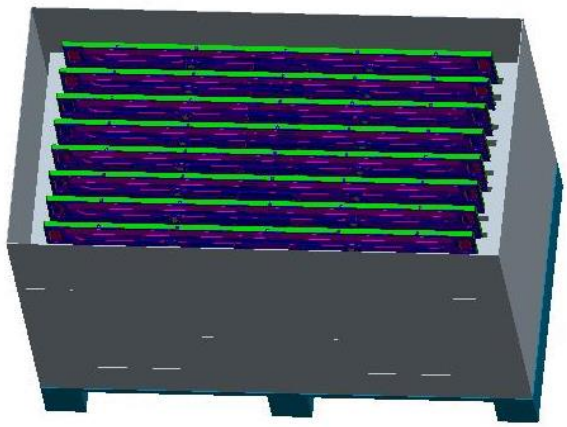
BOE provides the standard shipping container for customers, unless customer specifies their packing information. The standard packing method and Barcode information are shown in below

10.1 Packing Order

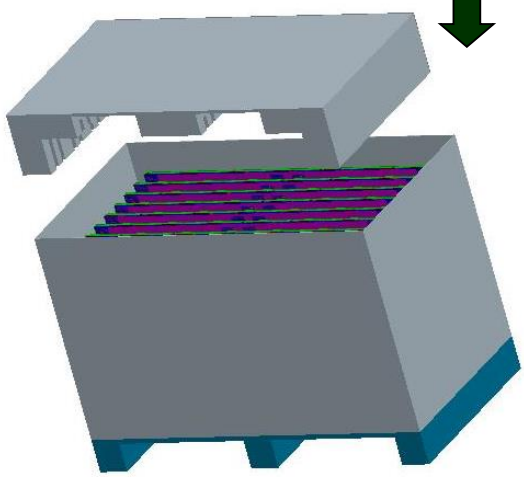
Put inner EPS-lower on the pallet



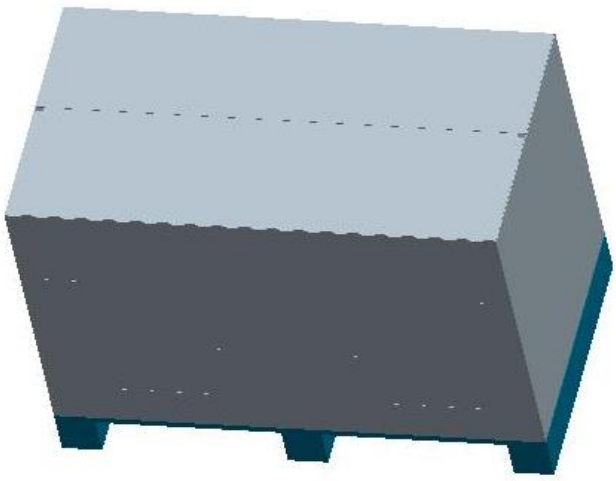
Put inner EPS-lower on the pallet



Put the other EPS-box on the first



Seal the box and stick label to the assigned area



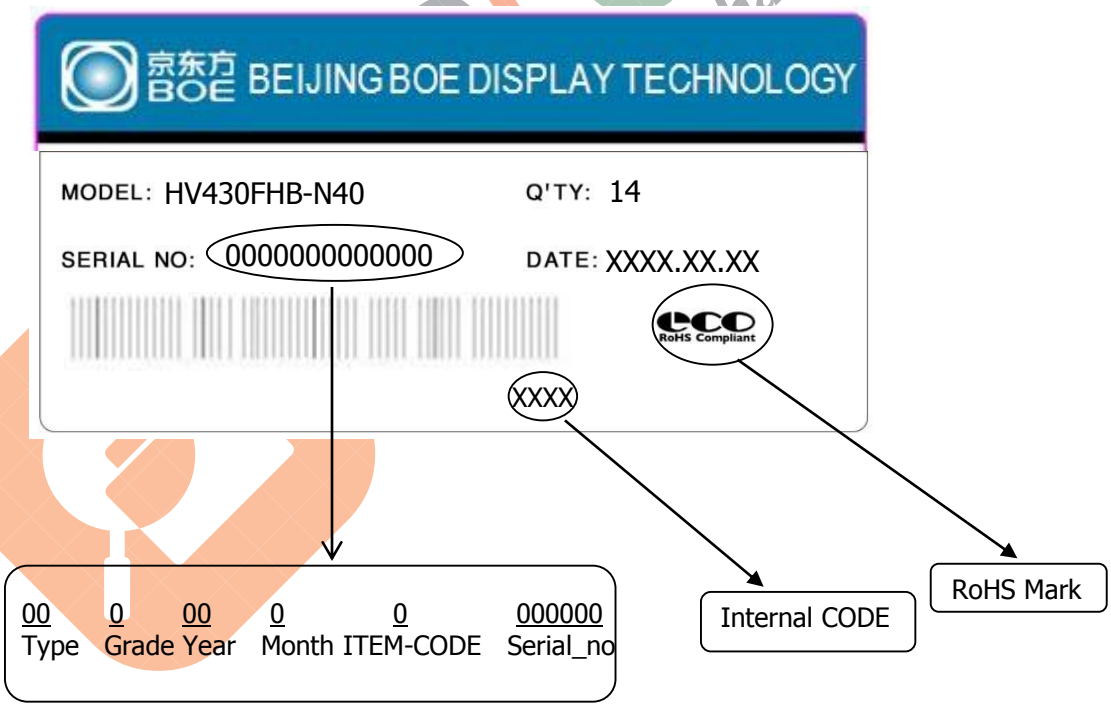
10.2 Packing Note

- Box Dimension : 1060mm (L) × 600mm (W) ×655mm (H)
- Package Quantity in one Box : 10pcs

10.3 Box Label

- Label Size : 110 mm (L) × 55 mm (W)
- Contents

  Model : DV430FHM-NN0
  Q`ty : 10 Module in one box.
  Serial No. : Box Serial No. See next page for detail description.
  Date : Packing Date
  FG Code : FG Code of Product



11.0 HANDLING & CAUTIONS

(1) Cautions when taking out the module
- Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module
- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation
- When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

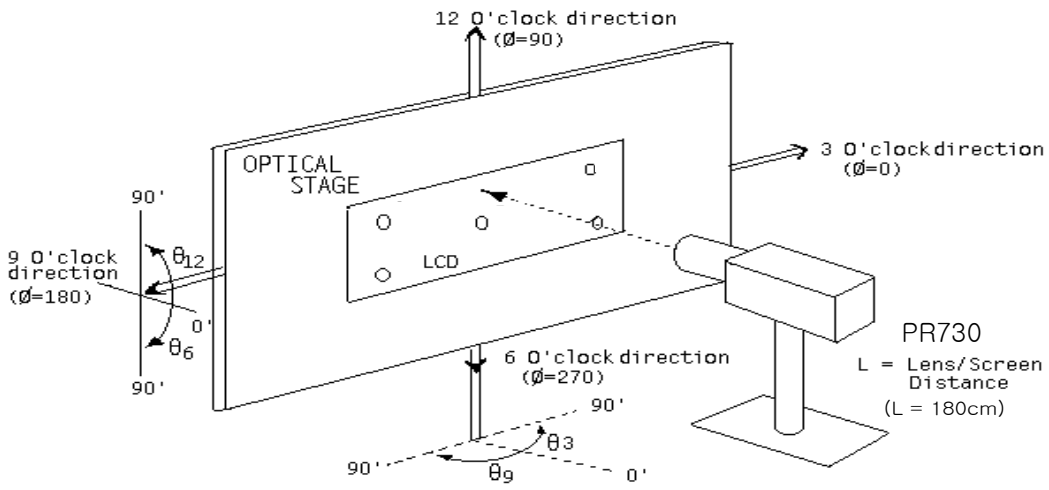
(4) Cautions for the atmosphere
- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics
- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

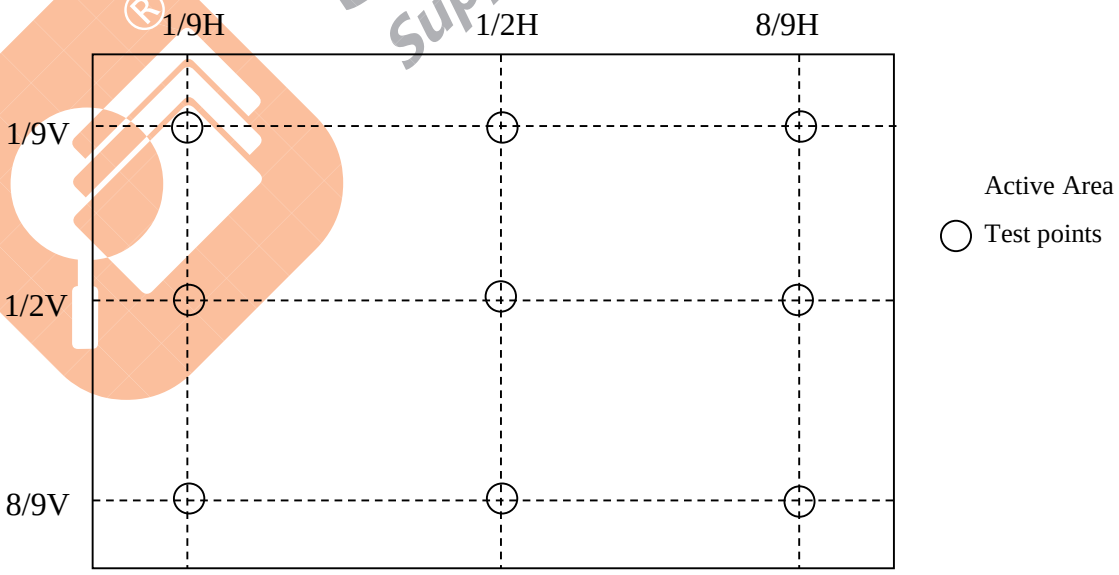
(6) Other cautions
- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc., Please pack the module not to be broken. We recommend to use the original shipping packages.

12.0 APPENDIX

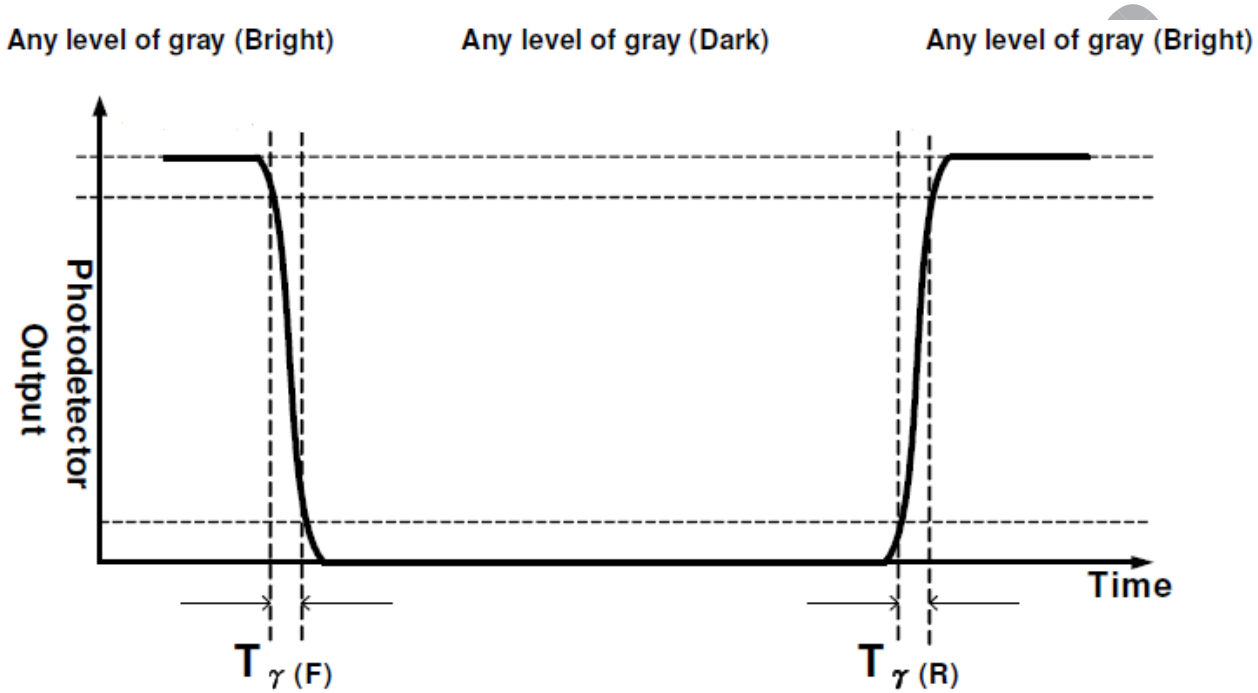
< Figure 1. Measurement Set Up >



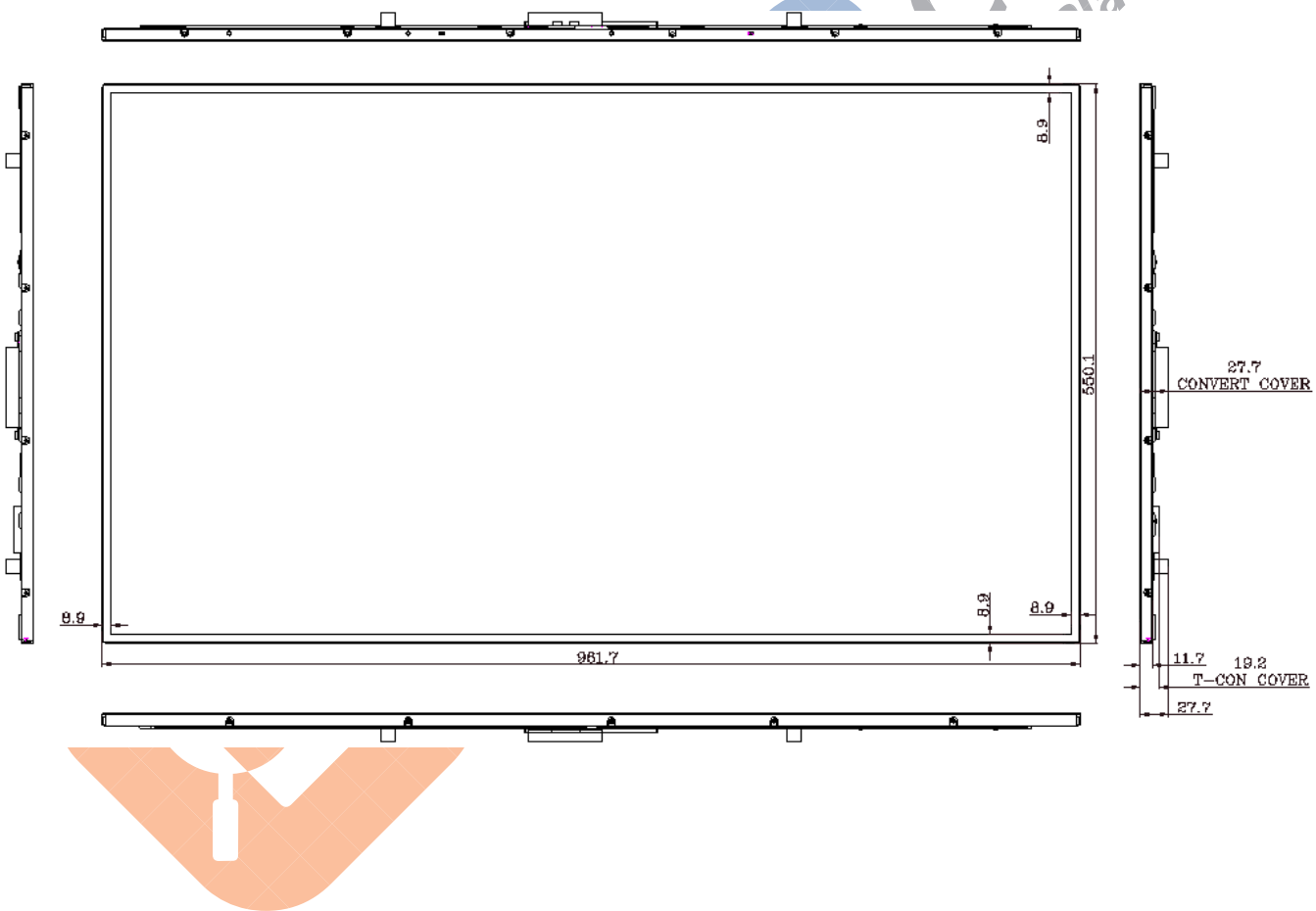
< Figure 2. White Luminance and Uniformity Measurement Locations >



< Figure 3. Response Time Testing >



< Figure 4. TFT-LCD Module Outline Dimensions (Front View) >



< Figure 5. TFT-LCD Module Outline Dimensions (Rear View) >