TITLE:

产品名：DV550FHM-NV1

Product Specification

Rev. 0

BEIJING BOE DISPLAY TECHNOLOGY CO.,LTD.

REVISION HISTORY

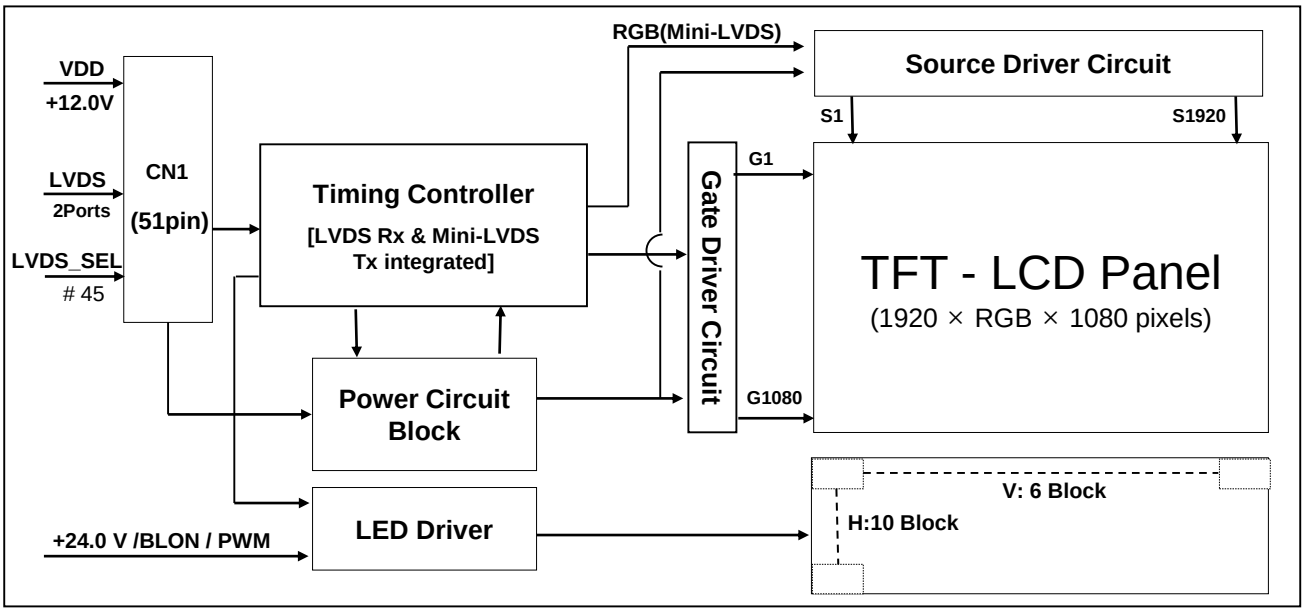
REV.	ECN NO.	DESCRIPTION OF CHANGES	DATE	PREPARED
O	-	Original Release	2017.01.23	Zhong Wei

Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

DV550FHM-NV1 is a color active matrix TFT LCD Module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 55.00 inch diagonally measured active area with FHD resolutions (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M colors. The TFT-LCD panel used for this module is adapted for a low reflection and higher color type.



1.2 Features

- LVDS interface with 2 pixel / clock
- High-speed response
- 8-bit color depth, display 16.7M colors
- Low power consumption
- Direct LED Backlight(180ea)
- DE (Data Enable) only mode
- ADS technology is applied for high display quality
- RoHS compliant

1.3 Application

- Home Alone Multimedia TFT-LCD TV
- Display Terminals for Control System
- Full High Definition TV(FHD TV)
- LFD application Products

1.4 General Specification

< Table 1. General Specifications >

Parameter	Specification	Unit	Remark
Active area	1209.6(H) × 680.4 (V)	mm	
Number of pixels	1920(H) ×1080(V)	pixels	
Pixel pitch	210(H) ×RGB×630(V)	㎛	
Pixel arrangement	Pixels RGB Vertical stripe		
Display colors	16.7M(8bits-true)	colors	
Display mode	Transmission mode, Normally Black		
Brightness	800(Typ.)	nit	Center point
Weight	18760	gram	
Power Consumption	198(Typ.)	Watt	
Surface Treatment	Haze25% ,3H, (Front Polarizer) Clear (Bottom Polarizer)		

2.0 ABSOLUTE MAXIMUM RATINGS

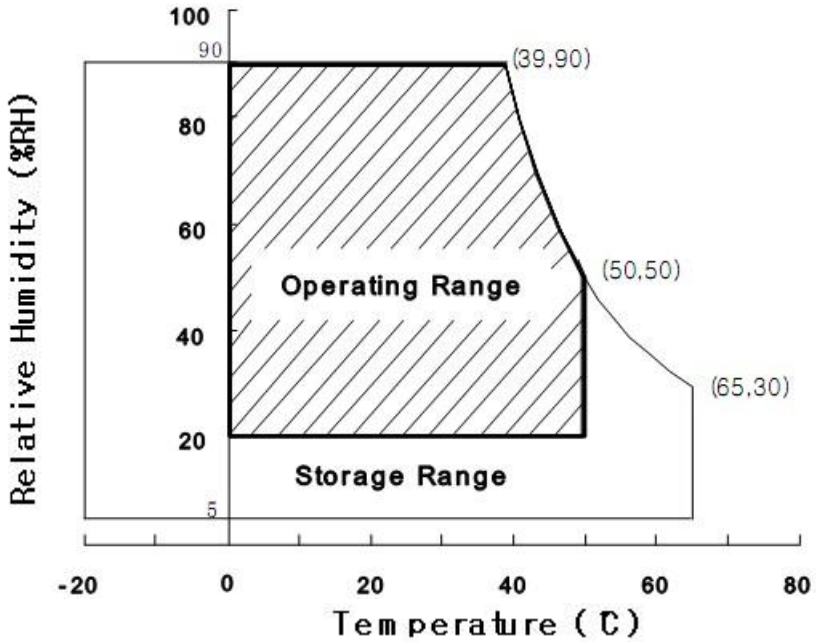
The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Open Cell Electrical Specifications >

[VSS=GND=0V]

Parameter	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	V_{DD}	V_{SS}-0.3	13.5	V	Ta = 25 ℃
Logic Supply Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V	
LED Channel Current	I_{BL}	-	280	mA	
Operating Temperature	T_{OP}	0	+50	℃	Note 1
Storage Temperature	T_{ST}	-20	+65	℃	

Note 1 : Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39 ℃ max. and no condensation of water.



3.0 ELECTRICAL SPECIFICATIONS

3.1Electrical Specifications

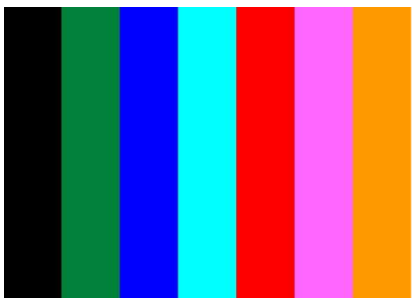
< Table 3. Electrical Specifications >

[Ta =25±2 ℃]

Parameter		Symbol	Values			Unit	Remark
			Min	Typ	Max		
Power Supply Input Voltage		VDD	10.8	12	13.2	Vdc	
Power Supply Ripple Voltage		VRP	-	-	300	mV	
Power Supply Current		IDD	-	600	1000	mA	Note 1
Power Consumption		PDD	-	7.2	13.2	Watt	
Rush current		IRUSH	-	-	5	A	Note 2
LVDS Interface	Differential Input High Threshold Voltage	VLVTH	+100		+600	mV	
	Differential Input Low Threshold Voltage	VLVTL	-600		-100	mV	
	Common Input Voltage	VLVC	1.0	1.2	1.4	V	
CMOS Interface	Input High Threshold Voltage	VIH	2.7	-	3.3	V	
	Input Low Threshold Voltage	VIL	0	-	0.6	V	

Note 1 : The supply voltage is measured and specified at the interface connector of LCM.
The current draw and power consumption specified is for VDD=12.0V,
Frame rate f_V=60Hz and Clock frequency = 75.4MHz.
Test Pattern of power supply current

a) Typ : Color Test (L0/L255)



b) Max : Horizontal 1 Line (L0/L255)

Note 2 : The duration of rush current is about 2ms and rising time of Power Input is 1ms(min)

3.2 Converter Electrical Specifications

< Table 4. Converter Electrical Specifications > [Ta =25±2℃]

Parameter		Symbol		Values			Unit	Remark
				Min	Typ	Max		
Power Supply Input Voltage		VDD		21.6	24	26.4	Vdc	
Power Supply Ripple Voltage		VRP		-	-	400	mV	
Power Supply Current		IDD		-	7.91	10	A	
Power Consumption		PDD		-	190	205	Watt	
SPI Interface	SI	V_{SI}	HI	2.4	3.3	3.6	V	
			LO	0	-	0.3	V	
	SO	V_{SO}	HI	2.4	3.3	3.6	V	
			LO	0	-	0.3	V	
	SCK	V_{SCK}	HI	2.4	3.3	3.6	V	
			LO	0	-	0.3	V	
	SCS	V_{SCS}	HI	2.4	3.3	3.6	V	
			LO	0	-	0.3	V	
Backlight On/Off Control Voltage		V_{BLON} (off)		0	-	0.3	V	
		V_{BLON} (on)		2.4	3.3	5.0	V	
Backlight PWM		High Level		2.4	3.3	3.6	V	On duty
		Low Level		0	-	0.3	V	Off duty
		Dimming Ratio		1	-	100	%	Note1
		PWM Frequency		100	-	300	Hz	
Light Bar Forward Voltage		$V_{F\_Light\ Bar}$		9.6	-	13.6	V	
LED Forward Current		I_F		-	280	-	mA	
Light Bar Forward Voltage Difference		△Vf		-	-	0.2	V	

Note1: 正常显示时TCON Board输出给Converter的分区占空比与PWM信号的占空比之积必须保证在1%以上

4.0 INTERFACE CONNECTION

4.1 Module Input Signal & Power

- Connector : IS050-C51B-C39-S (UJU) / FI-RE51S-HF-R1500 (JAE) or Equivalent.

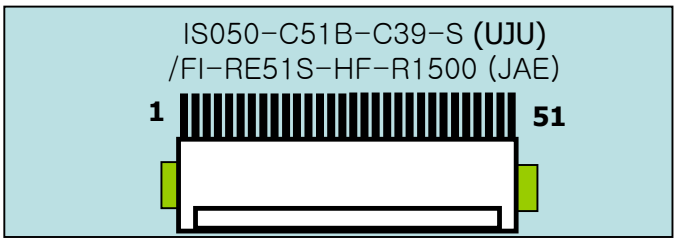
< Table 5. Input Connector Pin Configuration >

Pin No	Symbol	Description	Pin No	Symbol	Description
1	VCC	Input Voltage	20	CH1[3]-	First pixel negative LVDS differential data input. Pair3
2	VCC	Input Voltage	21	CH1[3]+	First pixel positive LVDS differential data input. Pair3
3	VCC	Input Voltage	22	CH1[4]-	First pixel negative LVDS differential data input. Pair4
4	VCC	Input Voltage	23	CH1[4]+	First pixel positive LVDS differential data input. Pair4
5	VCC	Input Voltage	24	GND	Ground
6	NC	Not Connected	25	CH2[0]-	Second pixel negative LVDS differential data input. Pair0
7	GND	Ground	26	CH2[0]+	Second pixel positive LVDS differential data input. Pair0
8	GND	Ground	27	CH2[1]-	Second pixel negative LVDS differential data input. Pair1
9	GND	Ground	28	CH2[1]+	Second pixel positive LVDS differential data input. Pair1
10	CH1[0]-	First pixel negative LVDS differential data input. Pair0	29	CH2[2]-	Second pixel negative LVDS differential data input. Pair2
11	CH1[0]+	First pixel positive LVDS differential data input. Pair0	30	CH2[2]+	Second pixel positive LVDS differential data input. Pair2
12	CH1[1]-	First pixel negative LVDS differential data input. Pair1	31	GND	Ground
13	CH1[1]+	First pixel positive LVDS differential data input. Pair1	32	CH2CLK-	First pixel negative LVDS clock
14	CH1[2]-	First pixel negative LVDS differential data input. Pair2	33	CH2CLK+	First pixel positive LVDS clock
15	CH1[2]+	First pixel positive LVDS differential data input. Pair2	34	GND	Ground
16	GND	Ground	35	CH2[3]-	Second pixel negative LVDS differential data input. Pair3
17	CH1CLK-	First pixel negative LVDS clock	36	CH2[3]+	Second pixel positive LVDS differential data input. Pair3
18	CH1CLK+	First pixel positive LVDS clock	37	CH2[4]-	Second pixel negative LVDS differential data input. Pair4
19	GND	Ground	38	CH2[4]+	Second pixel positive LVDS differential data input. Pair4

Pin No	Symbol	Description	Pin No	Symbol	Description
39	GND	Ground	46	NC	Not Connected
40	NC	Not Connected	47	NC	Not Connected
41	Local Dimming	'L' = Disable	48	NC	Not Connected
42	NC	Not Connected	49	NC	Not Connected
43	NC	Not Connected	50	NC	Not Connected
44	NC	Not Connected	51	NC	Not Connected
45	SELLVDS	High or Open: VESA Low : JEIDA			

Notes : 1. NC(Not Connected) : This pins are only used for BOE internal operations.
2. Input Level of LVDS signal is based on the IEA 664 Standard.
3. LVDS_SEL : This pin is used for selecting LVDS signal data format.
If this Pin : High (3.3V) or Open(NC)→VESA LVDS format
Otherwise : Low (GND) → JEIDA LVDS format

Rear view of LCM



BIST Pattern

4.2 BLU Input Signal & Power

- Connector : CI0114M1HR0-NH(Manufactured by Cvilux) or Equivalent.

< Table 6. Input Connector Pin Configuration CN8 for Master Board >

Pin No	Symbol	Description	Pin No	Symbol	Description
1	VIN	Operating Voltage Supply, +24V DC regulated	8	GND	Ground and Current Return
2	VIN	Operating Voltage Supply, +24V DC regulated	9	GND	Ground and Current Return
3	VIN	Operating Voltage Supply, +24V DC regulated	10	GND	Ground and Current Return
4	VIN	Operating Voltage Supply, +24V DC regulated	11	NC	No Connection
5	VIN	Operating Voltage Supply, +24V DC regulated	12	BLON	BLU On-Off control: DC 0 to 0.3V off，DC 2.4 to 5.25V On
6	GND	Ground and Current Return	13	PWM 调光	0V:Min，3.3V:Max
7	GND	Ground and Current Return	14	NC	No Connection

< Table 7. Input Connector Pin Configuration CN8 for Slave Board >

- Connector : CI0114M1HR0-NH(Manufactured by Cvilux) or Equivalent.

Pin No	Symbol	Description	Pin No	Symbol	Description
1	VIN	Operating Voltage Supply, +24V DC regulated	8	GND	Ground and Current Return
2	VIN	Operating Voltage Supply, +24V DC regulated	9	GND	Ground and Current Return
3	VIN	Operating Voltage Supply, +24V DC regulated	10	GND	Ground and Current Return
4	VIN	Operating Voltage Supply, +24V DC regulated	11	NC	No Connection
5	VIN	Operating Voltage Supply, +24V DC regulated	12	NC	No Connection
6	GND	Ground and Current Return	13	NC	No Connection
7	GND	Ground and Current Return	14	NC	No Connection

4.3 LVDS Interface

- LVDS Receiver : Timing Controller (LVDS Rx merged) / LVDS Data : Pixel Data

< Table 8. Input Connector Pin Configuration >

Channel No.	Data No.	8-bit LVDS Type	
		VESA	JEIDA
0	Bit-0	R0	R2
	Bit-1	R1	R3
	Bit-2	R2	R4
	Bit-3	R3	R5
	Bit-4	R4	R6
	Bit-5	R5	R7
	Bit-6	G0	G2
1	Bit-0	G1	G3
	Bit-1	G2	G4
	Bit-2	G3	G5
	Bit-3	G4	G6
	Bit-4	G5	G7
	Bit-5	B0	B2
	Bit-6	B1	B3
2	Bit-0	B2	B4
	Bit-1	B3	B5
	Bit-2	B4	B6
	Bit-3	B5	B7
	Bit-4	HS	HS
	Bit-5	VS	VS
	Bit-6	DE	DE
3	Bit-0	R6	R0
	Bit-1	R7	R1
	Bit-2	G6	G0
	Bit-3	G7	G1
	Bit-4	B6	B0
	Bit-5	B7	B1
	Bit-6	-	

5.0 SIGNAL TIMING SPECIFICATION

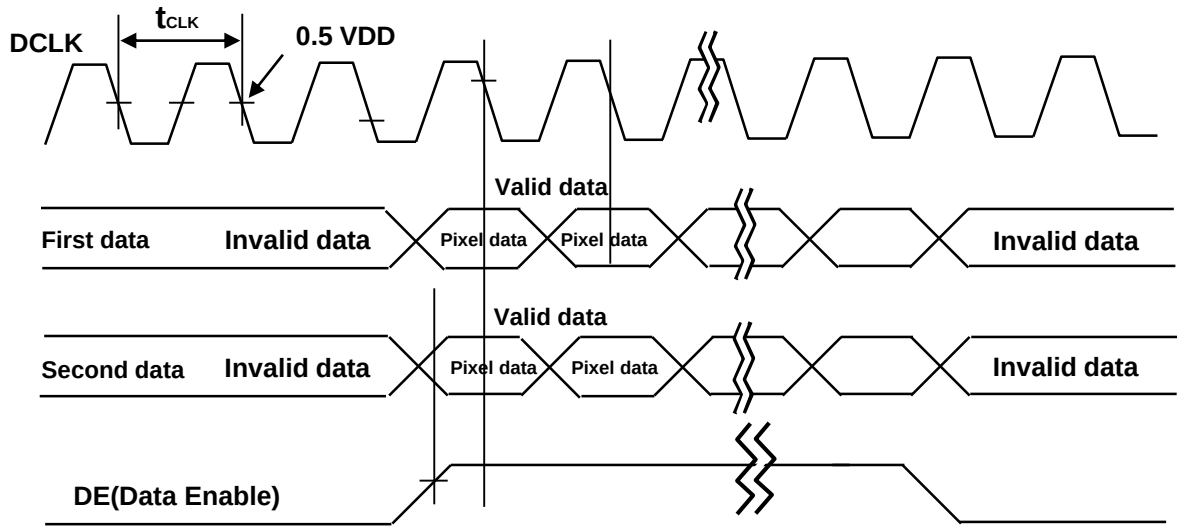
5.1 Timing Parameters (DE only mode)

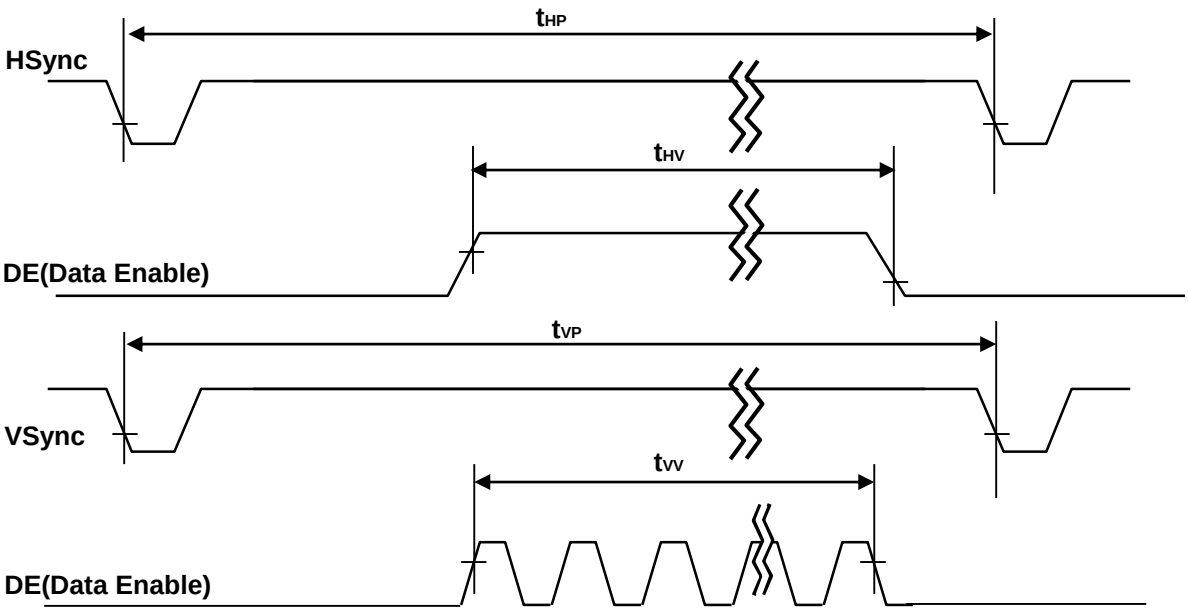
< Table 9. Timing Table >

Item		Symbols	Min	Typ	Max	Unit
Clock	Frequency	1/Tc	66.00	74.25	82	MHz
	High Time	Tch	-	4/7Tc	-	
	Low Time	Tcl	-	4/7Tc	-	
Frame Period		Tv	1100	1125	1149	lines
			57	60	63	Hz
Vertical Display Period		Tvd	-	1080	-	lines
One line Scanning Period		Th	1050	1100	1150	clocks
Horizontal Display Period		Thd	960	960	960	clocks

Notes: This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

5.2 Signal Timing Waveform





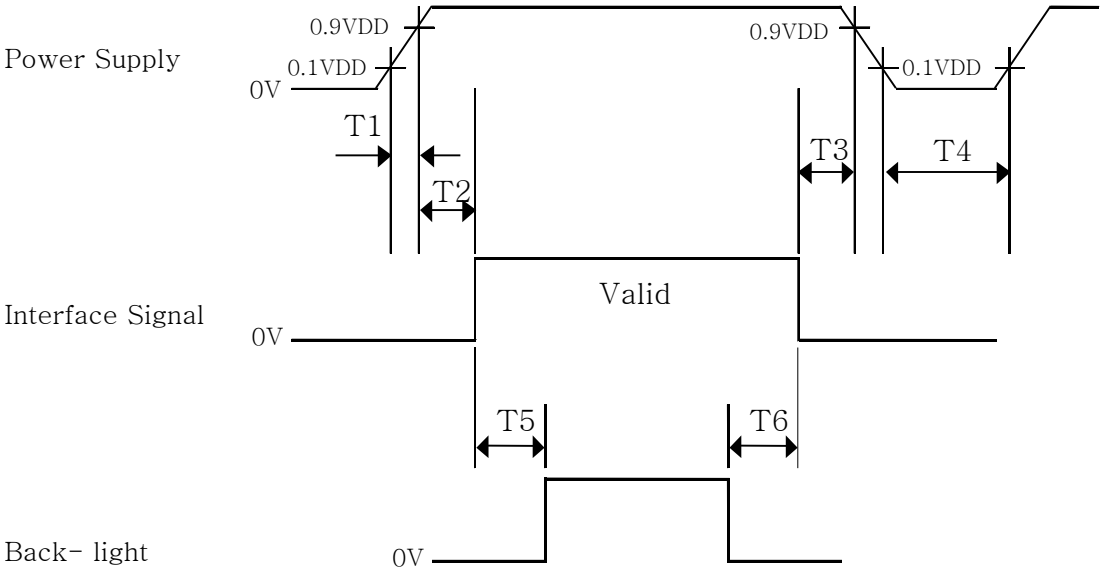
5.3 Input Signals, Basic Display Colors and Gray Scale of Colors

< Table 10. Input Signal and Display Color Table >

Color & Gray Scale		Input Data Signal																							
		Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▽	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	▽	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Gray Scale of White	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1
	▽	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

5.4 Power Sequence

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below



- 0.5 ms ≤ T1 ≤ 10 ms
- 0 ≤ T2 ≤ 50 ms
- 0 ≤ T3 ≤ 50 ms
- 1 sec ≤ T4
- 200 ms ≤ T5
- 200 ms ≤ T6

Notes:

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on.
3. Back Light must be turn on after power for logic and interface signal are valid.

6.0 OPTICAL SPECIFICATIONS

The test of optical specifications shall be measured in a dark room (ambient luminance≤1 lux and temperature=25±2℃) with the equipment of Luminance meter system (Goniometer system and PR730) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to $\theta_{Ø=0}$ (=θ_3) as the 3 o'clock direction (the "right"), $\theta_{Ø=90}$ (= θ_{12}) as the 12 o'clock direction ("upward"), $\theta_{Ø=180}$ (= θ_9) as the 9 o'clock direction ("left") and $\theta_{Ø=270}$(= θ_6) as the 6 o'clock direction ("bottom"). While scanning θ and/or Ø, the center of the measuring spot on the Display surface shall stay fixed. The measurement shall be executed after 30 minutes warm-up period. VDD shall be 12.0V +/-10% at 25°C. Optimum viewing angle direction is 6 'clock.

< Table 11. Optical Table >

[VDD = 12.0V, Frame rate = 60Hz, Ta =25±2 ℃]

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle	Horizontal	Θ_3	CR > 10		89		Deg.	Note 1
		Θ_9			89		Deg.	
	Vertical	Θ_{12}			89		Deg.	
		Θ_6			89		Deg.	
Contrast ratio		CR	Θ = 0° (Center) Normal Viewing Angle	900:1	**1200:1**	-		Note 2
Reproduction of color	White	W_x		TYP. - 0.03	0.280	TYP. + 0.03		Note 3
		W_y			0.290			
	Red	R_x			0.641			
		R_y			0.339			
	Green	G_x			0.274			
		G_y			0.603			
	Blue	B_x			0.147			
		B_y			0.058			
Response Time	G to G	T_g		-	8	10	ms	Note 4
Gamma Scale				2.0	2.2	2.4		
Brightness				700	800		nit	
Color Temperature					10000		K	
Color Gamut					72		%	
Brightness Uniformity					75		%	9 point

Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of $\theta = 0°$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See Figure 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The color chromaticity coordinates specified in Table 9.shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel. The BLU is used by BOE.
4. Response time Tg is the average time required for display transition by switching the input signal as below table and is based on Frame rate fV =60Hz to optimize.
   Each time in below table is defined as Figure 2 and shall be measured by switching the

Measured Response Time		Target																
		0	15	31	47	63	79	95	111	127	143	159	175	191	207	223	239	255
Start	0																	
	15																	
	31																	
	47																	
	63																	
	79																	
	95																	
	111																	
	127																	
	143																	
	159																	
	175																	
	191																	
	207																	
	223																	
	239																	
	255																	

7.0 MECHANICAL CHARACTERISTICS

7.1 Dimensional Requirements

Figure 3(located in Appendix) shows mechanical outlines for the model DV550FHM-NV2. Other parameters are shown in Table 12.

< Table 12. Dimensional Parameters >

Parameter	Specification	Unit
Active area	1209.6 (H) ×680.4(V)	mm
Pixel pitch	0.630(H) ×0.210(V)	mm
Number of pixels	1920(H) ×1080(V) (1 pixel = R + G + B dots)	pixels
MDL Size	1213.7×684.5	mm
Thickness	59.39	mm
Weight	18760	gram

7.2 Semi-Glare and Polarizer Hardness

The surface of the LCD has an Anti-glare coating to minimize reflection and a coating to Reduce scratching.

8.0 RELIABILITY TEST

The Reliability test items and its conditions are shown in below.

< Table 13. Reliability Test Parameters >

No	Test Items	Conditions
1	High temperature storage test	Ta = 60 ℃, 240 hrs
2	Low temperature storage test	Ta = -20 ℃, 240 hrs
3	High temperature & high humidity operation test	Ta = 50 ℃, 80%RH, 240hrs
4	High temperature operation test	Ta = 50 ℃, 240hrs
5	Low temperature operation test	Ta = 0 ℃, 240hrs
6	Thermal shock	Ta = -20 ℃ ↔ 60 ℃ (0.5 hr), 100 cycle
7	Vibration test (non-operating)	Frequency : 10 ~ 300 Hz, Random Gravity / AMP : 1.0 Grms Period : X, Y, Z 30 min/axis
8	Shock test (non-operating)	Gravity : 50G Pulse width : 11msec, Sine wave ±X, ±Y, ±Z Once for each direction
9	Electro-static discharge test	Air : ±15kV ,150pF/330Ω ,100Point ,1time/Point Contact : ±8kV ,150pF/330Ω ,100Point ,1time/Point Non operation Contact: ±4KV~±6KV,150pF/330Ω,100Point, Input connector Pin, 3 times/pin with no function loss

9.0 PRODCUT SERIAL NUMBER

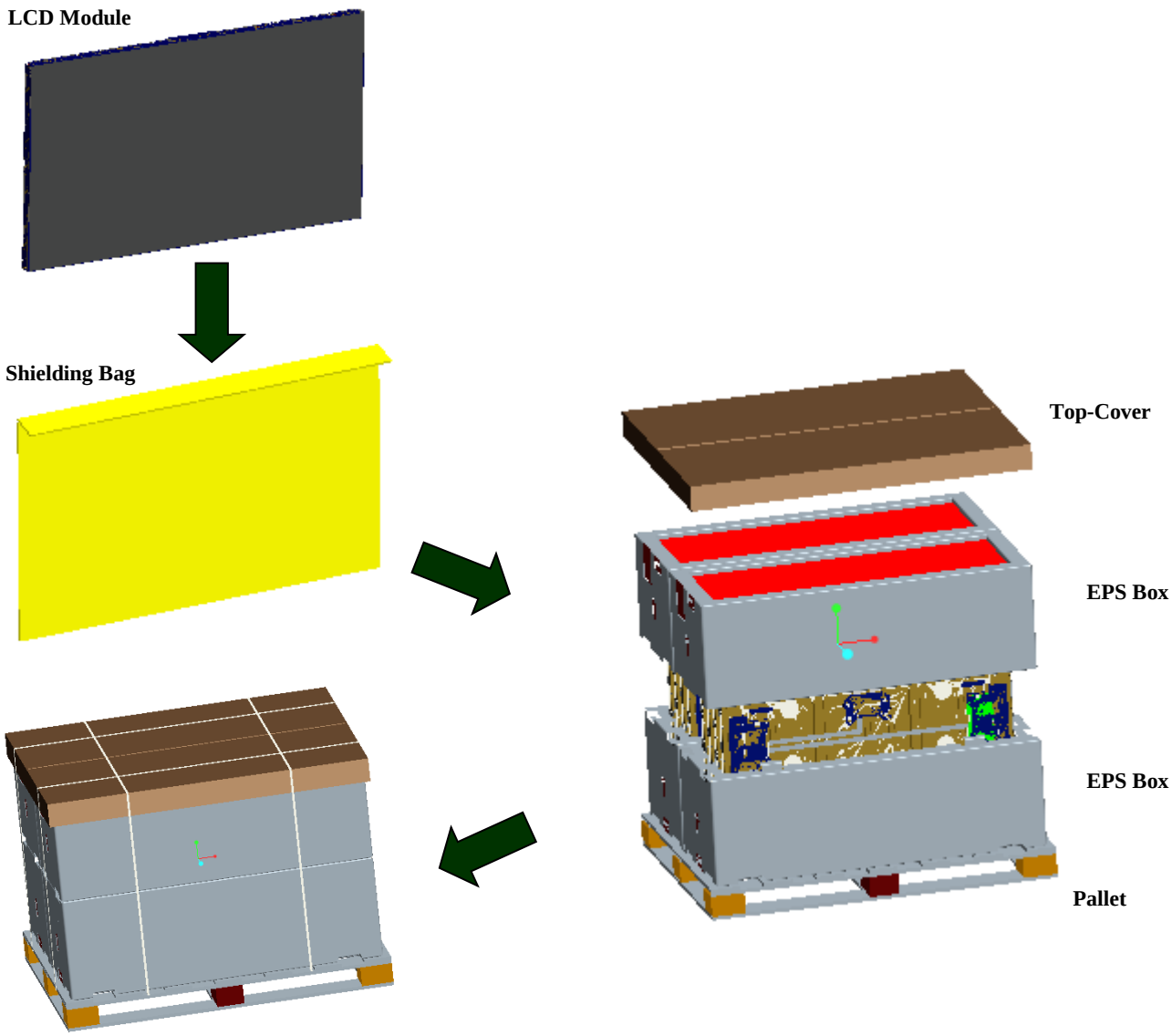
1	2	3	4	5	6	7
X X	X	X	X X	X	X X X X	X X X X X X

1. Control Number
2. Rank / Grade
3. Line Classification
4. Year (2011 : 11, 2012 : 12, …)
5. Month (1,2,3, … , 9, X, Y, Z)
6. Internal Use
7. Serial Number

10.0 PACKING INFORMATION

BOE provides the standard shipping container for customers, unless customer specifies their packing information. The standard packing method and Barcode information are shown in below.

10.1 Packing Order



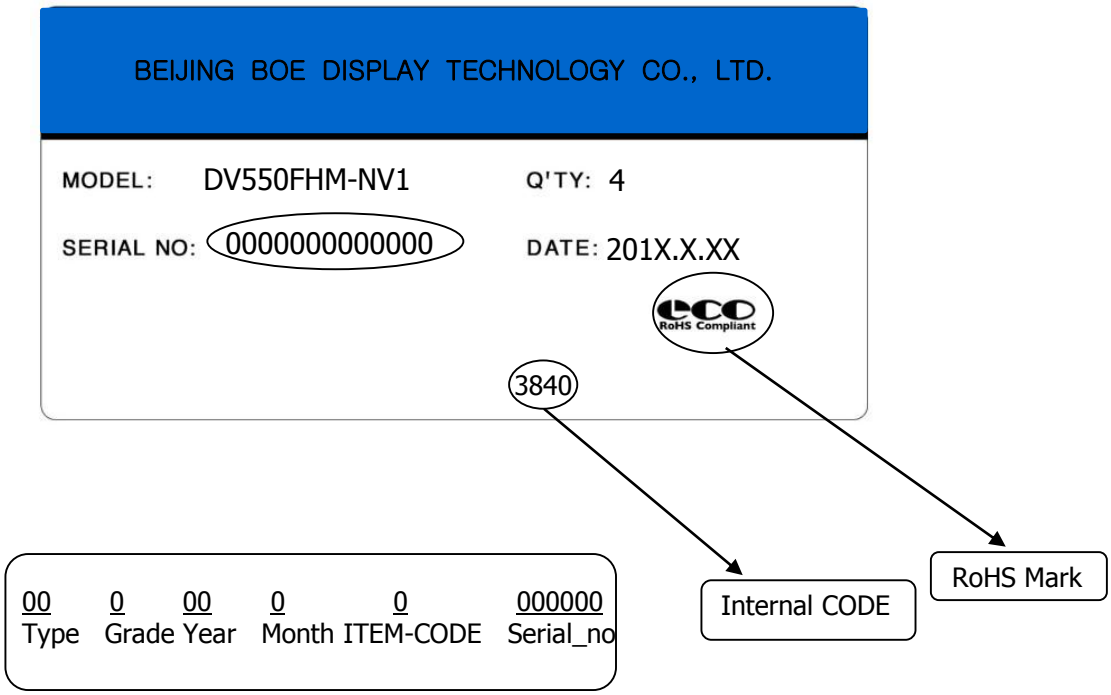
10.2 Packing Note

- Box Dimension : 1385 mm (L) × 545 mm (W) × 892.3 mm (H)
- Package Quantity in one Box : 4 pcs

10.3 Box Label

- Label Size : 110 mm (L) × 55 mm (W)
- Contents

  Model : DV550FHM-NV1
  Q`ty：Module 4 Q`ty in one box
  Serial No. : Box Serial No. See next page for detail description.
  Date : Packing Date
  FG Code : FG Code of Product



11.0 HANDLING & CAUTIONS

(1) Cautions when taking out the module
- Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module
- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation
- When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

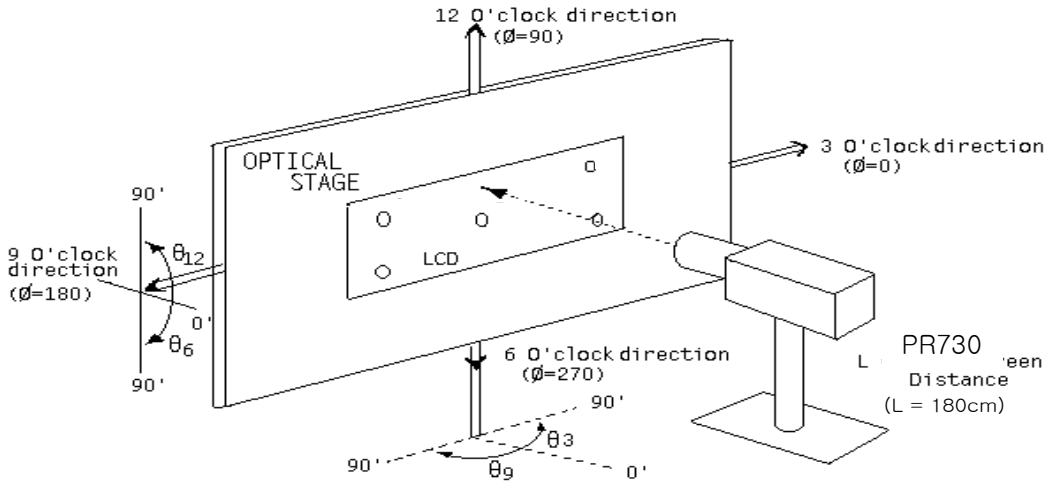
(4) Cautions for the atmosphere
- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics
- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions
- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc., Please pack the module not to be broken. We recommend to use the original shipping packages.

12.0 APPENDIX

< Figure 1. Measurement Set Up >



< Figure 2. Response Time Testing >

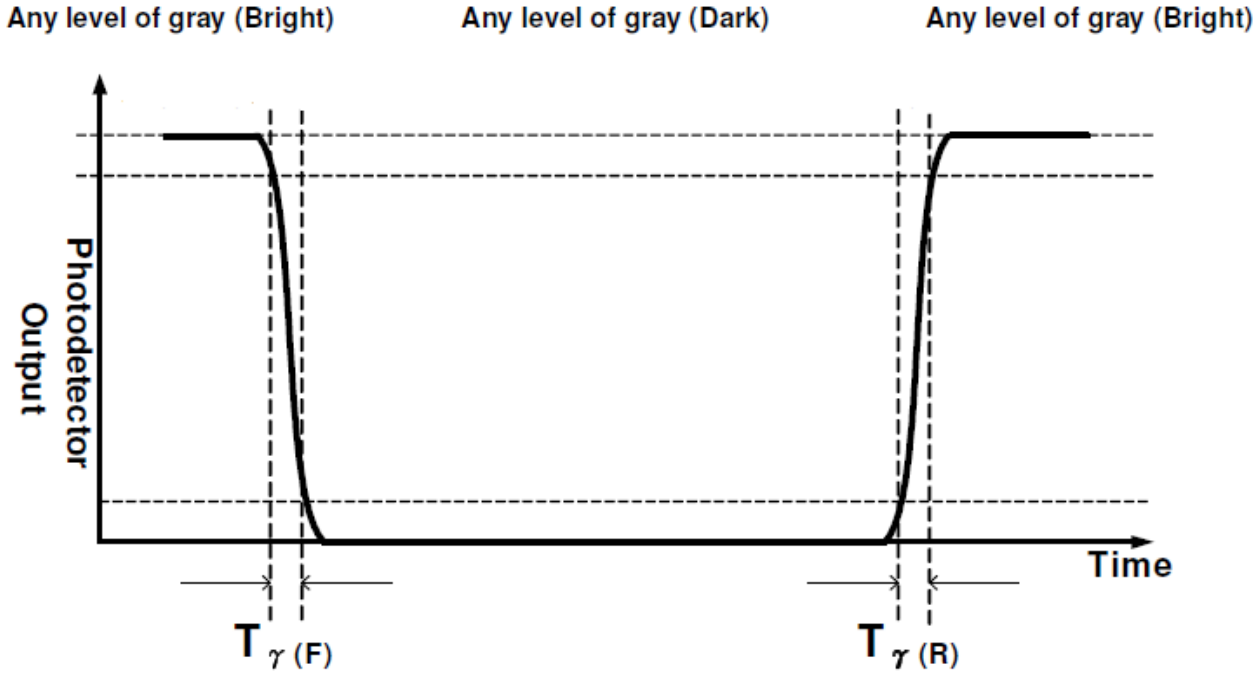
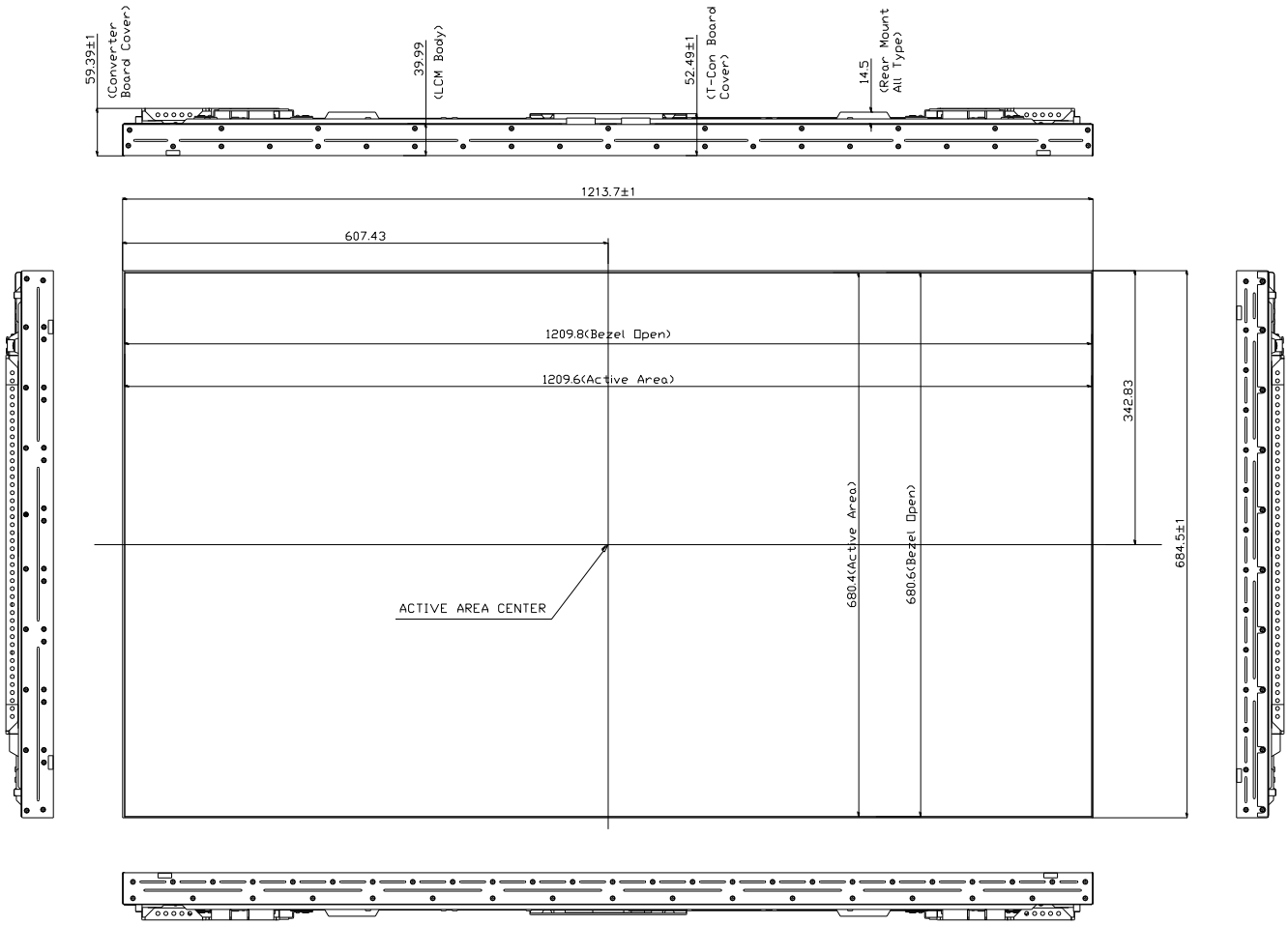
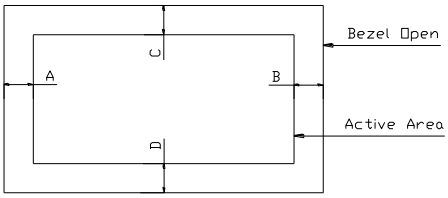
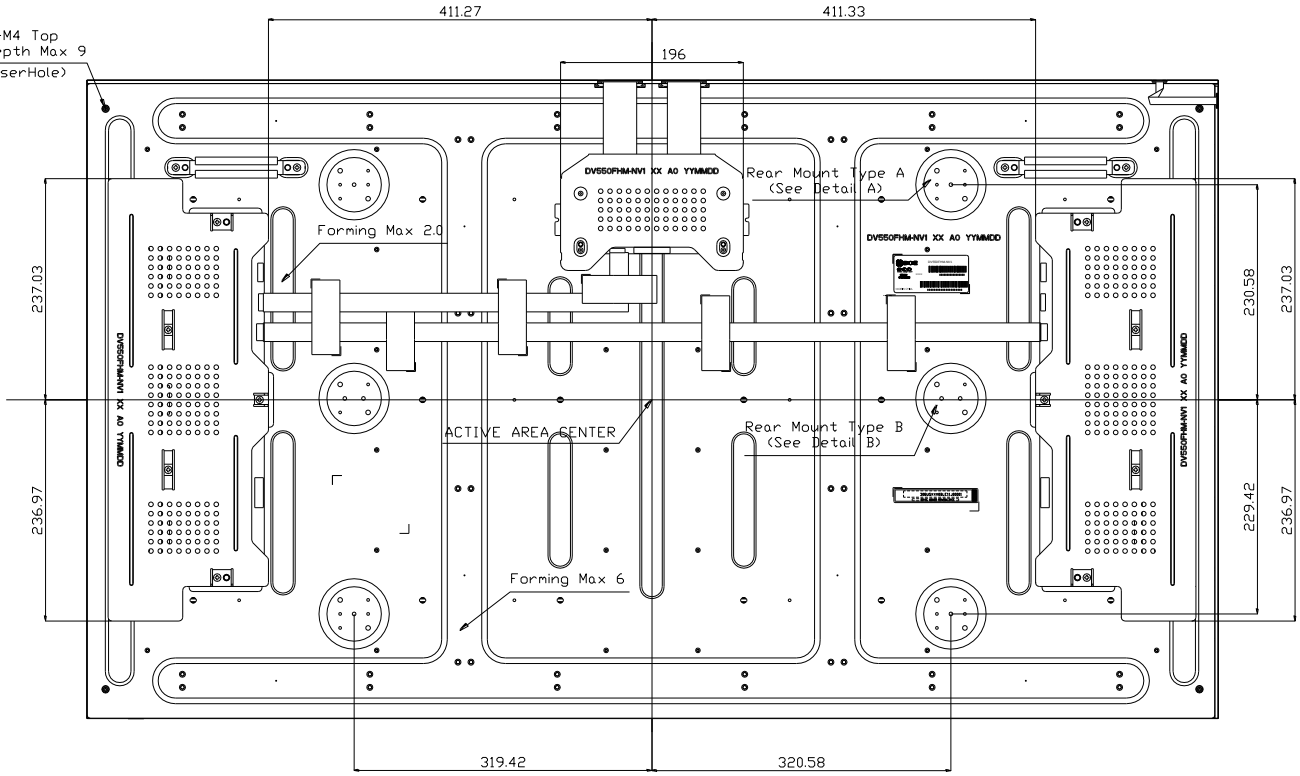


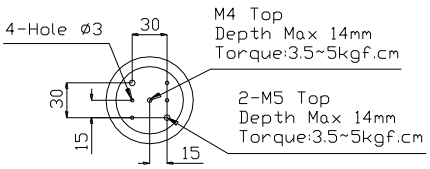
Figure 3. TFT-LCD Module Outline Dimensions (Front view)



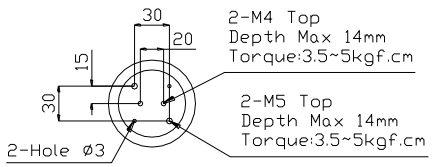


NOTES:
1.UNSPECIFIED DIMENSIONAL TOLERANCES TO BE ±0.5MM.
2.TILT AND A PARTIAL DISPOSITION TOLERANCE OF DISPLAY AREA ARE AS FOLLOW.
1)X-DIRECTION:IA-BI<2.0MM
2)Y-DIRECTION:IC-DI<2.0MM





Detail A



Detail B