DW9718S

- High efficiency driver IC for VCM

Ver. 1.7.1
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CONTENTS

1. General Description

The DW9718S has a single 10-bit DAC with 100mA output current sinking capability, which is designed for linear control of voice coil motors, capable of operating voltage up to 4.8V. The SAC(Smart Actuator Control) mode is applied to minimize mechanical vibrations automatically. The SAC mode highly improves the actuator's settling time and tolerance coverage compared with conventional LSC(Linear Slope Control) mode. The DW9718S is controlled via an I2C serial interface, the clock rates of which is up to 400 kHz.

The DW9718S has a POR(Power On Reset) circuit and power down mode. POR circuit gets to operate when VDD(supply power) turns on. The output current keeps 0mA until valid register value takes place. During the power down mode, it consumes max. 1uA.

The DW9718S is designed for auto focus and optical zoom for mobile cameras, digital still cameras, camcorders and other nano actuator applications.

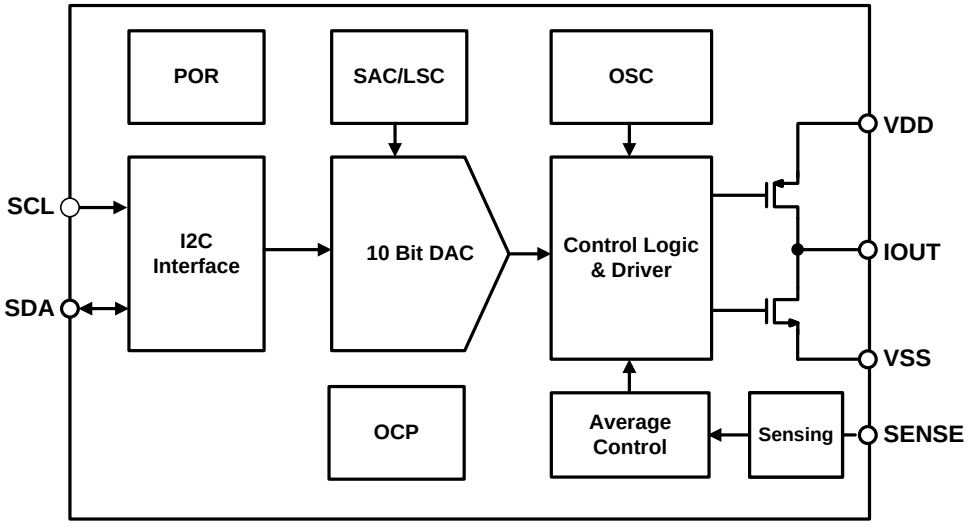
■ Features

VCM driver for auto-focus
High efficiency switching mode operation
10bit resolution current sinking of 100mA for VCM
SAC(Smart Actuator Control) mode, LSC(Linear Slope Control) mode
Supply voltage range(VDD): 2.3V to 4.8V(Linear Mode)
Fast mode I2C interface(1.8V interface available)
Power down mode
Power on reset(POR)
UVLO(Under Voltage Lockout), OCP(Over Current Protection)
Package: 6 pin WLCSP(0.73 X 1.13 X 0.31(mm))

■ Applications

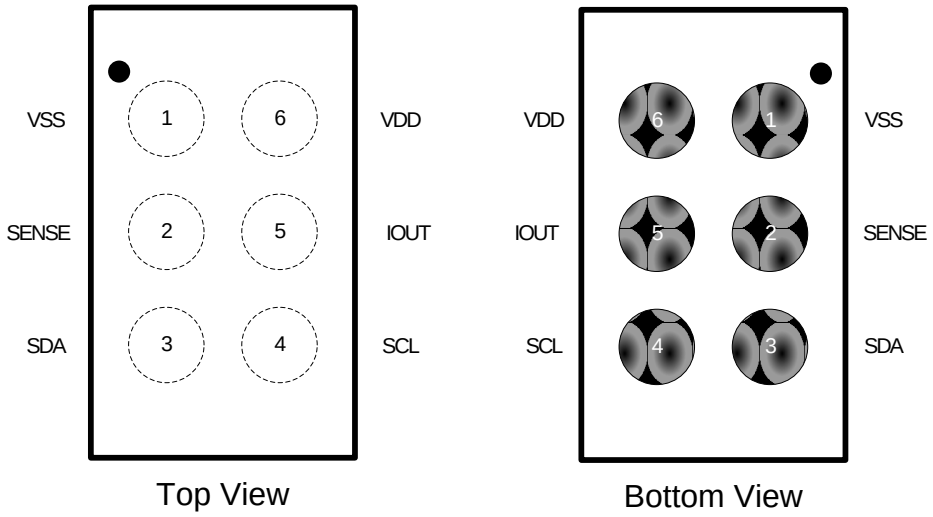
Mobile camera
Digital still camera
Camcorder
Web camera
Nano actuator

2. Block Diagram



3. Pin Information

■ Pin assignment and dimension



IC size : 0.73(W) X 1.13(L) X 0.31(T)mm
Pin pitch = 0.4mm(6 pin WLCSP)

■ Pin Description

No.	Pin Name	I/O	Description	Note
1	VSS	-	Ground	
2	SENSE	I	Output current sense	
3	SDA	I/O	I2C interface input/output (DATA)	
4	SCL	I	I2C interface input (CLOCK)	
5	IOUT	O	Output current source	
6	VDD	-	Power supply	

4. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
VDD	Power supply voltage	-0.3	5.5	V
Vin	Control input voltage	-0.3	VDD+0.3	V
Topr	Operating temperature range	-35	85	℃
Tj	Junction temperature		125	℃

■ Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range (Topr) may result in IC damage. The implementation of a physical safety measures such as a fuse should be considered when you use the IC in a special mode in which you anticipate the absolute maximum ratings may be exceeded.

5. Recommended Operating Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Power supply voltage(Linear Mode)	2.3		4.8	V
Vin	Control input voltage	0		VDD	V
SCL	I2C bus transmission rate			400	KHz

6. Electrical Specifications

(VDD=2. 8V, Vin=1.8V to VDD, Ta= 25℃, unless otherwise specified.)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Overall						
Supply Voltage	V_{DD}	Linear Mode	2.3		4.8	V
		PWM Mode	2.5		4.8	V
V_{DD} Current	I_{PD}	Power down mode	-1		+1	uA
	I_Q	Quiescent mode	0.5	1.5	2.0	mA
Logic Input / Output (SCL,SDA)						
Input Current		VDD&VIO=4.8V	-8		+8	uA
Low Level Input Voltage	V_{IL}				0.54	V
High Level Input Voltage	V_{IH}		1.26			V
Glitch rejection(1)					50	ns
SDA Low Level Output Voltage (open drain)	V_{OL}	Sink Current = 3mA			0.4	V
Hardware Reset Detection time	t_{HRST}	SCL & SDA = 0V			3	ms
Delay time for POR / PD(1)	t_{OPR}		100			us
Delay time for Mode change operation(1)	t_{MODE}		85			us
Over Current Protection						
Over Current Protection(1)	OCP			200		mA
Under Voltage Lockout						
Under Voltage Lockout	UVLO		1.8		2.45	V
AC Performance						
Switching frequency			0.588		5	MHz
Frequency tolerance(2)			-3		+3	%
Load Inductance			30		150	uH
VCM driver						
Current resolution(1)		97.65uA/LSB		10		Bits
INL (1)(3)	INL		-4		+4	LSB
DNL(1)(3)	DNL		-1		+1	LSB
Zero code error	ZCE	Zero data loaded to DAC	-1		+1	mA
Total Resistance value of the Output(1) (Sensing Resistor + Tr On Resistance)		Output Current = 100mA			2	Ω
Maximum output current	Imax		95	100	105	mA
Output current @ power down			-0.1		+0.1	uA

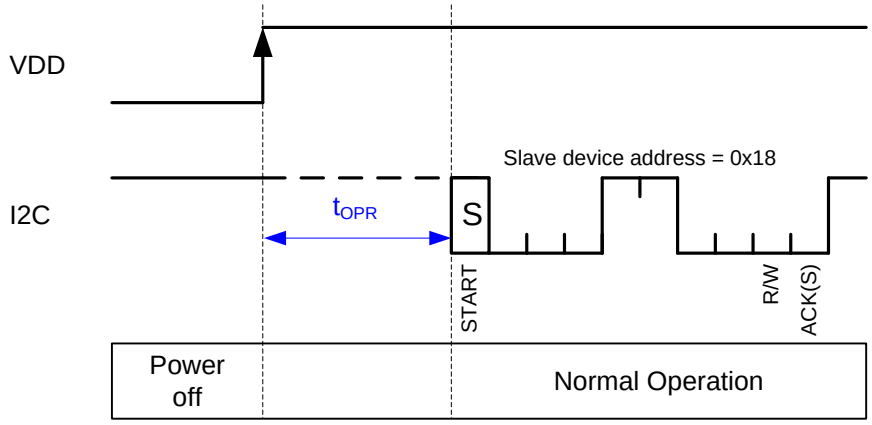
(1) These are guaranteed by design spec. and characterization.

(2) Test condition is 1Mhz at free-air temperature.

(3) Linearity is guaranteed for code 32 through code 992.

7. Power ON & Reset sequence

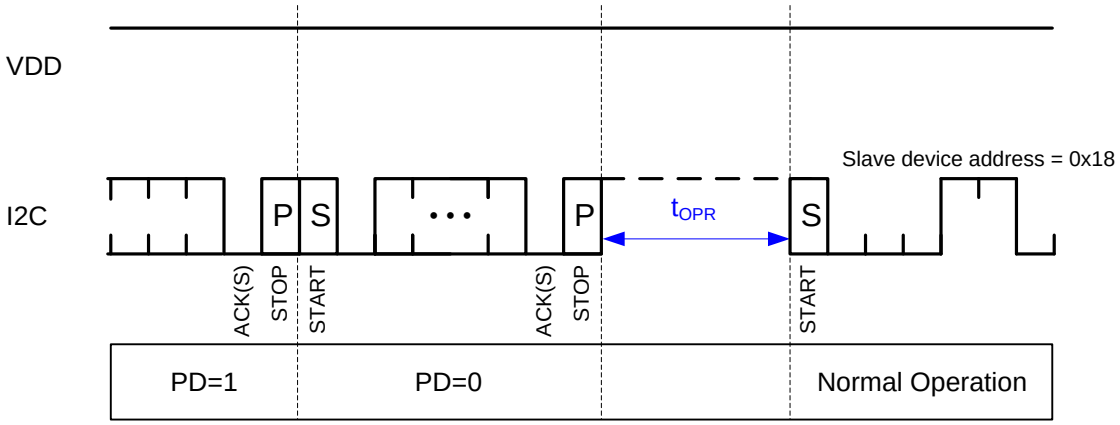
7.1. Power ON



※DW9718S requires waiting time of t_{OPR} after VDD rising.

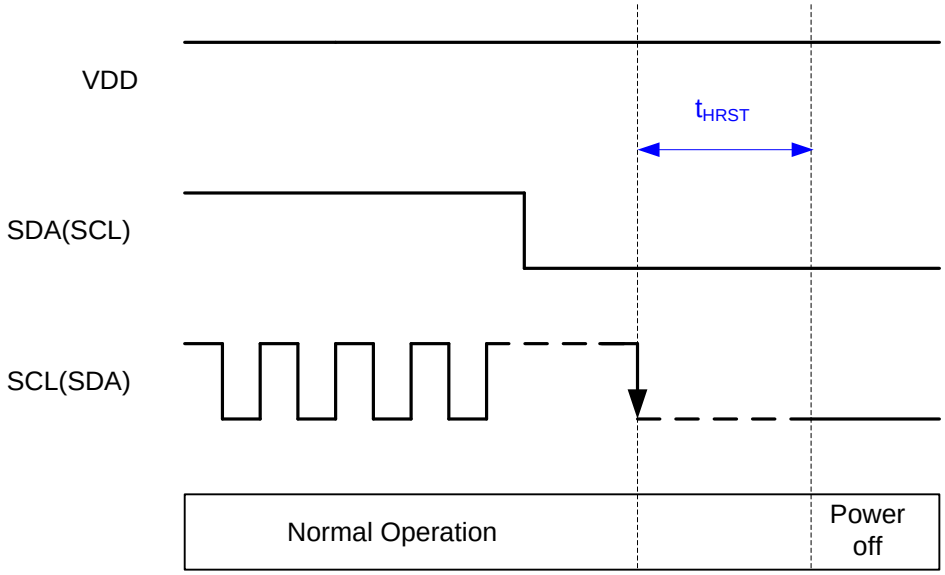
※If VDD rising time is more than 10ms, DW9718S could be unknown state. In this case, DW9718S has to input PD sequence.

7.2. PD(Power Down) sequence



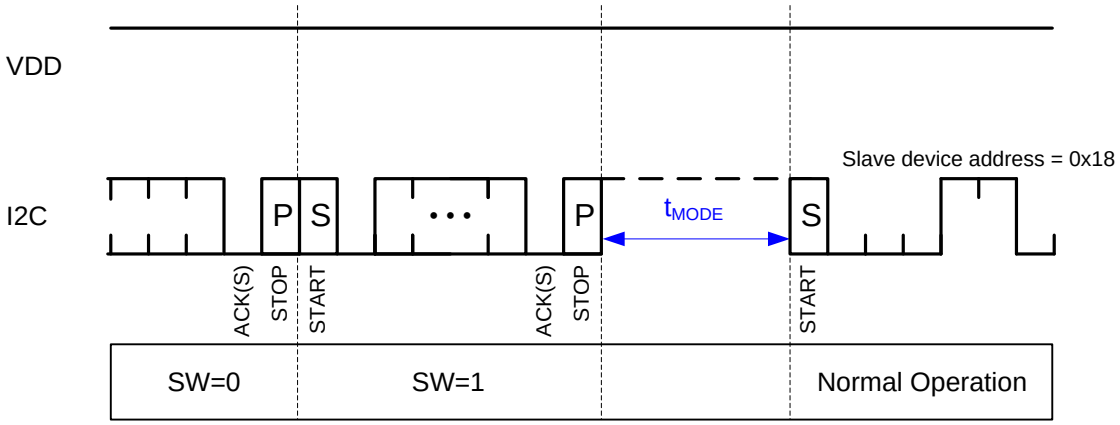
※ DW9718S requires waiting time(delay time) of t_{OPR} after PD reset takes place.

7.3. Hardware Reset



※ DW9718S turns into hardware reset mode when both SCL and SDA turn low and keep it during t_{HRST}.
※ Default value of hardware reset is disabled. It can be enabled by factory option.

8. Mode change

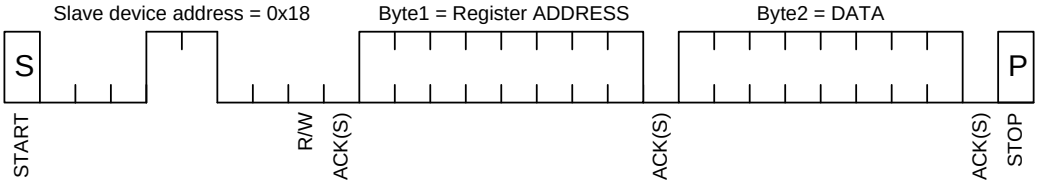


※ DW9718S requires waiting time(delay time) of t_{MODE} after mode change(Switching mode to Linear mode) takes place.

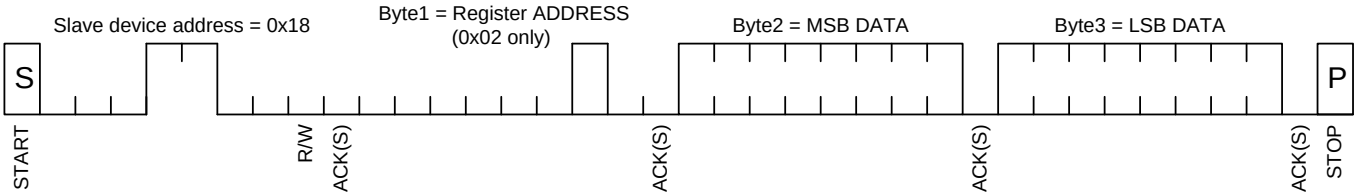
9. Register

9.1. I2C format

■ Write Operation − Byte Write

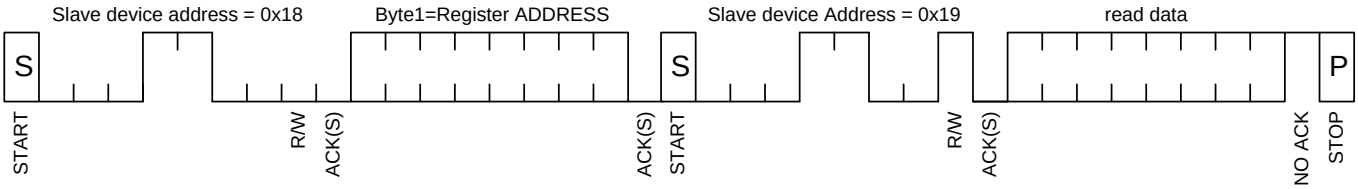


■ Write Operation − Sequential Write



* Sequential Write is available only for DATA_M registers(Address 0x02)

■ Read Operation − Selective Read



※ In I2C format, Master(ISP, AP etc.) must check the ACK bit before sending the next data.

9.2. Register table

NAME	Addr.	Default	R/W	Data							
PD	0x00	0x00	W								PD
CONTROL	0x01	0x00	R/W			UVLO _ENB	OCP _ENB	S2	S1	S0	SW
DATA_M	0x02	0x00	R/W							D9	D8
DATA_L	0x03	0x00	R/W	D7	D6	D5	D4	D3	D2	D1	D0
SW	0x04	0x00	R/W			DRV1	DRV0	SWF3	SWF2	SWF1	SWF0
SACT	0x05	0x60	R/W	DIV1	DIV0	SACT5	SACT4	SACT3	SACT2	SACT1	SACT0
FLAG	0x10	0x00	R						OCP _M	UVLO _M	FG

xxxxxx = Default value is "H"

9.3. Register description

NAME	Addr.	Default	R/W	Data							
PD	0x00	0x00	W								PD

PD

1: Power Down mode(active high)

0: Normal operation mode

※ DW9718S requires waiting time(delay time) of t_{OPR} after PD reset takes place

NAME	Addr.	Default	R/W	Data							
CONTROL	0x01	0x00	R/W			UVLO _ENB	OCP _ENB	S2	S1	S0	SW

UVLO_ENB

1: Under Voltage detection disabled

0: Under Voltage detection enabled(default)

OCP_ENB

1: Over Current detection disabled

0: Over Current detection enabled(default)

※ These options(UVLO, OCP) are just for one time use at the start up(POR / PD) to fix either enable or disable. They should be disabled below 2.5V.

S[2:0] : SAC(Smart Actuator Control) mode

S[2:0]	Mode
000	Direct mode
001	LSC mode
010	SAC1 mode
011	SAC2 mode
100	SAC3 mode
101	SAC4 mode
110	SAC5 mode
111	SAC6 mode

SW: Switching mode

1: Linear mode

0: Switching mode(default)

NAME	Addr.	Default	R/W	Data							
DATA_M	0x02	0x00	R/W							D9	D8
DATA_L	0x03	0x00	R/W	D7	D6	D5	D4	D3	D2	D1	D0

D [9:0]: DAC data input

Output current = (D[9:0]/1023) X 100mA

NAME	Addr.	Default	R/W	Data							
SW	0x04	0x00	R/W			DRV1	DRV0	SWF3	SWF2	SWF1	SWF0

DRV[1:0] : Soft Switching Option

00: Soft switching0 (fast slope, default)
01: Soft switching1
10: Soft switching2
11: Soft switching3 (slow slope)

SWF [3:0]: Switching frequency

SWF[3:0]	Frequency [MHz]	SWF[3:0]	Frequency [MHz]
0000	5.00	1000	1.00
0001	3.33	1001	0.91
0010	2.50	1010	0.83
0011	2.00	1011	0.77
0100	1.67	1100	0.71
0101	1.43	1101	0.67
0110	1.25	1110	0.63
0111	1.11	1111	0.59

NAME	Addr.	Default	R/W	Data							
SACT	0x05	0x60	R/W	DIV1	DIV0	SACT5	SACT4	SACT3	SACT2	SACT1	SACT0

DIV [1:0]: Step period divider(Pre-scaler) for LSC mode & SAC mode

DIV [1:0]	Period
00	T_{SAC} x 2 (double)
01	T_{SAC} x 1 (default)
10	T_{SAC} x 1/2 (half)
11	T_{SAC} x 1/4 (quarter)

SACT [5:0]: 1-Step period(T_{LSC}) for LSC mode
SAC period(T_{SAC}) for SAC mode

where, T_{LSC}(1-step period) = 126us + SACT[5:0] * 2us
T_{SAC}(SAC period) = 6.3ms + SACT[5:0] * 0.1ms

NAME	Addr.	Default	R/W	Data							
FLAG	0x10	0x00	R						OCP _M	UVLO _M	FG

OCP_M

1 : Over Current Lockout
0 : Normal

UVLO_M

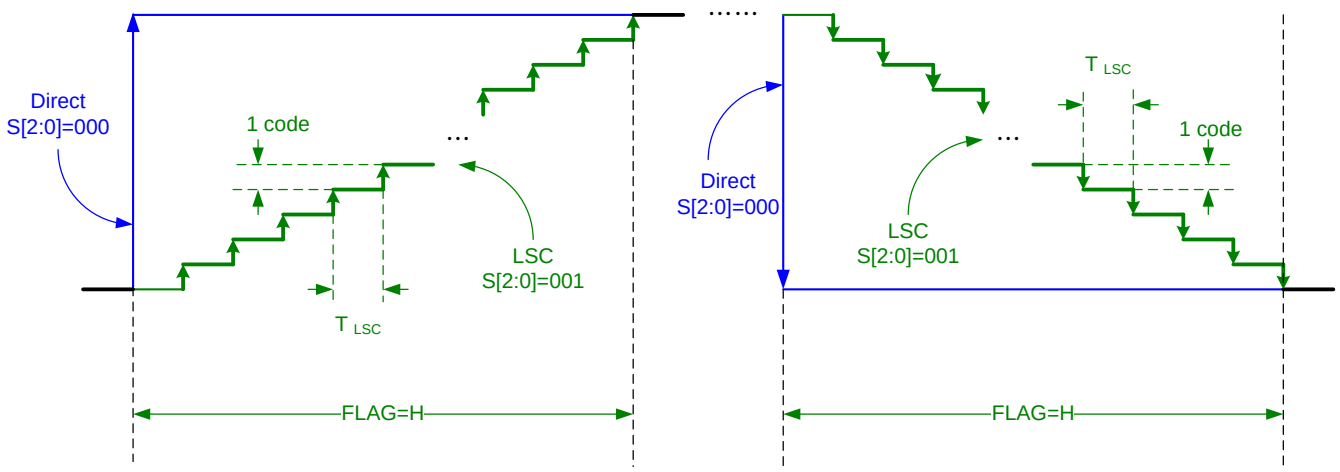
1 : Under Voltage Lockout
0 : Normal

FG

FG bit must be ”L” during ”DATA_ M and DATA_L” registers are being written.
During Ringing control operation, FG bit keeps ”H”. While FG=”H”**,** the I2C command is ignored.

10. Slew Rate Control Set up Method

10.1. Direct & LSC(Linear Slope Control) scheme



10.2. SAC(Smart Actuator Control) scheme

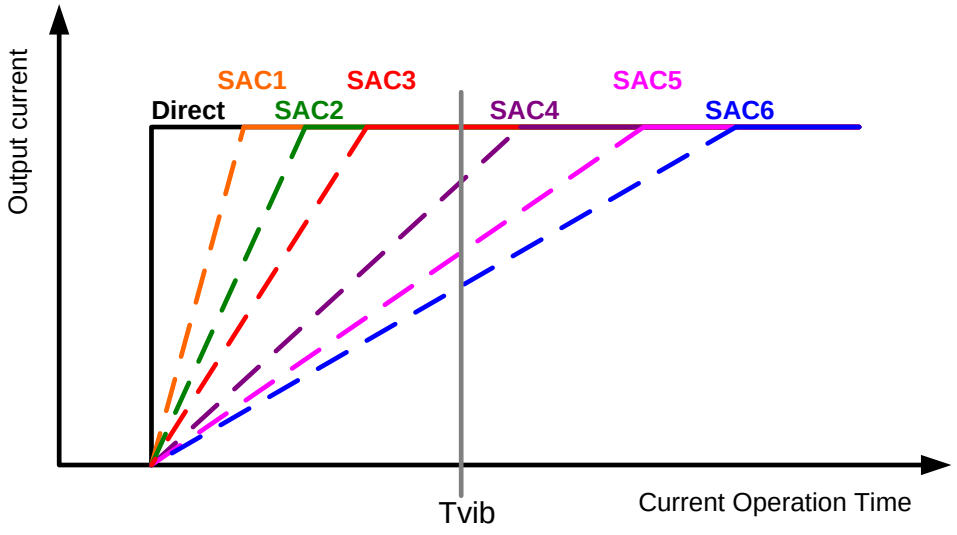
The SAC(Smart Actuator Control) mode is applied to minimize mechanical vibrations automatically.

S[2:0]	Mode	Current Operation time(1)	Actuator Tvib Tolerance Coverage(2)
010	SAC1	0.32*Tvib(3)	± 8 %
011	SAC2	0.48*Tvib(3)	± 9 %
100	SAC3	0.72*Tvib(3)	±19 %
101	SAC4	1.20*Tvib(3)	±37 %
110	SAC5	1.64*Tvib(3)	±43 %
111	SAC6	1.88*Tvib(3)	±63 %

(1) Operation time : Driver's current moving time

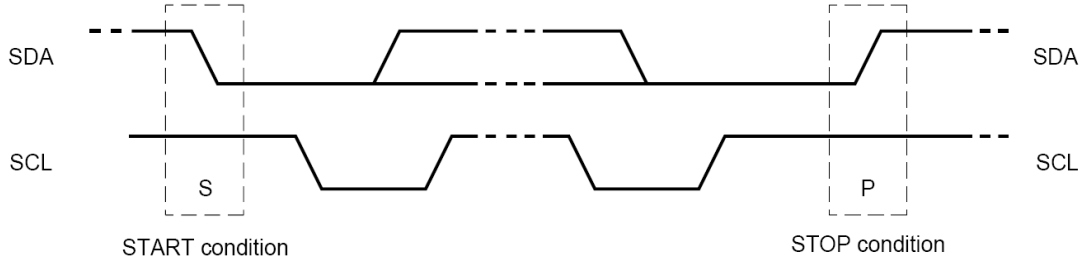
(2) This is a design spec. Tolerance coverage can be variable according to mechanical characteristics of each VCM

(3) Tvib = vibration period of VCM



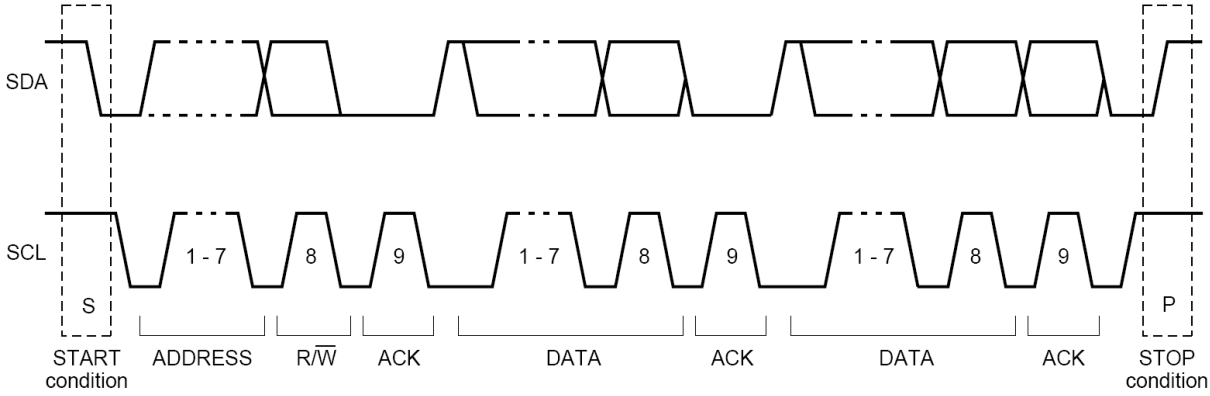
11. I2C Protocol

11.1. Start and Stop condition



Within the procedure of the I2C-bus, unique situations arise which are defined as START(S) and STOP(P) conditions. A HIGH to LOW transition on the SDA line while SCL is HIGH is one of such unique cases. This situation indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

11.2. Complete I2C Data Transfer

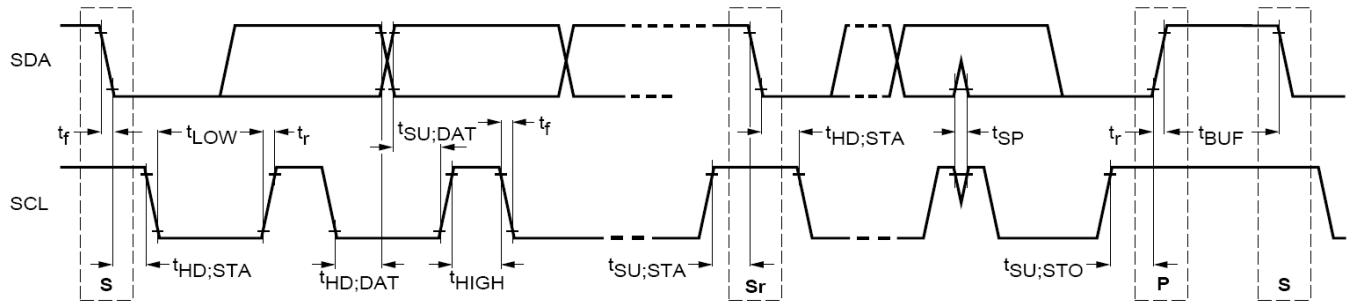


Data transfers follow the above format. After the START condition(S), a slave address is sent. A data transfer is always terminated by a STOP condition(P) generated by the master. However, if the master still needs to communicate on the bus, it can generate a repeated data transfer.

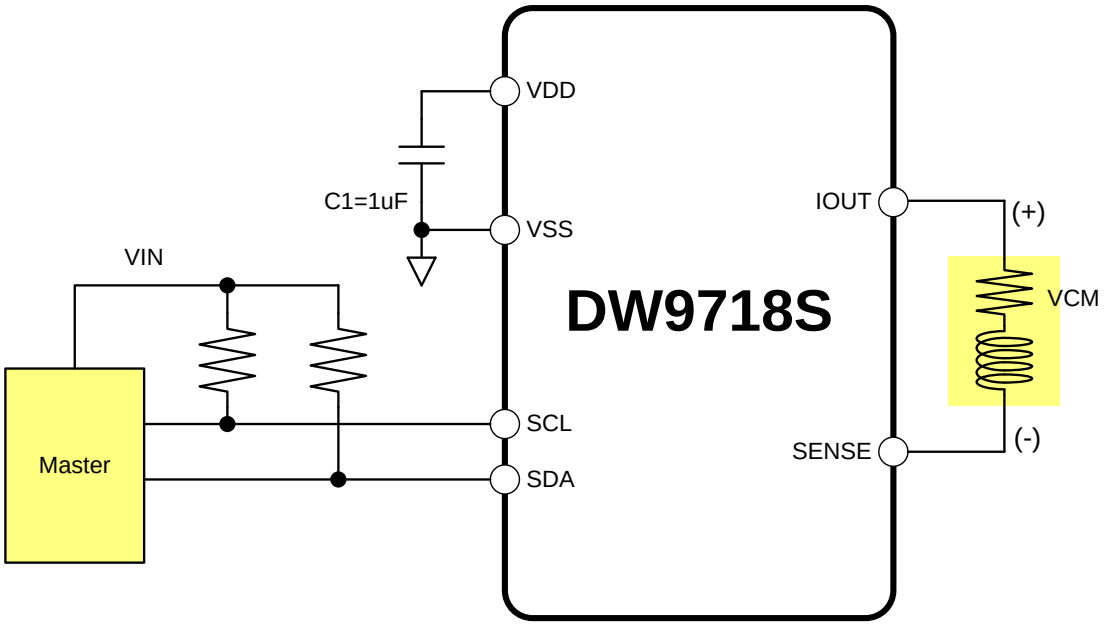
11.3. I2C timing

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	f_{SCL}	0	400	kHz
Hold time (repeated) START condition.	$t_{HD;STA}$	0.6	-	us
Low period of the SCL clock	t_{LOW}	1.3	-	us
High period of the SCL clock	t_{HIGH}	0.6	-	us
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	-	us
Data hold time	$t_{HD;DAT}$ (1)	-	0.9	us
Data set-up time	$t_{SU;DAT}$	100	-	ns
Rise time of both SDA and SCL signals	t_r	20+0.1C_b (2)	300	ns
Fall time of both SDA and SCL signals	t_f	20+0.1C_b (2)	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	0.6	-	us
Bus free time between a STOP and START condition	t_{BUF}	1.3	-	us
Capacitive load for each bus line	C_b	-	400	pF
Pulse width of spike suppress	t_{SP}	0	50	ns

(1) A master device must provide a hold time of at least 100ns for the SDA signal to bridge the undefined region of the falling edge of SCL. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
(2) C_b is the total capacitance of one bus line in pF, t_r and t_f are measured between 0.3V_{DD} and 0.7V_{DD}.



12. Typical Application Circuit



※ Power supply decoupling capacitor (C1) should be placed as close to the VDD and VSS as possible.

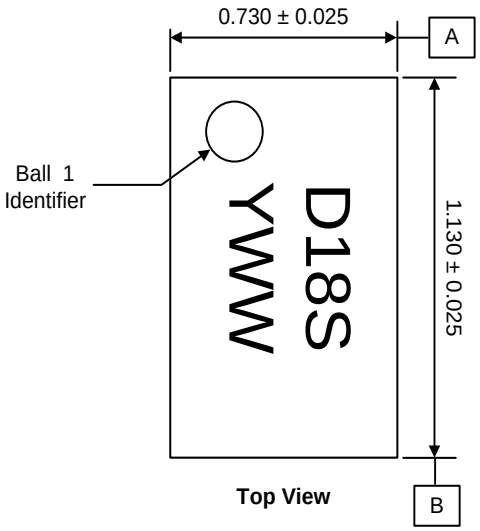
※ The value of C1 is recommended more than 1uF.

※ PCB pattern of VDD, GND, OUT and SENSE should be as short and wide as possible.

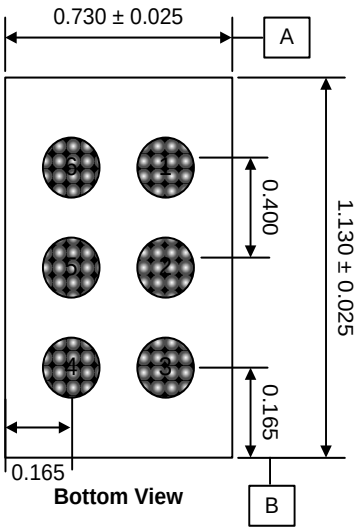
※ Refer to the Application Note of DW9718S for more information about **PCB Layout Guide for switching mode.**

13. Package Dimension (6 WLCSP, 0.73mm X 1.13mm X 0.31 mm)

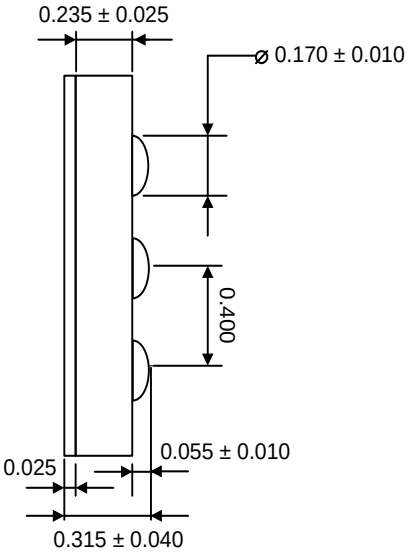
Unit : mm



Top View



Bottom View



Side View

NO	NAME	I/O
1	VSS	-
2	SENSE	I
3	SDA	I/O
4	SCL	I
5	IOUT	O
6	VDD	-