DZ80

8-bit Microprocessor

ver 1.00

OVERVIEW

Document contains brief description of DZ80 core functionality. The DZ80 is an advanced 8-bit microprocessor with 208 bits of user accessible registers, composed of six general purpose registers, able to be used individually as either 8-bit registers, or as 16-bit register pairs. Additionally to those registers, DZ80 supports two sets of accumulator and flag registers.
The DZ80 contains also Stack Pointer, program Counter, two index registers, a REFRESH register, and an INTERRUPT register. All output signals are fully decoded and timed to control standard memory or peripheral circuits. The DZ80 is supported by a wide range of peripherals family.

DZ80 is **fully customizable**, which means it is delivered in the exact configuration to meet users requirements. *There is no need to pay extra for not used features and wasted silicon.* It includes **fully automated testbench** with **complete set of tests** allowing easy package validation at each stage of SoC design flow.

CPU FEATURES

- Fully compatible with industry standard Z80
- Fully synthesizable, static synchronous design with no internal tri-states
- No internal reset generator or gated clock
- Scan test ready
- Technology independent HDL source code
- Core can be fully customized

DESIGN FEATURES

- ONE GLOBAL SYSTEM CLOCK
- SYNCHRONOUS RESET
- ALL ASYNCHRONOUS INPUT SIGNALS ARE SYNCHRONIZED BEFORE INTERNAL USE
- ALL LATHES IMPLEMENTED IN ORIGINAL Z80 MICROCONTROLLER ARE REPLACED BY EQUIVALENT FLI-FLOPS.

http://www.DigitalCoreDesign.com
http://www.dcd.pl

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
  - *Phone & email support*

LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

Single Design license allows use IP Core in single FPGA bitstream and ASIC implementation.

Unlimited Designs, *One Year* licenses allow use IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

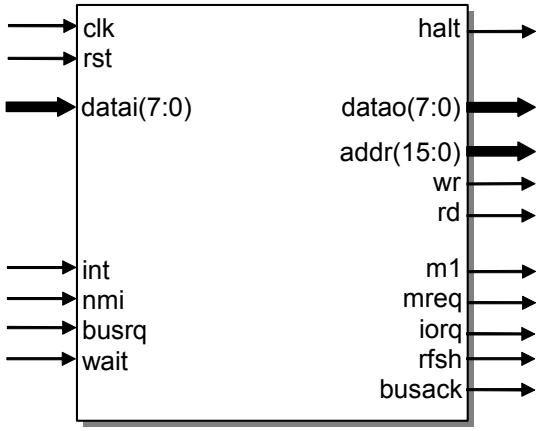
In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time restriction except *One Year* license where time of use is limited to 12 months.

- Single Design license for
  - *VHDL, Verilog source code called HDL Source*
  - *Encrypted, or plain text EDIF called Netlist*
- Unlimited Designs license for
  - *HDL Source*
  - *Netlist*
- Upgrade from
  - *HDL Source to Netlist*
  - *Single Design to Unlimited Designs*

PINS DESCRIPTION

PIN	ACTIVE	TYPE	DESCRIPTION
clk	-	input	Global system clock
rst	Low	input	Global reset input
int	Low	input	Interrupt request
nmi	Low	input	Non-Maskable Interrupt Request
wait	Low	input	WAIT input
busreq	Low	input	Bus Request
datai[7:0]	-	input	Memory bus input
datao[7:0]	-	output	Data memory & UFR bus output
addr[15:0]	-	output	Data memory address bus
wr	Low	output	Write enable
rd	Low	output	Read enable
busack	Low	output	Bus Acknowledge
m1	Low	output	Machine Cycle One
mreq	Low	output	Memory Request
iorq	Low	output	Input/Output Request
rfsh	Low	output	Refresh
halt	Low	output	Halt State

SYMBOL



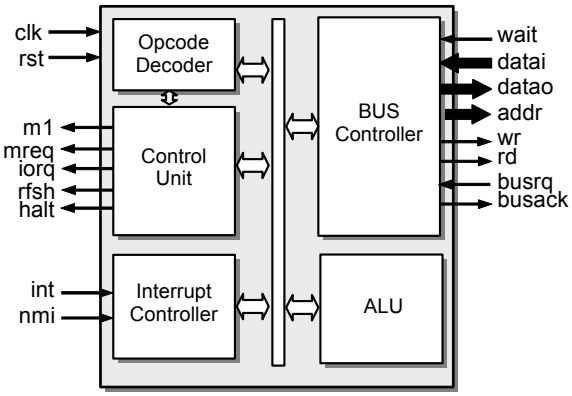
BLOCK DIAGRAM

Control Unit - Performs the core synchronization and data flow control. This module manages execution of all instructions. The Control Unit also manages execution of HALT state and waking-up the processor from the HALT mode.

Opcode Decoder - Performs an instruction opcode decoding and the control functions for all other blocks.

ALU - Arithmetic Logic Unit performs the arithmetic and logic operations during execution of an instruction. Contains accumulator CPU registers and related logic such as arithmetic and logic unit. ALU communicates with internal registers and the external data bus by using internal data bus. Functions performed by the ALU include:

- Addition
- Subtraction
- Logical AND
- Logical OR
- Logical Exclusive OR
- Compare
- Left or Right Shifts or Rotates
- Increment
- Decrement
- Set/Reset and Test Bit



Bus Controller –Data Memory & SFR's (Special Function Register) interface controls access into the program and data memories and special registers. It contains Program Counter (PC), Stack Pointer (SP) register, Index registers and related logic.

Interrupt Controller – manages execution of maskable and nonmaskable interrupts. It contains a Interrupt Enable register. Interrupt controller is responsible for the special M1 Cycle generation and wait states implementation during interrupt service.

CONTACTS

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