EPSON

E0C6282

4-bit Single Chip Microcomputer

Wide Voltage Operation Products

- Core CPU Architecture
- SVD Circuit/Comparator
- Melody Circuit
- 288 Segments for LCD

■ DESCRIPTION

The E0C6282 is an advanced single-chip CMOS 4-bit microcomputer consisting of the E0C6200A CMOS 4-bit core CPU. It also contains the ROM, RAM, LCD driver circuit, time base counter, stopwatch counter and melody generation circuit.
The E0C6282 provides an excellent solution for low-power consumption systems with clock functions.

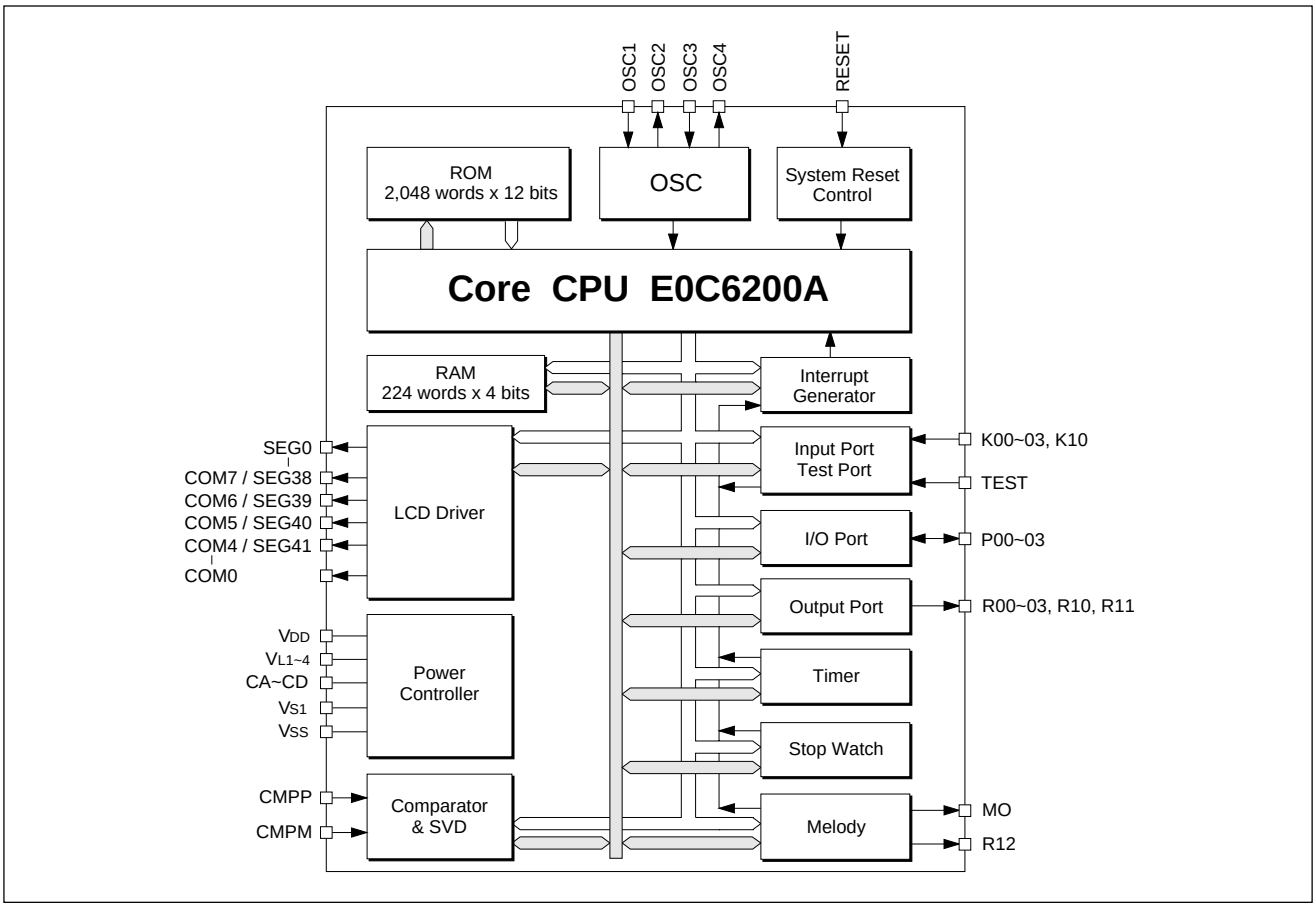
■ FEATURES

- CMOS LSI ..... 4-bit parallel processing
- Clock 32.768kHz/1MHz
- Instruction set ..... 100 instructions
- Instruction cycle time ..... 153µsec, 214µsec or 366µsec at 32kHz (depending on instruction)
  5µsec, 7µsec or 12µsec at 1MHz (depending on instruction)
- ROM capacity ..... 2,048 × 12 bits
- RAM capacity ..... 224 × 4 bits (include segment memory)
- Input port ..... 5 bits (pull-down resistors are available by mask option)
- Output port ..... 5 bits (general purpose port)
  2 bits (for melody output): MO, $\overline{MO}$ (also used as the external CR connecting terminal for envelope)
  1 bit (for clock output: frequency can be selected from 256Hz through 32kHz by mask option)
- Built-in stopwatch timer
- Built-in analog comparator
- I/O port ..... 4 bits
- LCD driver ..... 42 segments × 4 commons/38 segments × 8 commons
  (1/4 or 1/8 duty is selectable by mask option)
- Built-in supply voltage detection (SVD) circuit
- Built-in melody generation circuit ..... Melody memory capacity : 128 words
  Interval memory capacity : 32 words (including one pause note)
- Interrupts ..... External : Input interrupt 2 lines
  Internal : Timer interrupt 2 lines
  Melody completion interrupt 1 line
- Current consumption E0C6282/62L82
  HALT mode (32.768kHz) : 1.5µA (Typ.)
  OPERATING mode (32.768kHz) : 4.0µA (Typ.)
  E0C62A82
  OPERATING mode (1MHz) : 150µA (Typ.)
- Package ..... QFP5-80pin (plastic), QFP14-80pin (plastic)
  Die form

■ LINE UP

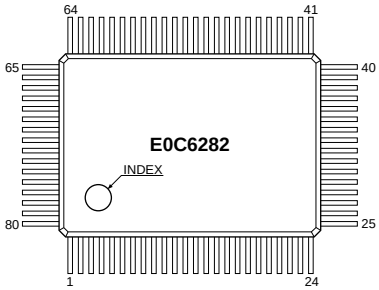
Model	Supply voltage	Clock
E0C62L82	1.5V (1.1V to 3.5V)	32kHz (Crystal or CR oscillation)
E0C6282	3.0V (2.2V to 5.5V)	32kHz (Crystal or CR oscillation)
E0C62A82	3.0V (2.2V to 5.5V)	32kHz (Crystal or CR oscillation) & 1MHz (Ceramic or CR oscillation)

■ BLOCK DIAGRAM



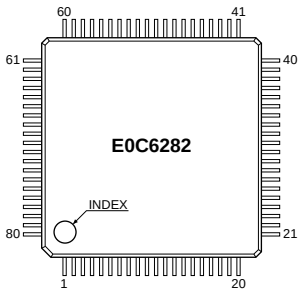
■ PIN CONFIGURATION

QFP5-80pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	V_{DD}	17	SEG14	33	K02	49	SEG28	65	P01
2	TEST	18	SEG15	34	K01	50	SEG29	66	P00
3	SEG0	19	SEG16	35	K00	51	SEG30	67	CD
4	SEG1	20	SEG17	36	RESET	52	SEG31	68	CC
5	SEG2	21	SEG18	37	CMPP	53	SEG32	69	CB
6	SEG3	22	SEG19	38	CMPM	54	SEG33	70	CA
7	SEG4	23	R03	39	COM3	55	SEG34	71	V_{L4}
8	SEG5	24	R02	40	COM2	56	SEG35	72	V_{L3}
9	SEG6	25	R01	41	COM1	57	SEG36	73	V_{L2}
10	SEG7	26	R00	42	COM0	58	SEG37	74	V_{L1}
11	SEG8	27	MO	43	SEG22	59	SEG38/COM7	75	V_{SS}
12	SEG9	28	R12	44	SEG23	60	SEG39/COM6	76	OSC4
13	SEG10	29	R11	45	SEG24	61	SEG40/COM5	77	OSC3
14	SEG11	30	R10	46	SEG25	62	SEG41/COM4	78	V_{S1}
15	SEG12	31	K10	47	SEG26	63	P03	79	OSC2
16	SEG13	32	K03	48	SEG27	64	P02	80	OSC1

QFP14-80pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	SEG0	17	SEG16	33	K00	49	SEG30	65	CD
2	SEG1	18	SEG17	34	RESET	50	SEG31	66	CC
3	SEG2	19	SEG18	35	CMPP	51	SEG32	67	CB
4	SEG3	20	SEG19	36	CMPM	52	SEG33	68	CA
5	SEG4	21	R03	37	COM3	53	SEG34	69	V_{L4}
6	SEG5	22	R02	38	COM2	54	SEG35	70	V_{L3}
7	SEG6	23	R01	39	COM1	55	SEG36	71	V_{L2}
8	SEG7	24	R00	40	COM0	56	SEG37	72	V_{L1}
9	SEG8	25	MO	41	SEG22	57	SEG38/COM7	73	V_{SS}
10	SEG9	26	R12	42	SEG23	58	SEG39/COM6	74	OSC4
11	SEG10	27	R11	43	SEG24	59	SEG40/COM5	75	OSC3
12	SEG11	28	R10	44	SEG25	60	SEG41/COM4	76	V_{S1}
13	SEG12	29	K10	45	SEG26	61	P03	77	OSC2
14	SEG13	30	K03	46	SEG27	62	P02	78	OSC1
15	SEG14	31	K02	47	SEG28	63	P01	79	V_{DD}
16	SEG15	32	K01	48	SEG29	64	P00	80	TEST

■ PIN DESCRIPTION

Pin name	Pin No.		In/Out	Function
	QFP5-80pin	QFP14-80pin		
V_{DD}	1	79	I	Power source (+) terminal
V_{SS}	75	73	I	Power source (-) terminal
V_{S1}	78	76	–	Oscillation and internal logic system regulated voltage output terminal
V_{L1}–V_{L4}	71–74	69–72	–	LCD system power source terminal
CA–CD	67–70	65–68	–	LCD system booster capacitor connecting terminal
OSC1	80	78	I	Crystal or CR oscillation input terminal
OSC2	79	77	O	Crystal or CR oscillation output terminal
OSC3	77	75	I	Ceramic or CR oscillation input terminal (62A82 only)
OSC4	76	74	O	Ceramic or CR oscillation output terminal (62A82 only)
K00–K00, K10	32–35, 31	30–33, 29	I	Input terminal
P00–P03	63–66	61–64	I/O	I/O terminal
R00–R03	23–26	21–24	O	Output terminal
R10	30	28	O	Output terminal (FOUT output available by mask option)
R11	29	27	O	Output terminal
R12	28	26	O	Output terminal (Melody inverted output and envelope function available by mask option)
MO	27	25	O	Melody signal output terminal
CMPP	37	35	I	Analog comparator non-inverted input terminal
CMPM	38	36	I	Analog comparator inverted input terminal
SEG0–37	3–22, 43–58	1–20, 41–56	O	LCD segment output terminal (Convertible to DC output by mask option) SEG20 and 21 may be used only when the chip has been supplied
COM0–3	39–42	37–40	O	LCD common output terminal
SEG38–41	59–62	57–60	O	LCD segment output terminal when 1/4 duty is selected
COM4–7				LCD common output terminal when 1/8 duty is selected
RESET	36	34	I	Initial reset input terminal
TEST	2	80	I	Test input terminal

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{SS}	-6.0 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1} - 0.3 to 0.5	V
Permissible total output current *1	ΣI_{VSS}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

∗1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
∗2: In case of plastic package (QFP5-80pin, QFP14-80pin).

● Recommended Operating Conditions

E0C6282

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-5.5	-3.0	-2.2	V
Oscillation frequency	f_{OSC1}		–	32.768	–	kHz

E0C62L82

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-3.5	-1.5	-1.1	V
		V_{DD}=0V, With software control *1	-3.5	-1.5	-0.9 *2	V
		V_{DD}=0V, When the analog comparator is used	-3.5	-1.5	-1.3	V
Oscillation frequency	f_{OSC1}		–	32.768	–	kHz

∗1: When switching to heavy load protection mode. The SVD circuit and analog voltage comparator are turned OFF.
∗2: The possibility of LCD panel display differs depending on the characteristics of the LCD panel.

E0C62A82

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-5.5	-3.0	-2.2	V
Oscillation frequency (1)	f_{OSC1}		–	32.768	–	kHz
Oscillation frequency (2)	f_{OSC3}	duty 50±5%	–	1,000	–	kHz

● DC Characteristics

E0C6282/62A82

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L4} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–K03, K10, P00–P03	0.2•V_{SS}		0	V
High level input voltage (2)	V_{IH2}		RESET, TEST	0.10•V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–K03, K10, P00–P03	V_{SS}		0.8•V_{SS}	V
Low level input voltage (2)	V_{IL2}		RESET, TEST	V_{SS}		0.90•V_{SS}	V
High level input current (1)	I_{IH1}	V_{IH1}=0V No pull down resistor	K00–K03, K10, P00–P03 CMPP, CMPM	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V With pull down resistor	K00–K03, K10	5		16	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V With pull down resistor	P00–P03 RESET, TEST	30		100	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–K03, K10, P00–P03 CMPP, CMPM RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1•V_{SS}	R11			-1.0	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.1•V_{SS}	R00–R03, R10, P00–P03			-1.0	mA
High level output current (3)	I_{OH3}	V_{OH3}=0.1•V_{SS}	MO, R12			-2.0	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9•V_{SS}	R11	3.0			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9•V_{SS}	R00–R03, R10, P00–P03	3.0			mA
Low level output current (3)	I_{OL3}	V_{OL3}=0.9•V_{SS}	MO, R12	4.5			mA
Common output current	I_{OH4}	V_{OH4}=-0.05V	COM0–COM3			-3	µA
1/4 duty	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current	I_{OH5}	V_{OH5}=-0.05V	SEG0–SEG41			-3	µA
(during LCD output)1/4 duty	I_{OL5}	V_{OL5}=V_{L3}+0.05V		3			µA
Segment output current	I_{OH6}	V_{OH6}=0.1•V_{SS}	SEG0–SEG41			-300	µA
(during DC output) 1/4 duty	I_{OL6}	V_{OL6}=0.9•V_{SS}		300			µA
Common output current	I_{OH7}	V_{OH7}=-0.05V	COM0–COM7			-3	µA
1/8 duty	I_{OL7}	V_{OL7}=V_{L4}+0.05V		3			µA
Segment output current	I_{OH8}	V_{OH8}=-0.05V	SEG0–SEG37			-3	µA
(during LCD output)1/8 duty	I_{OL8}	V_{OL8}=V_{L4}+0.05V		3			µA
Segment output current	I_{OH9}	V_{OH9}=0.1•V_{SS}	SEG0–SEG37			-300	µA
(during DC output) 1/8 duty	I_{OL9}	V_{OL9}=0.9•V_{SS}		300			µA

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(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L4} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–K03, K10, P00–P03	0.2•V_{SS}		0	V
High level input voltage (2)	V_{IH2}		RESET, TEST	0.10•V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–K03, K10, P00–P03	V_{SS}		0.8•V_{SS}	V
Low level input voltage (2)	V_{IL2}		RESET, TEST	V_{SS}		0.90•V_{SS}	V
High level input current (1)	I_{IH1}	V_{IH1}=0V No pull down resistor	K00–K03, K10, P00–P03 CMPP, CMPM	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V With pull down resistor	K00–K03, K10	2.0		10	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V With pull down resistor	P00–P03 RESET, TEST	9.0		60	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–K03, K10, P00–P03 CMPP, CMPM RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1•V_{SS}	R11			-450	µA
High level output current (2)	I_{OH2}	V_{OH2}=0.1•V_{SS}	R00–R03, R10, P00–P03			-200	µA
High level output current (3)	I_{OH3}	V_{OH3}=0.1•V_{SS}	MO, R12			-0.8	mA
High level output current (4)	I_{OH4}	V_{OH4}=0.1•V_{SS} When envelope is used	MO (R12=Normal H level)			-0.4	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9•V_{SS}	R11	1,300			µA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9•V_{SS}	R00–R03, R10, P00–P03	700			µA
Low level output current (3)	I_{OL3}	V_{OL3}=0.9•V_{SS}	MO, R12	1.5			mA
Low level output current (4)	I_{OL4}	V_{OL4}=0.9•V_{SS} When envelope is used	MO (R12=Normal L level)	750			µA
Common output current	I_{OH5}	V_{OH5}=-0.05V	COM0–COM3			-3	µA
1/4 duty	I_{OL5}	V_{OL5}=V_{L3}+0.05V		3			µA
Segment output current	I_{OH6}	V_{OH6}=-0.05V	SEG0–SEG41			-3	µA
(during LCD output)1/4 duty	I_{OL6}	V_{OL6}=V_{L3}+0.05V		3			µA
Segment output current	I_{OH7}	V_{OH7}=0.1•V_{SS}	SEG0–SEG41			-100	µA
(during DC output) 1/4 duty	I_{OL7}	V_{OL7}=0.9•V_{SS}		130			µA
Common output current	I_{OH8}	V_{OH8}=-0.05V	COM0–COM7			-3	µA
1/8 duty	I_{OL8}	V_{OL8}=V_{L4}+0.05V		3			µA
Segment output current	I_{OH9}	V_{OH9}=-0.05V	SEG0–SEG37			-3	µA
(during LCD output)1/8 duty	I_{OL9}	V_{OL9}=V_{L4}+0.05V		3			µA
Segment output current	I_{OH10}	V_{OH10}=0.1•V_{SS}	SEG0–SEG37			-100	µA
(during DC output) 1/8 duty	I_{OL10}	V_{OL10}=0.9•V_{SS}		130			µA

● Analog Circuit Characteristics and Current Consumption

E0C6282 (Normal Operating Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L4} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		0.5•V_{L2} -0.1		0.5•V_{L2} +0.1	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		-2.25	-2.10	-1.95	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
	V_{L4}	Connect 1MΩ load resistor between V_{DD} and V_{L4} (without panel load)		4•V_{L1} -0.1		4•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (CMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (CMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{CMP}	V_{IP}=-1.5V, V_{IM}=V_{IP}±15mV				1	mS
Current consumption	I_{OP1}	During HALT *1	Without panel load		1.5	3.0	µA
		During operation *1	OSC1 is crystal oscillation		4.0	7.0	µA
	I_{OP2}	During HALT *1	Without panel load		6.0	10.5	µA
		During operation *1	OSC1 is CR oscillation		8.7	14.0	µA

*1: The SVD circuit and analog voltage comparator are turned OFF.

E0C6282 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L4} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		0.5•V_{L2} -0.1		0.5•V_{L2} +0.1	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		-2.25	-2.10	-1.95	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
	V_{L4}	Connect 1MΩ load resistor between V_{DD} and V_{L4} (without panel load)		4•V_{L1} -0.1		4•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (CMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (CMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{CMP}	V_{IP}=-1.5V, V_{IM}=V_{IP}±15mV				1	mS
Current consumption	I_{OP1}	During HALT *1	Without panel load		11.5	33.0	µA
		During operation *1	OSC1 is crystal oscillation		14.0	37.0	µA
	I_{OP2}	During HALT *1	Without panel load		16.0	40.5	µA
		During operation *1	OSC1 is CR oscillation		18.7	44.0	µA

*1: The SVD circuit and analog voltage comparator are turned OFF.

E0C62L82 (Normal Operating Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L4} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
	V_{L4}	Connect 1MΩ load resistor between V_{DD} and V_{L4} (without panel load)		4•V_{L1} -0.1		4•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (CMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (CMPM)					
Analog comparator offset voltage	V_{OF}					20	mV
Analog comparator response time	t_{CMP}	V_{IP}=-1.1V, V_{IM}=V_{IP}±30mV				1	mS
Current consumption	I_{OP1}	During HALT *1	Without panel load		1.5	3.0	µA
		During operation *1	OSC1 is crystal oscillation		4.0	7.0	µA
	I_{OP2}	During HALT *1	Without panel load		6.0	10.5	µA
		During operation *1	OSC1 is CR oscillation		8.7	14.0	µA

*1: The SVD circuit and analog voltage comparator are turned OFF.

E0C62L82 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L4} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.85	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.85	V
	V_{L4}	Connect 1MΩ load resistor between V_{DD} and V_{L4} (without panel load)		4•V_{L1} -0.1		4•V_{L1} ×0.85	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (CMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (CMPM)					
Analog comparator offset voltage	V_{OF}					20	mV
Analog comparator response time	t_{CMP}	V_{IP}=-1.1V, V_{IM}=V_{IP}±30mV				1	mS
Current consumption	I_{OP1}	During HALT *1	Without panel load		2.5	6.0	µA
		During operation *1	OSC1 is crystal oscillation		7.0	12.0	µA
	I_{OP2}	During HALT *1	Without panel load		11.5	20.5	µA
		During operation *1	OSC1 is CR oscillation		16.5	27.0	µA

*1: The SVD circuit and analog voltage comparator are turned OFF.

E0C62A82 (Normal Operating Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L4} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		0.5•V_{L2} -0.1		0.5•V_{L2} +0.1	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		-2.25	-2.10	-1.95	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
	V_{L4}	Connect 1MΩ load resistor between V_{DD} and V_{L4} (without panel load)		4•V_{L1} -0.1		4•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (CMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (CMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{CMP}	V_{IP}=-1.5V, V_{IM}=V_{IP}±15mV				1	mS
Current consumption	I_{OP1}	During HALT *1	Without panel load		1.70	3.0	µA
		During operation at 32kHz *1	OSC1 is crystal		4.0	7.0	µA
		During operation at 1MHz *2	oscillation		150.0	300.0	µA
	I_{OP2}	During HALT *1	Without panel load		30	60	µA
		During operation at 32kHz *1	OSC1 is CR oscillation		30	60	µA
		During operation at 1MHz *2			160	300	µA

*1: The OSC3 circuit, SVD circuit and analog voltage comparator are turned OFF.
*2: The SVD circuit and analog voltage comparator are turned OFF.

E0C62A82 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L4} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		0.5•V_{L2} -0.1		0.5•V_{L2} +0.1	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		-2.25	-2.10	-1.95	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
	V_{L4}	Connect 1MΩ load resistor between V_{DD} and V_{L4} (without panel load)		4•V_{L1} -0.1		4•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (CMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (CMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{CMP}	V_{IP}=-1.5V, V_{IM}=V_{IP}±15mV				1	mS
Current consumption	I_{OP1}	During HALT *1	Without panel load		11.7	33.0	µA
		During operation at 32kHz *1	OSC1 is crystal		14.0	37.0	µA
		During operation at 1MHz *2	oscillation		160.0	330.0	µA
	I_{OP2}	During HALT *1	Without panel load		40	90	µA
		During operation at 32kHz *1	OSC1 is CR oscillation		40	90	µA
		During operation at 1MHz *2			200	420	µA

*1: The OSC3 circuit, SVD circuit and analog voltage comparator are turned OFF.
*2: The SVD circuit and analog voltage comparator are turned OFF.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

E0C6282/62A82 (OSC1 Crystal oscillation)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (Vss)	-2.2			V
Oscillation stop voltage	Vstp	tstp≤10sec (Vss)	-2.2			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	Vss=-2.2 to -5.5V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	40			ppm
Harmonic oscillation start voltage	Vhho	(Vss)			-5.5	V
Permitted leak resistance	Rleak	Between OSC1 and V_{DD}, Vss	200			MΩ

E0C62L82 (OSC1 Crystal oscillation)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (Vss)	-1.1			V
Oscillation stop voltage	Vstp	tstp≤10sec (Vss)	-1.1(-0.9)*1			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	Vss=-1.1 to -3.5V (-0.9) *1			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	40			ppm
Harmonic oscillation start voltage	Vhho	(Vss)			-3.5	V
Permitted leak resistance	Rleak	Between OSC1 and V_{DD}, Vss	200			MΩ

*1: Items enclosed in parentheses ( ) are those used when operating at heavy load protection mode.

E0C6282/62A82 (OSC1 CR oscillation)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, R_{CR}=850kΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC1}		-20	32.768kHz	20	%
Oscillation start voltage	Vsta	(Vss)	-2.2			V
Oscillation start time	tsta	Vss=-2.2 to -5.5V		3		mS
Oscillation stop voltage	Vstp	(Vss)	-2.2			V

E0C62L82 (OSC1 CR oscillation)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, R_{CR}=850kΩ, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC1}		-20	32.768kHz	20	%
Oscillation start voltage	Vsta	(Vss)	-0.9			V
Oscillation start time	tsta	Vss=0.9 to -3.5V		3		mS
Oscillation stop voltage	Vstp	(Vss)	-0.9			V

E0C62A82 (OSC3 CR oscillation)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, R_{CR}=35kΩ, Ta=25°C)

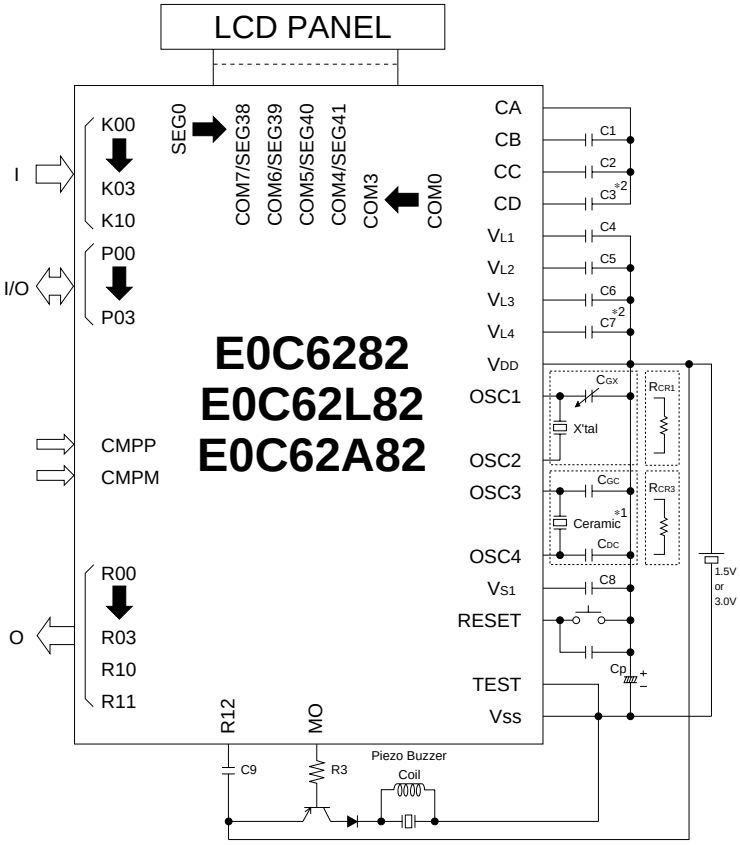
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	1MHz	30	%
Oscillation start voltage	Vsta	(Vss)	-2.2			V
Oscillation start time	tsta	Vss=-2.2 to -5.5V			3	mS
Oscillation stop voltage	Vstp	(Vss)	-2.2			V

E0C62A82 (OSC1 Ceramic oscillation)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, ceramic oscillation: 1MHz, C_{GC}=C_{DC}=100pF, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(Vss)	-2.2			V
Oscillation start time	tsta	Vss=-2.2 to -5.5V			5	mS
Oscillation stop voltage	Vstp	(Vss)	-2.2			V

■ BASIC EXTERNAL CONNECTION DIAGRAM



X'tal	Crystal oscillator	32.768kHz C_I(Max.)=35kΩ
R_{CR1}	Resistor for CR oscillation	850kΩ
C_{GX}	Trimmer capacitor	5–25pF
Ceramic	Ceramic oscillator	1MHz(Typ.)
R_{CR3}	Resistor for CR oscillation	35kΩ
C_{GC}, C_{DC}	Capacitor	100pF
C1–C8	Capacitor	0.1µF
C9	Capacitor	1µF–10µF
Cp	Capacitor	3.3µF
R3	Resistor	1kΩ

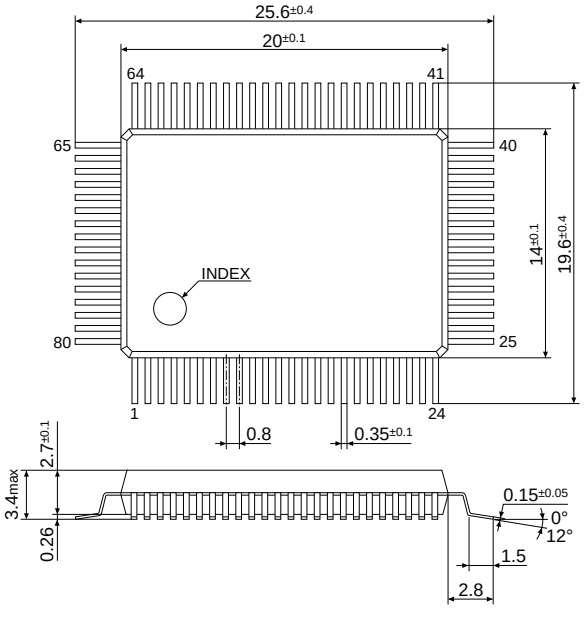
∗1 OSC3 oscillation circuit can be used only for E0C62A82. For the E0C6282 and 62L82, do not connect anything to terminals OSC3 and OSC4.

∗2 In case 1/4 duty was selected with the mask option, set CD and V_{L4} to N.C. (not connected). The C3 and C7 capacitor are not required.

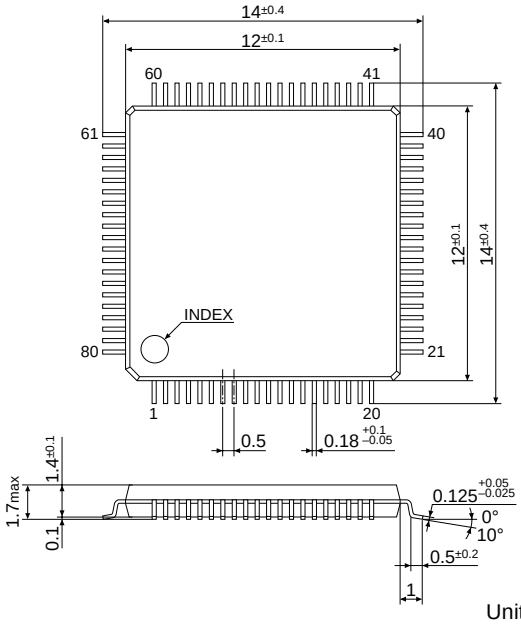
Note: The above table is simply an example, and is not guaranteed to work.

■ PACKAGE DIMENSIONS

Plastic QFP5-80pin



Plastic QFP14-80pin



Unit: mm

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