# n-channel JFETs *designed for . . .*

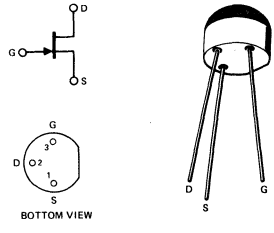
- **Analog Switches**
- **Choppers**
- **Commutators**

**Performance Curves NVA See Section 4**

BENEFITS

- Very Low Insertion Loss
  $R_{DS(on)} < 3\ \Omega$ (E105)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver

TO-106
See Section 5




## ABSOLUTE MAXIMUM RATINGS (25°C)

| | |
|---|---|
| Gate-Drain or Gate-Source Voltage | -30 V |
| Gate Current | 50 mA |
| Total Device Dissipation (25°C Free-Air Temperature) | 350 mW |
| Power Derating (to +125°C) | 3.5 mW/°C |
| Storage Temperature Range | -55 to +125°C |
| Operating Temperature Range | -55 to +125°C |
| Lead Temperature (1/16" from case for 10 seconds) | 300°C |

## ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| | | Characteristic | | E105 | | | E106 | | | E107 | | | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | | |
| 1 | STATIC | $I_{GSS}$ | Gate Reverse Current (Note 1) | | | -3 | | | -3 | | | -3 | nA | $V_{DS}$ = 0, $V_{GS}$ = -15 V | |
| 2 | STATIC | $V_{GS(off)}$ | Gate-Source Cutoff Voltage | -4.5 | | -10 | -2 | | -6 | -0.5 | | -4.5 | V | $V_{DS}$ = 5 V, $I_D$ = 1 μA | |
| 3 | STATIC | $BV_{GSS}$ | Gate-Source Breakdown Voltage | -30 | | | -30 | | | -30 | | | V | $V_{DS}$ = 0, $I_G$ = -1 μA | |
| 4 | STATIC | $I_{DSS}$ | Saturation Drain Current (Note 2) | 500 | | | 200 | | | 100 | | | mA | $V_{DS}$ = 15 V, $V_{GS}$ = 0 | |
| 5 | STATIC | $I_{D(off)}$ | Drain Cutoff Current (Note 1) | | | 3 | | | 3 | | | 3 | nA | $V_{DS}$ = 5 V, $V_{GS}$ = -10 V | |
| 6 | STATIC | $r_{DS(on)}$ | Drain Source ON Resistance | | | 3 | | | 6 | | | 8 | Ω | $V_{DS} \leq 0.1$ V, $V_{GS}$ = 0 | |
| 7 | DYNAMIC | $C_{dg(off)}$ | Drain Gate OFF Capacitance | | | 35 | | | 35 | | | 35 | pF | $V_{DS}$ = 0, $V_{GS}$ = -10 V | f = 1 MHz |
| 8 | DYNAMIC | $C_{sg(off)}$ | Source Gate OFF Capacitance | | | 35 | | | 35 | | | 35 | pF | $V_{DS}$ = 0, $V_{GS}$ = -10 V | f = 1 MHz |
| 9 | DYNAMIC | $C_{dg(on)}$ + $C_{sg(on)}$ | Drain Gate plus Source Gate ON Capacitance | | | 160 | | | 160 | | | 160 | pF | $V_{DS}$ = $V_{GS}$ = 0 | f = 1 MHz |
| 10 | DYNAMIC | $t_{d(on)}$ | Turn On Delay Time | | 15 | | | 15 | | | 15 | | ns | Switching Time Test Conditions | |
| 11 | DYNAMIC | $t_r$ | Rise Time | | 20 | | | 20 | | | 20 | | ns | | |
| 12 | DYNAMIC | $t_{d(off)}$ | Turn Off Delay Time | | 15 | | | 15 | | | 15 | | ns | | |
| 13 | DYNAMIC | $t_f$ | Fall Time | | 20 | | | 20 | | | 20 | | ns | | |

| Switching Time Test Conditions | E105 | E106 | E107 |
|---|---|---|---|
| $V_{DD}$ | 1.5 V | 1.5 V | 1.5 V |
| $V_{GS(off)}$ | -12 V | -7 V | -5 V |
| $R_L$ | 50 Ω | 50 Ω | 50 Ω |

**NOTES:**

1. Approximately doubles for every 10°C increase in $T_A$.
2. Pulse test duration = 300 μs; duty cycle ≤ 3%.

**NVA**