p-channel JFETs *designed for . . .*

- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves PS
See Section 4

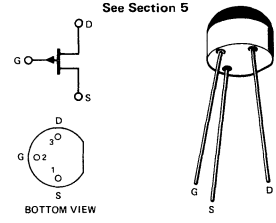
BENEFITS

- Low Insertion Loss
  $R_{DS(on)} < 85\ \Omega$ (E174)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Short Sample and Hold Aperture Time
  $C_{sg(off)}$ = 5.5 pF Typical
  $C_{dg(off)}$ = 5.5 pF Typical
- Fast Switching
  $t_{d(on)} + t_r$ = 7 ns Typical

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . 30 V
Gate Current . . . . . 50 mA
Total Device Dissipation
(25°C Free-Air Temperature) . . . . . 350 mW
Power Derating (to +125°C) . . . . . 3.5 mW/°C
Storage Temperature Range . . . . . -55 to +125°C
Operating Temperature Range . . . . . -55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-106
See Section 5



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristics	E174 Min	E174 Typ	E174 Max	E175 Min	E175 Typ	E175 Max	E176 Min	E176 Typ	E176 Max	E177 Min	E177 Typ	E177 Max	Unit	Test Conditions
1	STATIC	I_{GSS} Gate Reverse Current (Note 2)			1			1			1			1	nA	V_{DS} = 0, V_{GS} = 20 V
2	STATIC	$V_{GS(off)}$ Gate-Source Cutoff Voltage	5		10	3		6	1		4	0.8		2.25	V	V_{DS} = -15 V, I_D = -10 nA
3	STATIC	BV_{GSS} Gate-Source Breakdown Voltage	30			30			30			30			V	V_{DS} = 0, I_G = 1 μA
4	STATIC	I_{DSS} Saturation Drain Current (Note 3)	-20		-100	-7		-60	-2		-25	-1.5		-20	mA	V_{DS} = -15 V, V_{GS} = 0
5	STATIC	$I_{D(off)}$ Drain Cutoff Current (Note 2)			-1			-1			-1			-1	nA	V_{DS} = -15 V, V_{GS} = 10 V
6	STATIC	$r_{DS(on)}$ Drain-Source ON Resistance			85			125			250			300	Ω	V_{GS} = 0, V_{DS} = -0.1 V
7	DYNAMIC	$C_{dg(off)}$ Drain-Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	V_{DS} = 0, V_{GS} = 10 V; f = 1 MHz
8	DYNAMIC	$C_{sg(off)}$ Source-Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	V_{DS} = 0, V_{GS} = 10 V; f = 1 MHz
9	DYNAMIC	$C_{dg(on)} + C_{sg(on)}$ Drain-Gate Plus Source-Gate ON Capacitance		40			40			40			40		pF	V_{DS} = V_{GS} = 0; f = 1 MHz
10	DYNAMIC	$t_{d(on)}$ Turn On Delay Time		2			5			15			20		ns	Switching Time Test Conditions
11	DYNAMIC	t_r Rise Time		5			10			20			25		ns	
12	DYNAMIC	$t_{d(off)}$ Turn Off Delay Time		5			10			15			20		ns	
13	DYNAMIC	t_f Fall Time		10			20			20			25		ns	

Switching Time Test Conditions	E174	E175	E176	E177
V_{DD}	-10 V	-6 V	-6 V	-6 V
$V_{GS(off)}$	12 V	8 V	6 V	3 V
R_L	560 Ω	1.2 KΩ	5.6 KΩ	10 KΩ
$V_{GS(on)}$	0 V	0 V	0 V	0 V

PS

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 300 μs; duty cycle ≤ 3%.