



STE180NE10

N-CHANNEL 100V - 4.5 mΩ - 180A ISOTOP STripFET™ POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STE180NE10	100 V	< 6 mΩ	180 A

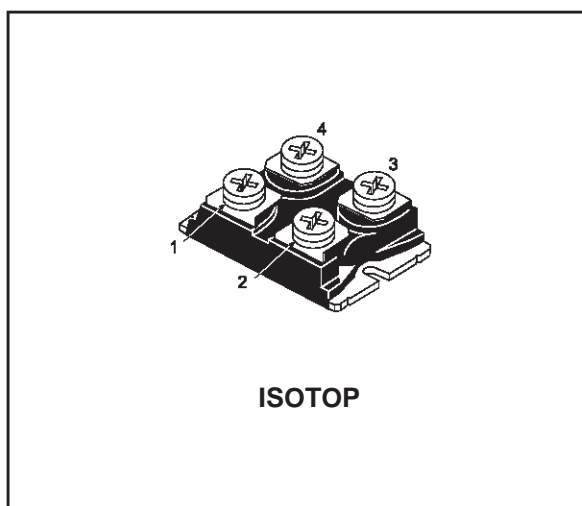
- TYPICAL R_{DS(on)} = 4.5 mΩ
- 100% AVALANCHE TESTED
- LOW INTRINSIC CAPACITANCE
- GATE CHARGE MINIMIZED
- REDUCED VOLTAGE SPREAD

DESCRIPTION

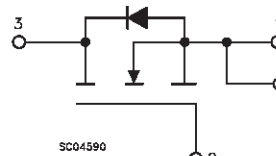
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- SMPS & UPS
- MOTOR CONTROL
- WELDING EQUIPMENT
- OUTPUT STAGE FOR PWM, ULTRASONIC CIRCUITS



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	100	V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 kΩ)	100	V
V _{GS}	Gate-source Voltage	± 20	V
I _D	Drain Current (continuous) at T _c = 25 °C	180	A
I _D	Drain Current (continuous) at T _c = 100 °C	119	A
I _{DM} (•)	Drain Current (pulsed)	540	A
P _{tot}	Total Dissipation at T _c = 25 °C	360	W
	Derating Factor	2.88	W/°C
V _{ISO}	Insulation Withstand Voltage (AC-RMS)	2500	V
T _{stg}	Storage Temperature	-55 to 150	°C
T _j	Max. Operating Junction Temperature	150	°C

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤ 180 A, di/dt ≤ 200 A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}

November 1999

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STE180NE10**THERMAL DATA**

$R_{thj-case}$	Thermal Resistance Junction-case	Max	0.347	$^{\circ}\text{C}/\text{W}$
R_{thc-h}	Thermal Resistance Case-heatsink With conductive Grease Applied	Max	0.05	$^{\circ}\text{C}/\text{W}$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	60	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 25\text{ V}$)	720	mJ

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1\text{ mA}$ $V_{GS} = 0$	100			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_c = 125^{\circ}\text{C}$			4 40	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 400	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 1\text{ mA}$	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}$ $I_D = 90\text{ A}$		4.5	6	$\text{m}\Omega$
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10\text{ V}$	180			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 80\text{ A}$	30			S
C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0$		21		nF
C_{oss}	Output Capacitance			2.5		nF
C_{rss}	Reverse Transfer Capacitance			0.9		nF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 50\text{ V}$ $I_D = 90\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, see fig. 3)		35		ns
t_r	Rise Time			100		ns
Q_g	Total Gate Charge	$V_{DD} = 80\text{ V}$ $I_D = 180\text{ A}$ $V_{GS} = 10\text{ V}$		142	185	nC
Q_{gs}	Gate-Source Charge			37		nC
Q_{gd}	Gate-Drain Charge			60		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-off Delay Time	$V_{DD} = 50\text{ V}$ $I_D = 90\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, see fig. 3)		110		ns
t_r	Fall Time			100		ns
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 80\text{ V}$ $I_D = 180\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Inductive Load, see fig. 5)		100		ns
t_f	Fall Time			50		ns
t_c	Cross-over Time			92		ns

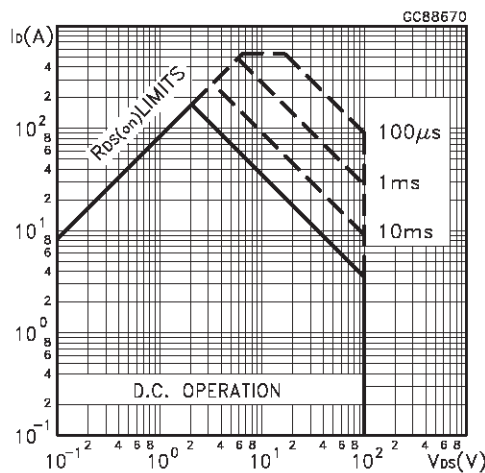
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				180	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				540	A
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 180\text{ A}$ $V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 180\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 50\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, fig. 5)		170		ns
Q_{rr}	Reverse Recovery Charge			850		μC
I_{RRM}	Reverse Recovery Current			10		A

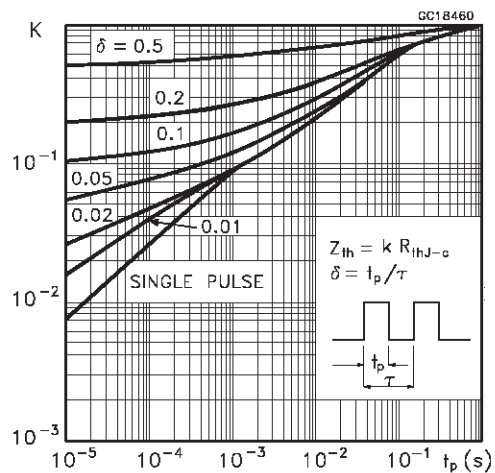
(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

(•) Pulse width limited by safe operating area

Safe Operating Area

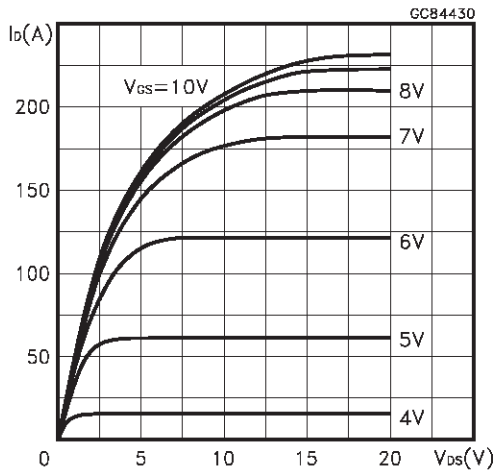


Thermal Impedance

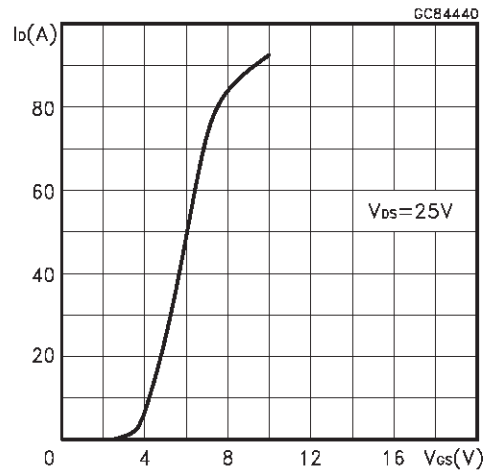


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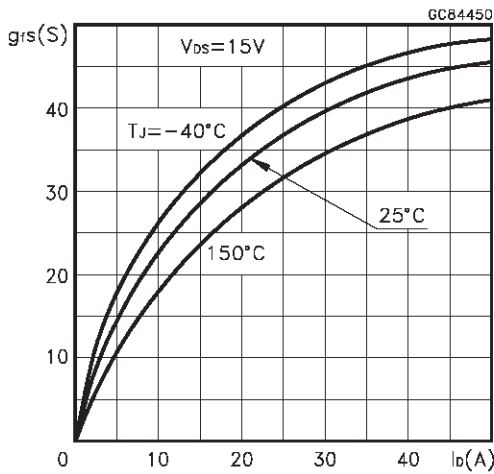
Output Characteristics



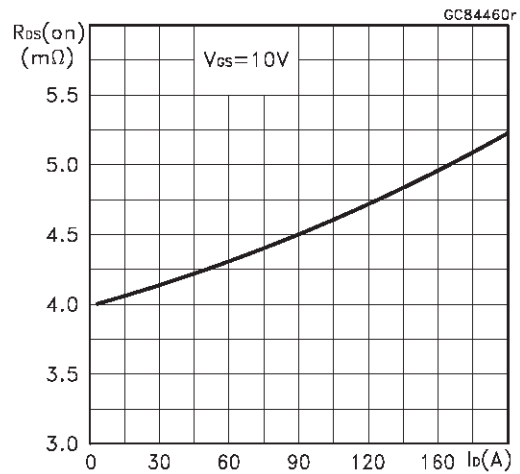
Transfer Characteristics



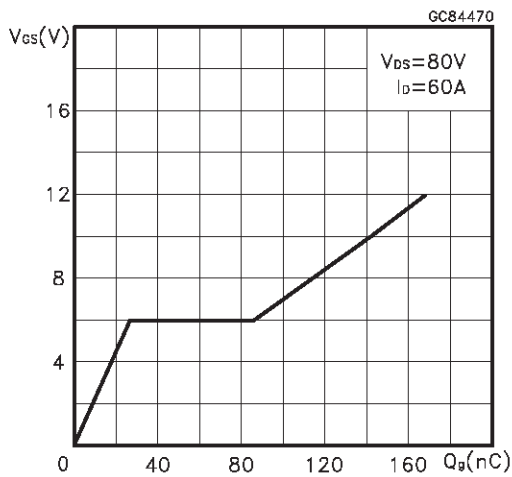
Transconductance



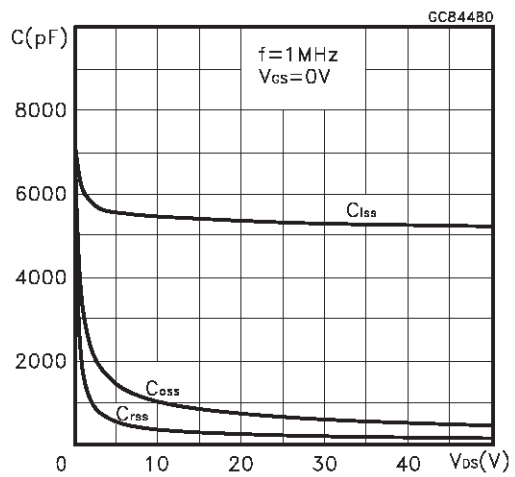
Static Drain-source On Resistance



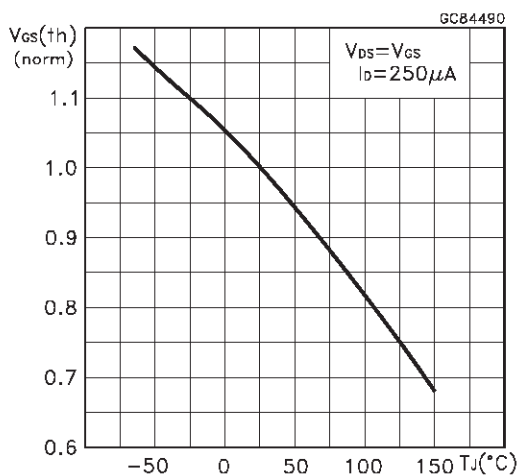
Gate Charge vs Gate-source Voltage



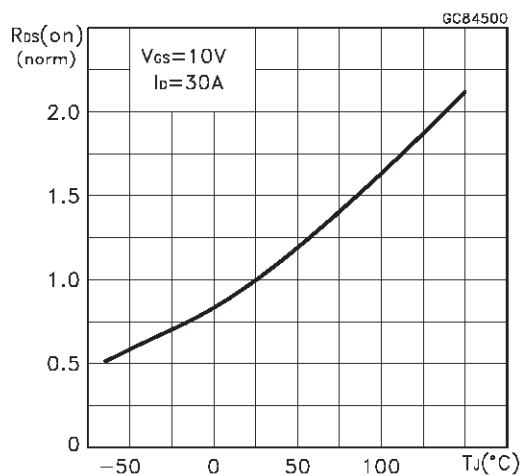
Capacitance Variations



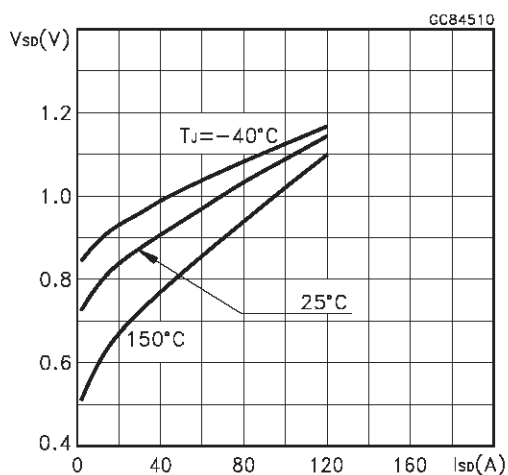
Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics



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Fig. 1: Unclamped Inductive Load Test Circuit

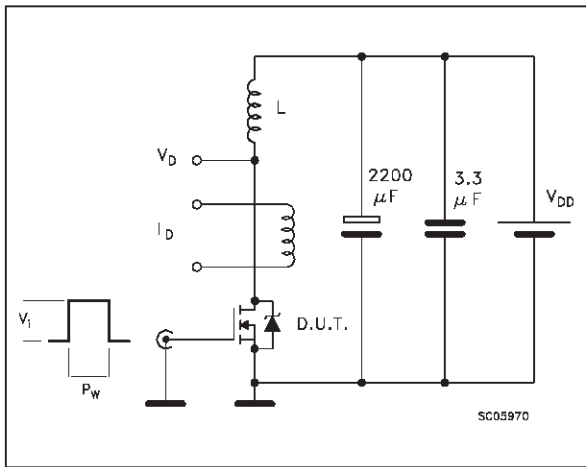


Fig. 2: Unclamped Inductive Waveform

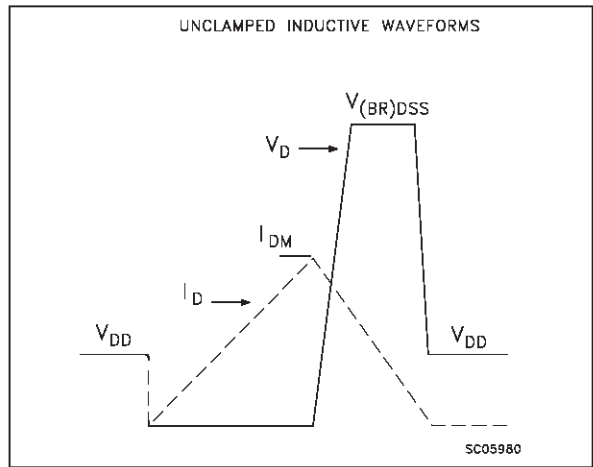


Fig. 3: Switching Times Test Circuits For Resistive Load

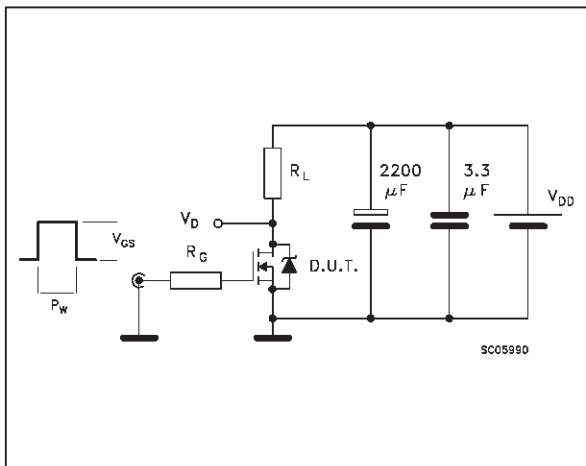


Fig. 4: Gate Charge test Circuit

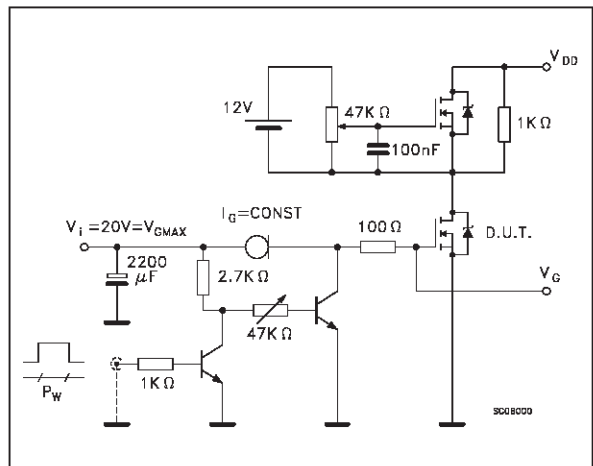
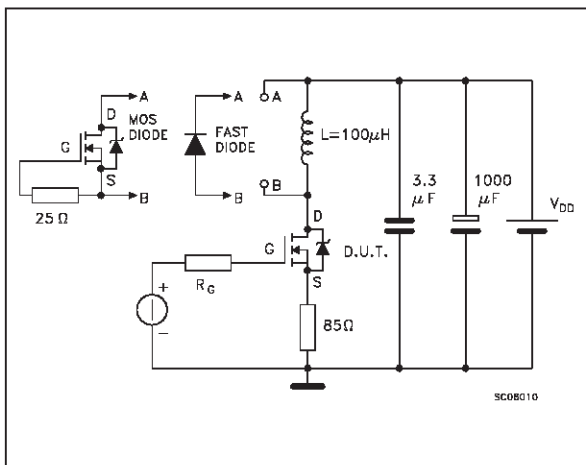
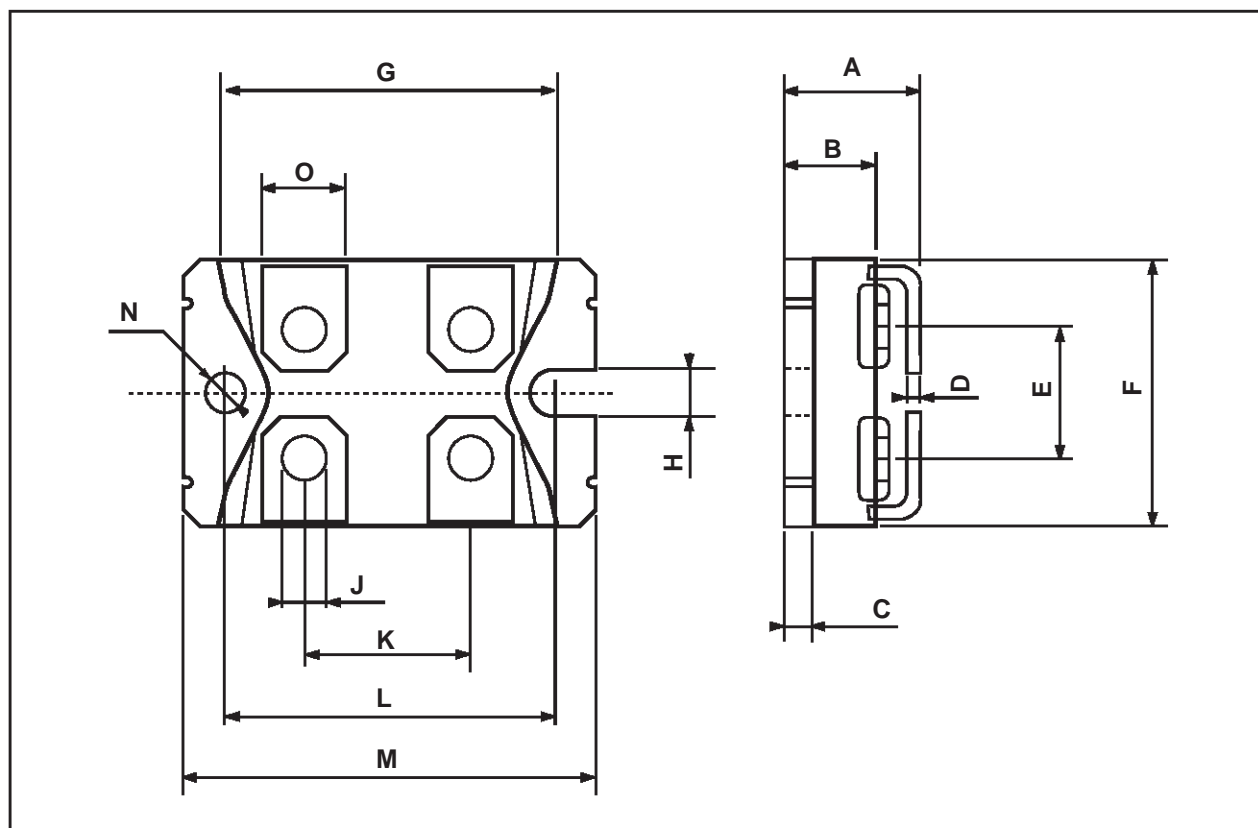


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



ISOTOP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	11.8		12.2	0.466		0.480
B	8.9		9.1	0.350		0.358
C	1.95		2.05	0.076		0.080
D	0.75		0.85	0.029		0.033
E	12.6		12.8	0.496		0.503
F	25.15		25.5	0.990		1.003
G	31.5		31.7	1.240		1.248
H	4			0.157		
J	4.1		4.3	0.161		0.169
K	14.9		15.1	0.586		0.594
L	30.1		30.3	1.185		1.193
M	37.8		38.2	1.488		1.503
N	4			0.157		
O	7.8		8.2	0.307		0.322



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