

E4M0025075J2

Silicon Carbide Power MOSFET
E-Series Automotive
N-Channel Enhancement Mode



Features

- 750V SiC MOSFET technology
- Optimized package with separate driver source pin
- 4.7mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant
- Automotive Qualified (AEC-Q101) and PPAP Capable

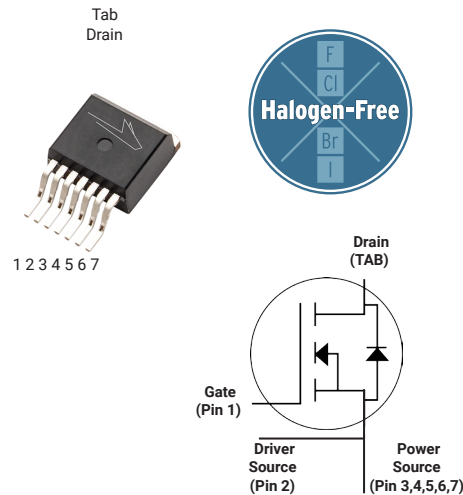
Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Applications

- Motor Control
- EV On Board Battery Chargers (OBC)
- Automotive DC/DC Converters for EV/HEV

Package



Part Number	Package	Marking
E4M0025075J2	TO-263-7XL	E4M0025075J2

Maximum Ratings ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit	Note	
V_{DSmax}	Drain - Source Voltage	750	V		
V_{GSmax}	Gate - Source Voltage	-8/+19	V	Note: 1	
I_D	Continuous Drain Current, $V_{GS} = 15\text{ V}$	$T_c = 25^\circ\text{C}$	84	A	Fig. 19 Note: 2
		$T_c = 100^\circ\text{C}$	61		
$I_{D(pulse)}$	Pulsed Drain Current, Pulse width t_p limited by T_{jmax}	251	A	Fig. 22	
P_D	Power Dissipation, $T_c=25^\circ\text{C}$, $T_j = 175^\circ\text{C}$	281	W	Fig. 20 Note: 2	
T_j, T_{stg}	Operating Junction and Storage Temperature	-55 to +175	$^\circ\text{C}$		
T_L	Solder Temperature, 1.6mm (0.063") from case for 10s	260	$^\circ\text{C}$		

Note (1): Recommended turn off / turn on gate voltage $V_{GSop} = -4V..0V / +15V$

Note (2): Verified by design


Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	750			V	$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.6	3.8	V	$V_{DS} = V_{GS}, I_D = 9.22\ \text{mA}$	Fig. 11
			2.1		V	$V_{DS} = V_{GS}, I_D = 9.22\ \text{mA}, T_J = 175^\circ\text{C}$	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	$V_{DS} = 750\ \text{V}, V_{GS} = 0\ \text{V}$	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	$V_{GS} = 15\ \text{V}, V_{DS} = 0\ \text{V}$	
$R_{DS(on)}$	Drain-Source On-State Resistance		25	34	m Ω	$V_{GS} = 15\ \text{V}, I_D = 33.5\ \text{A}$	Fig. 4, 5, 6
			35			$V_{GS} = 15\ \text{V}, I_D = 33.5\ \text{A}, T_J = 175^\circ\text{C}$	
g_{fs}	Transconductance		24		S	$V_{DS} = 20\ \text{V}, I_{DS} = 33.5\ \text{A}$	Fig. 7
			18			$V_{DS} = 20\ \text{V}, I_{DS} = 33.5\ \text{A}, T_J = 175^\circ\text{C}$	
C_{iss}	Input Capacitance		3055		pF	$V_{GS} = 0\ \text{V}, V_{DS} = 500\ \text{V}$ $f = 100\ \text{kHz}$ $V_{AC} = 25\ \text{mV}$	Fig. 17, 18
C_{oss}	Output Capacitance		158				
C_{rss}	Reverse Transfer Capacitance		16				
E_{oss}	C_{oss} Stored Energy		23		μJ	$V_{DS} = 500\ \text{V}, f = 100\ \text{kHz}$	Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		201		pF	$V_{GS} = 0\ \text{V}, V_{DS} = 0\ \text{to}\ 500\ \text{V}$	Note: 3
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		291		pF		
E_{ON}	Turn-On Switching Energy (Body Diode FWD)		202		μJ	$V_{DS} = 500\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}, I_D = 33.5\ \text{A},$ $R_{G(ext)} = 2.5\ \Omega, L = 59\ \mu\text{H}, T_J = 175^\circ\text{C}$ FWD = Internal Body Diode	Fig. 26, 28
E_{OFF}	Turn-Off Switching Energy (Body Diode FWD)		57				
$t_{d(on)}$	Turn-On Delay Time		11		ns	$V_{DD} = 500\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}, I_D = 33.5\ \text{A},$ $R_{G(ext)} = 2.5\ \Omega, L = 59\ \mu\text{H}$ Timing relative to V_{DS} Inductive load	Fig. 27, 28
t_r	Rise Time		19				
$t_{d(off)}$	Turn-Off Delay Time		32				
t_f	Fall Time		9				
$R_{G(int)}$	Internal Gate Resistance		2.0		Ω	$f = 1\ \text{MHz}, V_{AC} = 25\ \text{mV}$	
Q_{gs}	Gate to Source Charge		34		nC	$V_{DS} = 500\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $I_D = 33.5\ \text{A}$ Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		36				
Q_g	Total Gate Charge		114				

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{ds} is rising from 0 to 500V
 $C_{o(tr)}$, a lumped capacitance that gives same charging time as C_{oss} while V_{ds} is rising from 0 to 500V


Reverse Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.8		V	$V_{GS} = -4\text{ V}, I_{SD} = 16.8\text{ A}, T_J = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.2		V	$V_{GS} = -4\text{ V}, I_{SD} = 16.8\text{ A}, T_J = 175^\circ\text{C}$	
I_S	Continuous Diode Forward Current		49	A	$V_{GS} = -4\text{ V}, T_c = 25^\circ\text{C}$	
$I_{S, pulse}$	Diode pulse Current		251	A	$V_{GS} = -4\text{ V}$, pulse width t_p limited by T_{jmax}	
t_{rr}	Reverse Recover time	15		ns	$V_{GS} = -4\text{ V}, I_{SD} = 33.5\text{ A}, V_R = 500\text{ V}$ $di_F/dt = 6745\text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$	
Q_{rr}	Reverse Recovery Charge	358		nC		
I_{rrm}	Peak Reverse Recovery Current	41		A		
t_{rr}	Reverse Recover time	17		ns	$V_{GS} = -4\text{ V}, I_{SD} = 33.5\text{ A}, V_R = 500\text{ V}$ $di_F/dt = 2240\text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$	
Q_{rr}	Reverse Recovery Charge	183		nC		
I_{rrm}	Peak Reverse Recovery Current	18		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.41	0.53	$^\circ\text{C}/\text{W}$		Fig. 21



Typical Performance

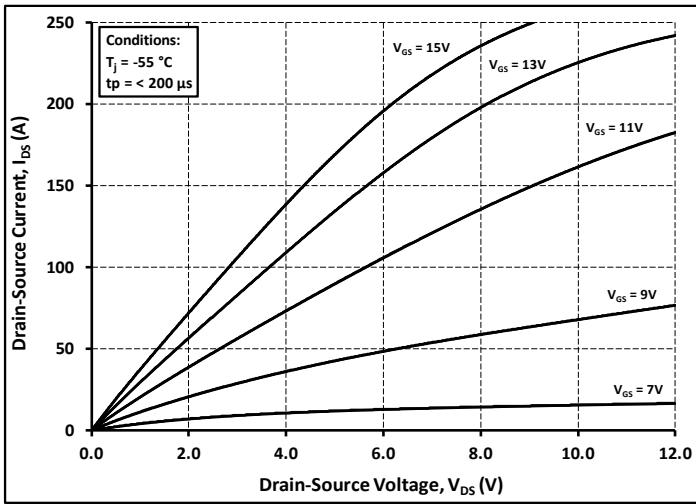


Figure 1. Output Characteristics $T_J = -55\text{ }^\circ\text{C}$

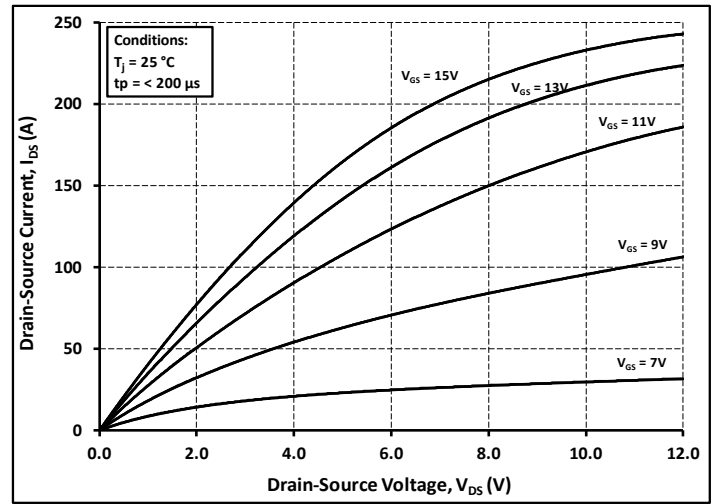


Figure 2. Output Characteristics $T_J = 25\text{ }^\circ\text{C}$

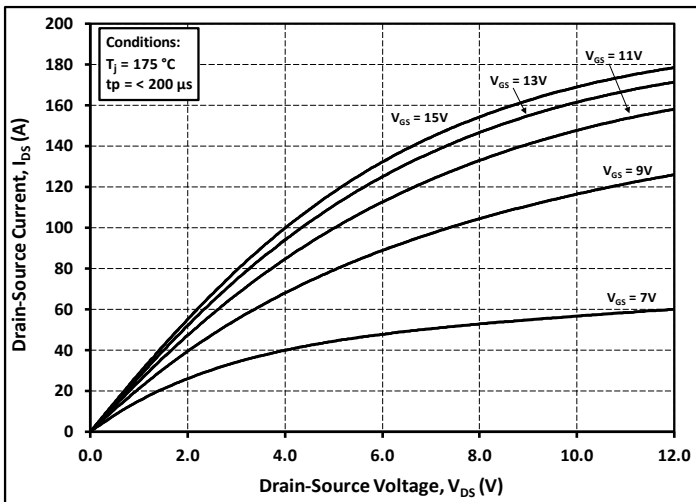


Figure 3. Output Characteristics $T_J = 175\text{ }^\circ\text{C}$

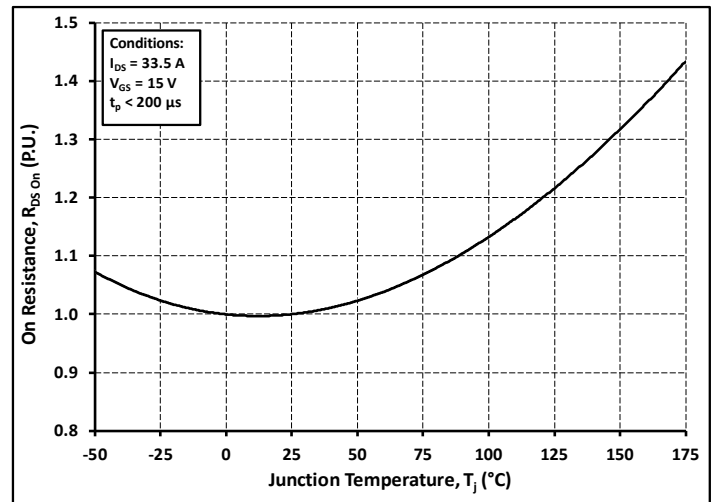


Figure 4. Normalized On-Resistance vs. Temperature

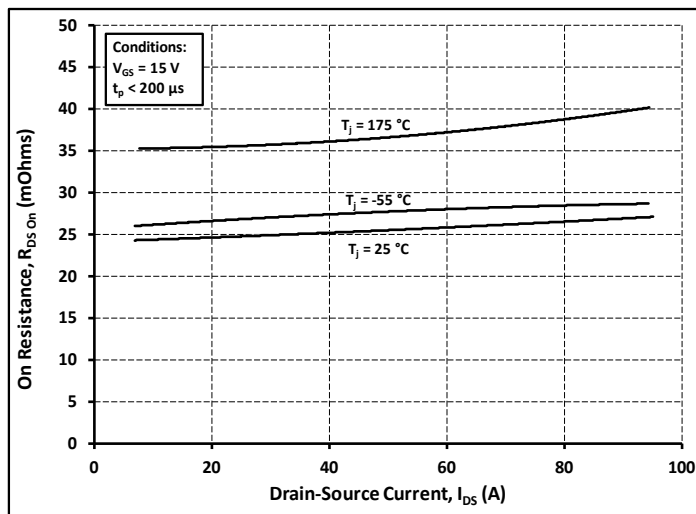


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

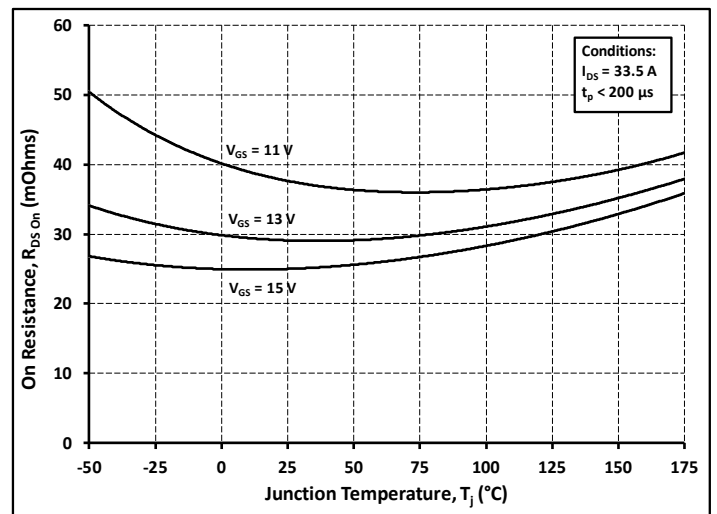


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage



Typical Performance

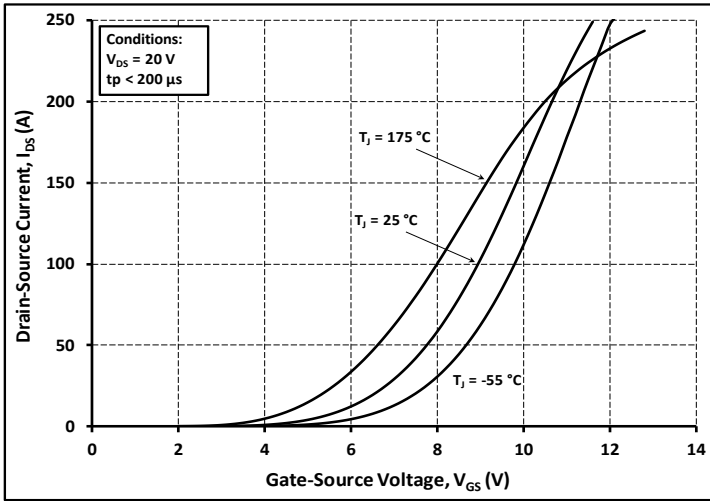


Figure 7. Transfer Characteristic for Various Junction Temperatures

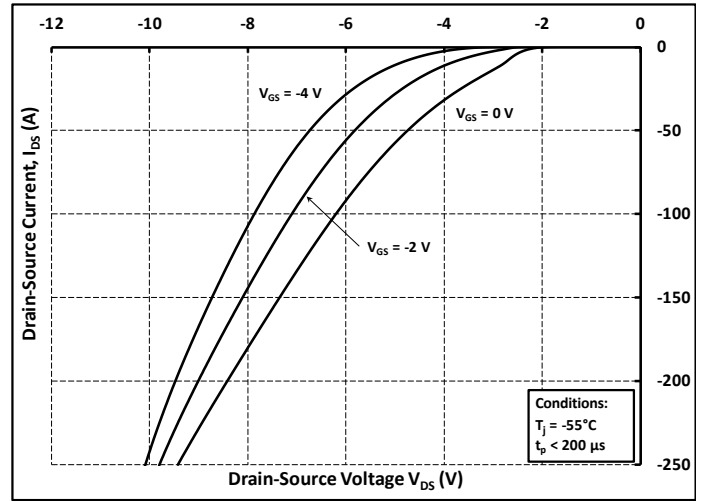


Figure 8. Body Diode Characteristic at -55 °C

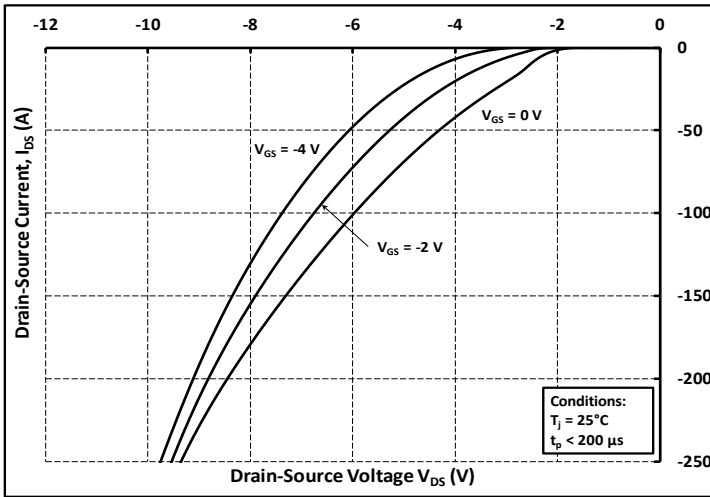


Figure 9. Body Diode Characteristic at 25 °C

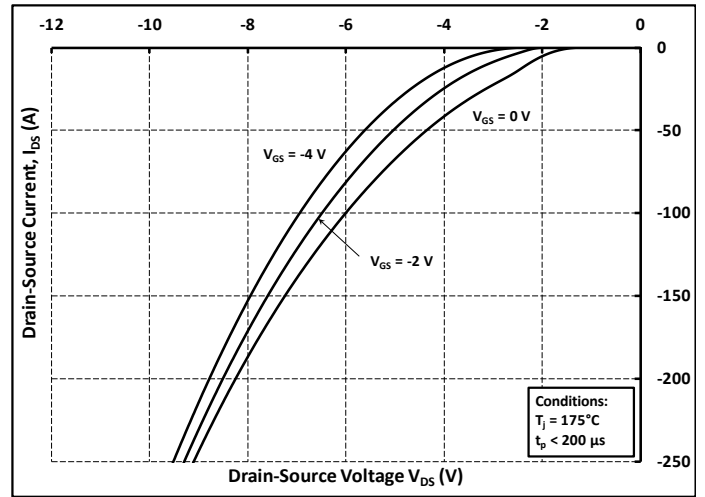


Figure 10. Body Diode Characteristic at 175 °C

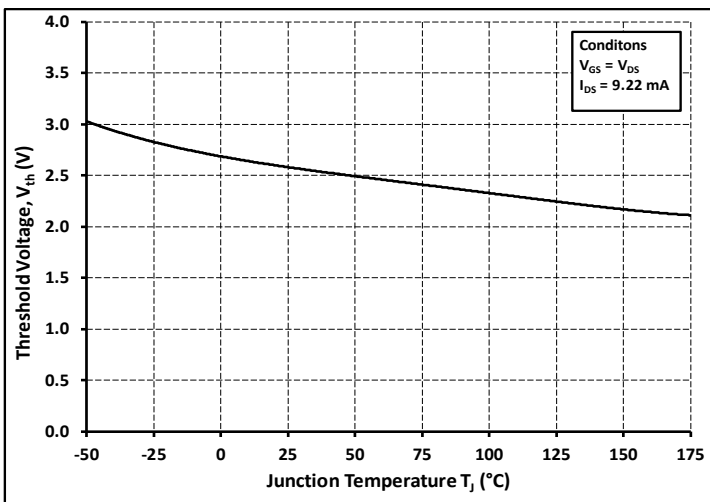


Figure 11. Threshold Voltage vs. Temperature

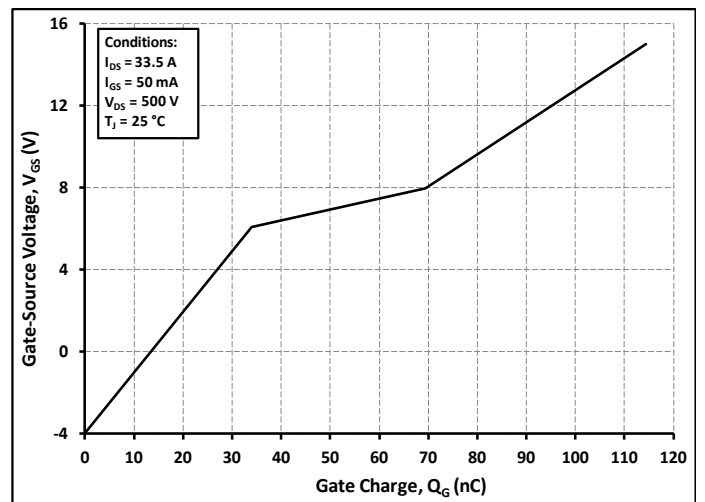


Figure 12. Gate Charge Characteristics



Typical Performance

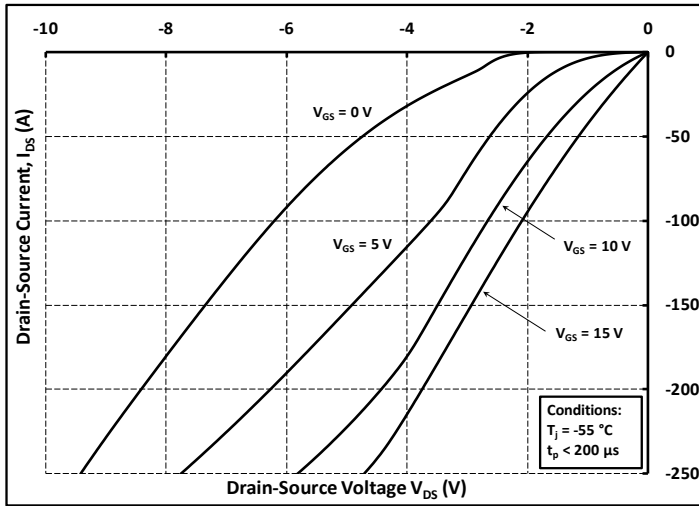


Figure 13. 3rd Quadrant Characteristic at $-55\text{ }^\circ\text{C}$

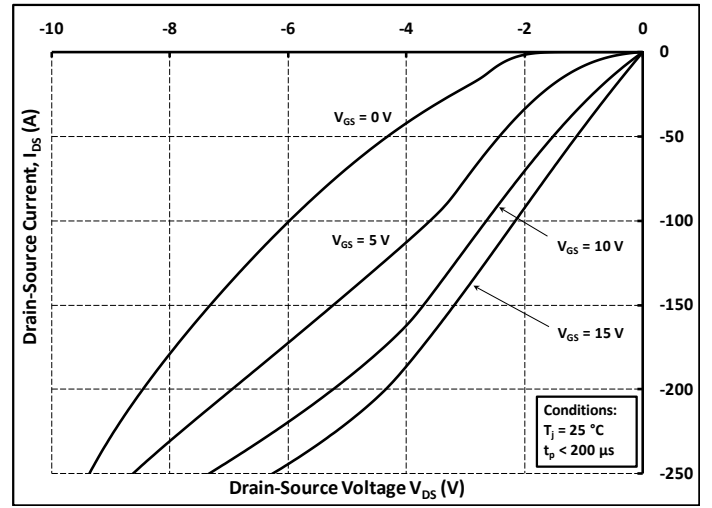


Figure 14. 3rd Quadrant Characteristic at $25\text{ }^\circ\text{C}$

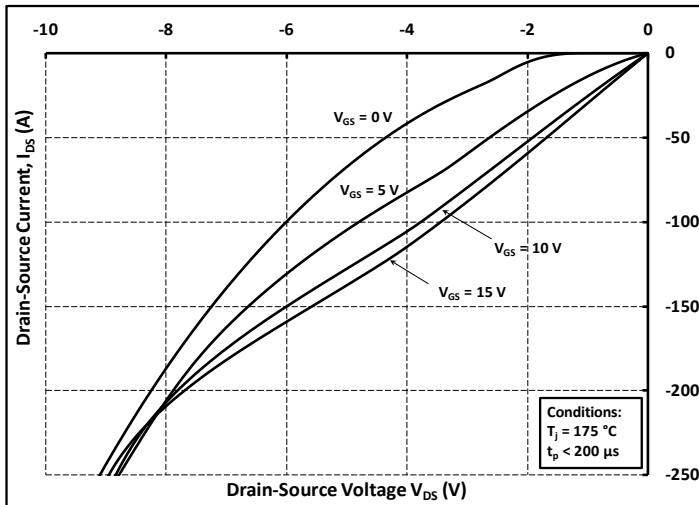


Figure 15. 3rd Quadrant Characteristic at $175\text{ }^\circ\text{C}$

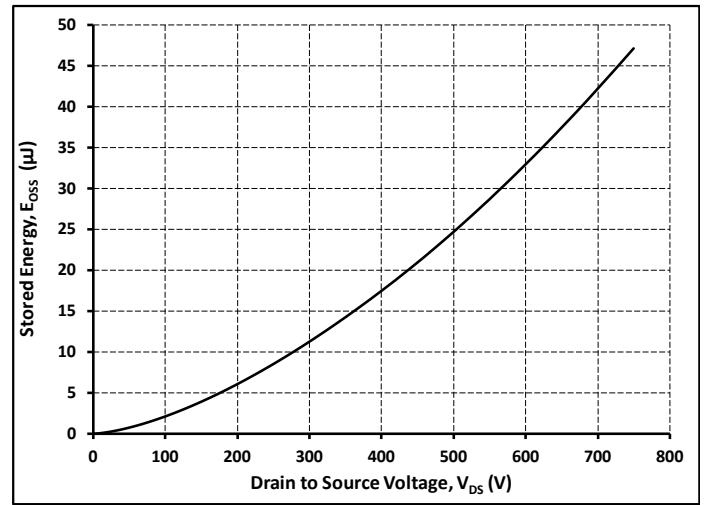


Figure 16. Output Capacitor Stored Energy

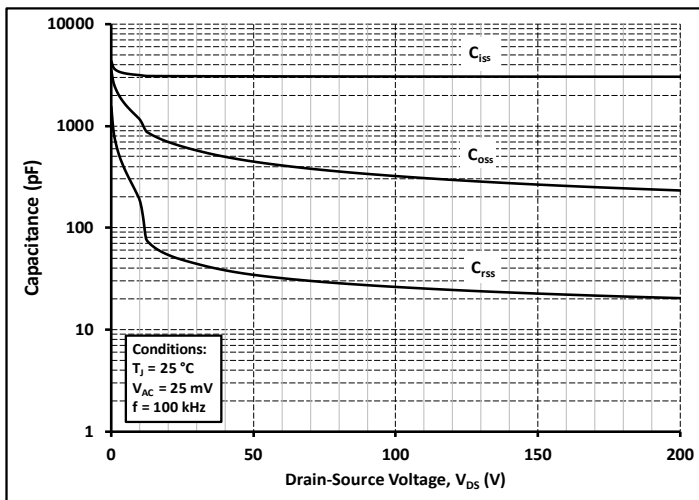


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

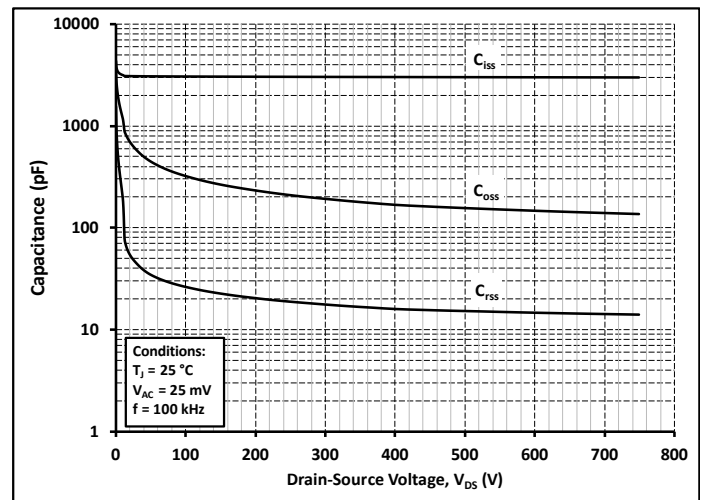


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 750V)



Typical Performance

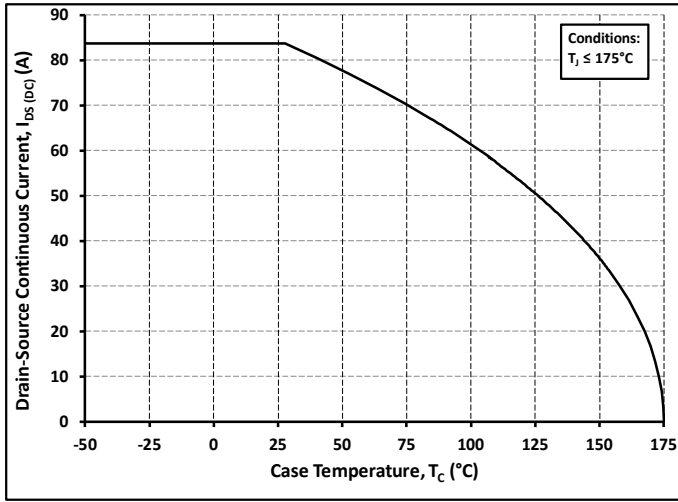


Figure 19. Continuous Drain Current Derating vs. Case Temperature

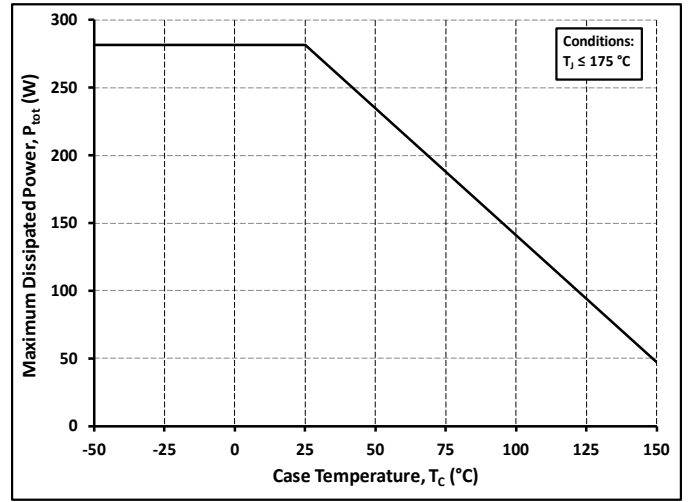


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

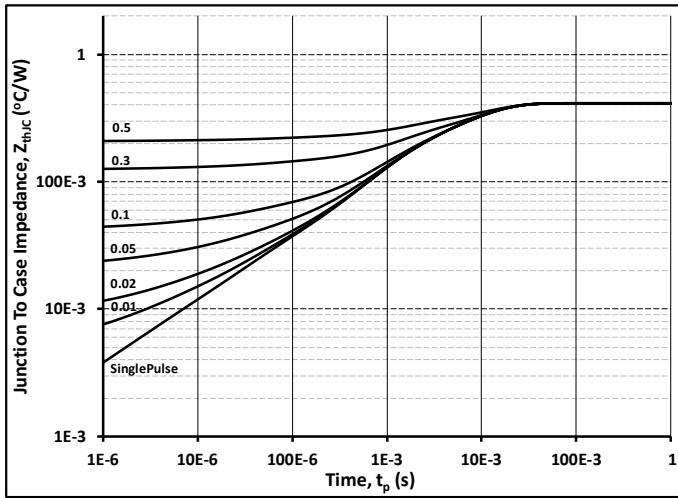


Figure 21. Transient Thermal Impedance (Junction - Case)

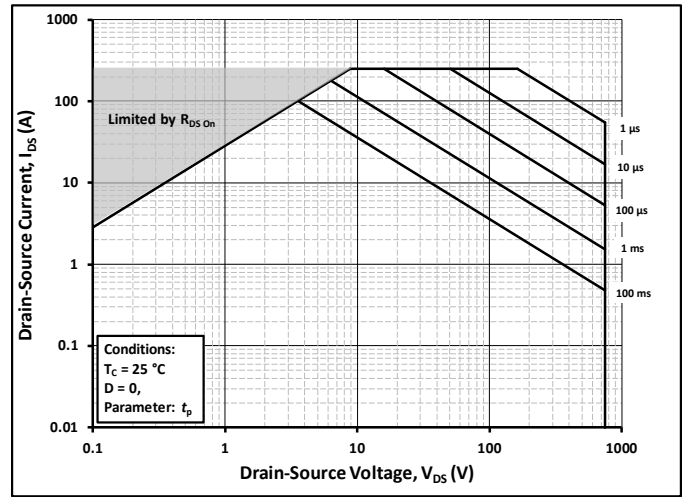


Figure 22. Safe Operating Area

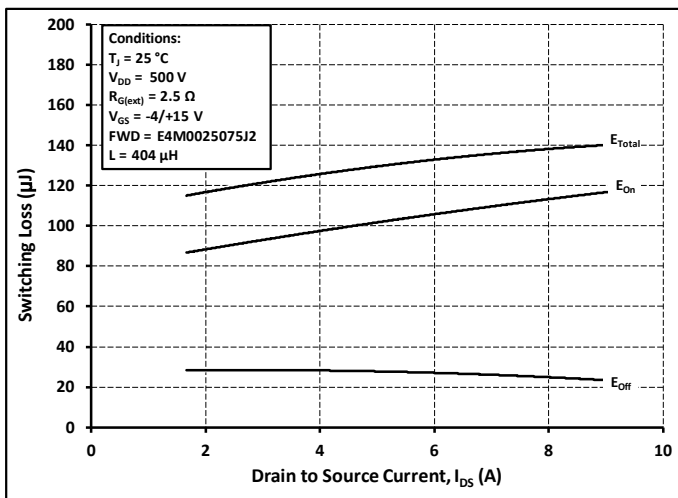


Figure 23. Clamped Inductive Switching Energy vs. Low Drain Current ($V_{DD} = 500V$)

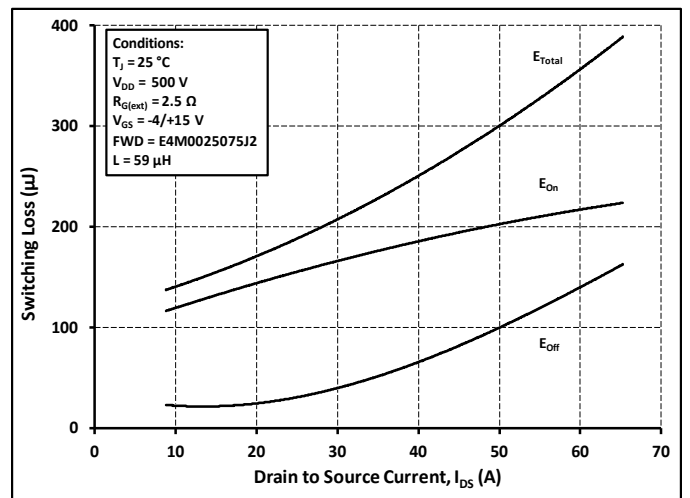


Figure 24. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 500V$)



Typical Performance

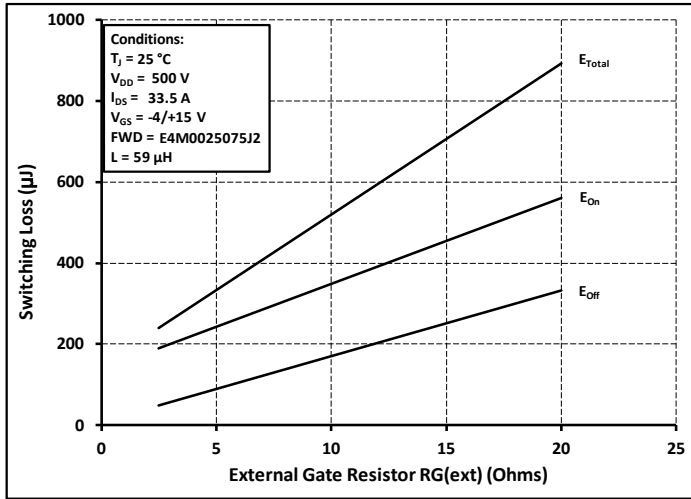


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

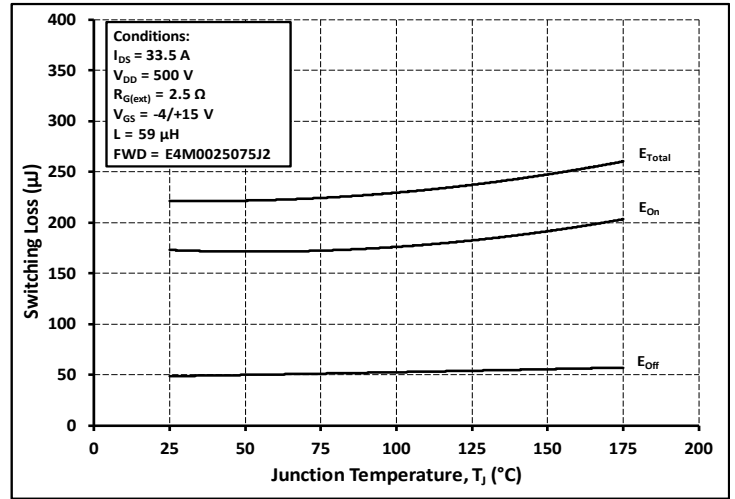


Figure 26. Clamped Inductive Switching Energy vs. Temperature

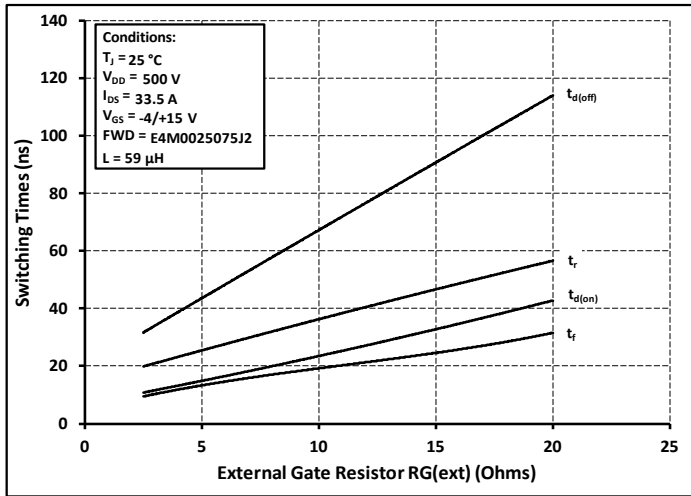


Figure 27. Switching Times vs. $R_{G(ext)}$

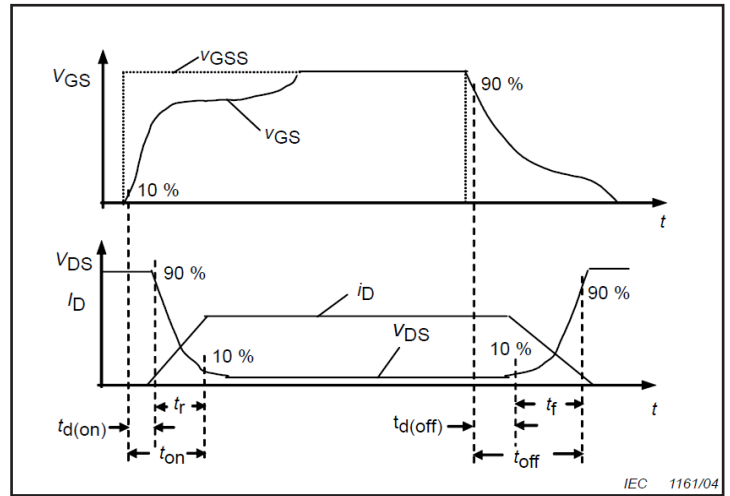


Figure 28. Switching Times Definition

Test Circuit Schematic

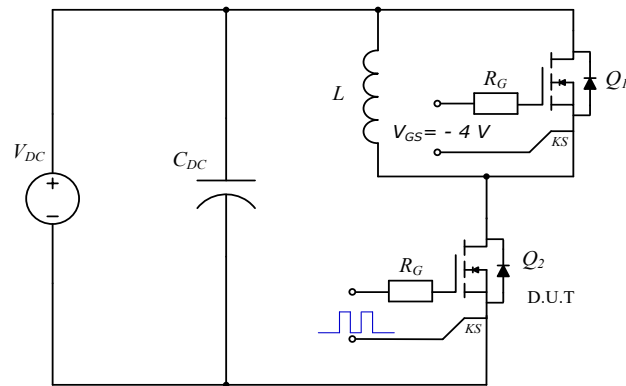
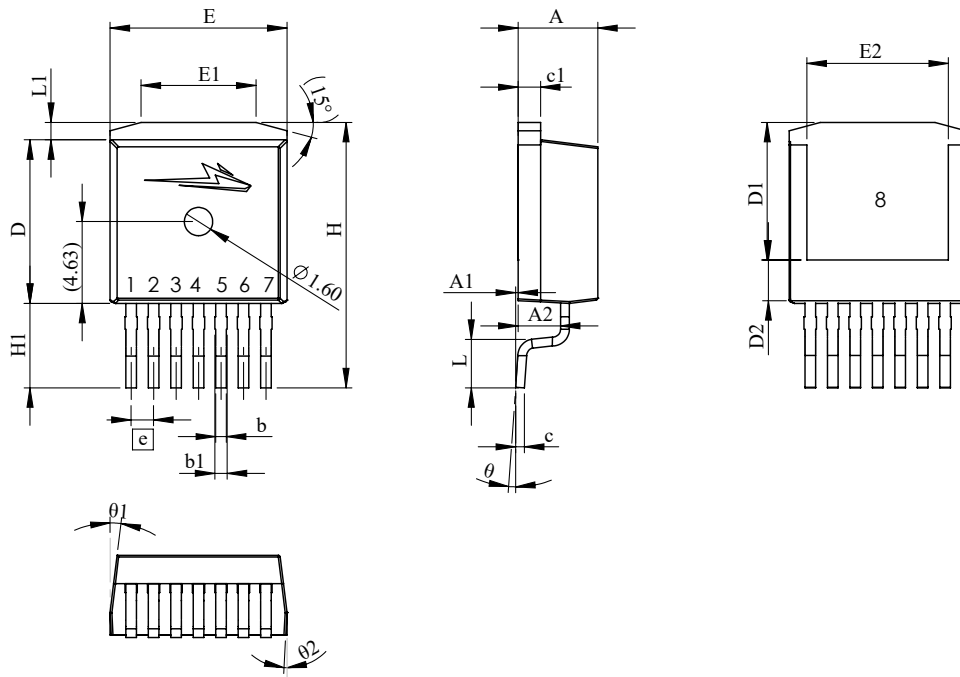


Figure 29. Clamped Inductive Switching Waveform Test Circuit



Package Dimensions



SYMBOL	MIN (mm)	MAX (mm)
A	4.30	4.70
A1	0.00	0.25
A2	2.20	2.60
b	0.52	0.72
b1	0.60	0.80
c	0.42	0.62
c1	1.07	1.47
D	9.05	9.45
D1	7.58	7.98
D2	2.05	2.45
E	9.80	10.20
E1	6.30	6.97
E2	7.80	8.20
e	1.27 BSC	
H	14.87	15.27
H1	4.55	4.95
L	2.48	2.88
L1	0.87	1.27
θ	0°	8°
θ1	4°	10°
θ2	0°	6°

1	GATE
2	KELVIN
3	SOURCE
4	
5	
6	
7	DRAIN
8	

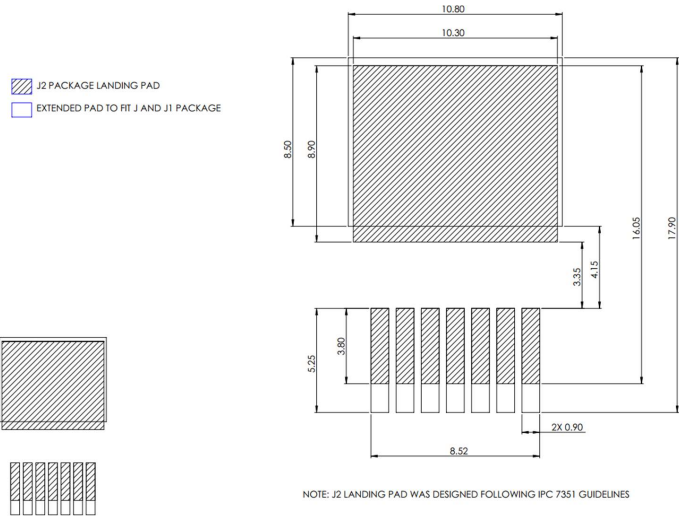
NOTE

1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS



Recommended Solder Pad Layout

All dimensions in mm





Revision history

Document Version	Date of release	Description of changes
1.0	January 2024	Initial release



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