Engineering Bulletin

EB622/D
Rev. 1, 5/2003

Motorola Book E Implementation Standards: APU ID Reference

MOTOROLA intelligence everywhere™ | digital dna™

This document contains the following:

1.1 Introduction

The e500 Application Binary Interface (ABI), and possibly other ABIs, provide a mechanism for specifying the types and revisions of APUs that are required for proper behavior of a program. This information is contained in an optional `.PPC.EMB.apuinfo` section in the ELF-format object file. This document provides the official mapping between Motorola Book E Implementation Standard APUs and the numeric APU IDs that are used in the APUinfo section. See "APU Information Section" in Chapter 3, "Object Files," of the PowerPC *e500 Application Binary Interface*, for more details on the format and usage of this section.

1.2 Motivation

The APU information is intended primarily to allow link-time checks of compatibility between object files to avoid obvious errors. For example, because both AltiVec and the signal processing engine (SPE) APU use the same instruction encodings for different instructions, linking an object file that requires AltiVec instructions with an object file that requires SPE instructions should provide an error message.

The APU information can also be used by disassemblers to unambiguously disassemble such shared opcodes. In addition, operating systems can use the APUinfo section in an application to provide transparent emulation of APUs that are not present in the hardware. Without APU information, an operating system would not know whether it should emulate AltiVec or SPE semantics for certain instruction encodings.

1.3 Implementation

The APUinfo section contains an entry for each APU that the object file requires. Each entry contains a 32-bit word: an upper 16-bit half word specifying the APU type, and a lower 16-bit half word specifying the revision of that APU. This document presents the current assignments for the APU types. See the reference manual for the implementation to determine the revision of an APU for the lower half word of the entry.

Table 1-1 provides the current APU ID assignments. Note that this application note is the definitive source for APU ID assignments and will be revised as new APUs are added.

Table 1-1. APU IDs

APU ID (16 Bits)	APU
0x0000–0x003E	Reserved for legacy use
0x003f	Motorola AltiVec APU [1]
0x0040	Book E integer select (**isel**) APU
0x0041	Motorola Book E performance monitor APU
0x0042	Motorola Book E machine check APU
0x0043	Motorola Book E cache locking APU
0x0044–0x00FF	Reserved
0x0100	Motorola Book E SPE APU
0x0101	Motorola Book E SPFP APU
0x0102	e500 branch-locking APU (also called the BTB locking APU)
0x0102–0xFFFF	Reserved

[1] Although AltiVec predates the Book E concept of APUs, AltiVec can be considered an APU.

1.4 References

PowerPC e500 Application Binary Interface, Motorola Order Number E500ABIUG/D

AltiVec Technology Programming Environments Manual, Motorola Order Number ALTIVECPEM/D

PowerPC e500 Core Complex Reference Manual, Motorola Order Number E500CORERM/D

EREF: A Reference for Motorola Book E and the e500 Core, Motorola Order Number EREF/D

HOW TO REACH US:

USA/EUROPE/LOCATIONS NOT LISTED:

Motorola Literature Distribution
P.O. Box 5405, Denver, Colorado 80217
1-303-675-2140
(800) 441-2447

JAPAN:

Motorola Japan Ltd.
SPS, Technical Information Center
3-20-1, Minami-Azabu Minato-ku
Tokyo 106-8573 Japan
81-3-3440-3569

ASIA/PACIFIC:

Motorola Semiconductors H.K. Ltd.
Silicon Harbour Centre, 2 Dai King Street
Tai Po Industrial Estate, Tai Po, N.T., Hong Kong
852-26668334

TECHNICAL INFORMATION CENTER:

(800) 521-6274

HOME PAGE:

www.motorola.com/semiconductors

EB622/D

Freescale Semiconductor, Inc.