Reference Manual

DOC. REV. 9/8/2016

EBX-12

Pentium M® / Celeron M®
based SBC with Ethernet,
Video, Audio and Industrial I/O

Product Release Notes

Rev 7 Release

- Updated nominal battery voltage content

Rev 6 Release

- **Conformal Coated Models**. The conformal-coated EBX-12pr and tr models were released at revision 6.02.
- **RoHS Models**. RoHS-compliant versions were released, the EBX-12p, r, t and v. The first production release of these boards was revision 6.01.
- **USB Wiring Change**. The wiring of the USB circuits and cables was changed to improve USB performance and reduce susceptibility to noise.
- **RoHS Cables**. A RoHS-compliant cable kit was released, CKR-COBRA, which is equivalent to the non-RoHS CKT-COBRA. The RoHS kit includes a new cable assembly, CBR-8005.
- **BIOS**. Revisions 5.3.110 and 5.3.111 were released for Rev. 6.xx boards.

Rev 5 Release

- **PCB**. Multiple improvements, including LVDS connector J5 silkscreen correction.
- **BIOS**. Initially shipped with BIOS version 5.3.108. Updated to 5.3.109 for board revision 5.03.
- **CompactFlash**. New signals added to support faster transfer mode.
- **Revision Indicator Codes**. Updated.

Rev 4 Release

Production release.

Rev 3 Release

Charlie release only.

Rev 2 Release

Beta release only.

Rev 1 Release

Pre-production only. No customer releases.

Support Page

The **EBX-12 support page**, at **http://www.VersaLogic.com/private/cobrasupport.asp**, contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Operating system information and software drivers
- Data sheets and manufacturers' links for chips used in this product
- BIOS information and upgrades
- Utility routines and benchmark software

Note: This is a private page for EBX-12 users that can be accessed only be entering this address directly. It cannot be reached from the VersaLogic homepage.

Model EBX-12

Pentium M® / Celeron M® Based SBC with Ethernet,
Video, Audio and Industrial I/O

REFERENCE MANUAL

VERSALOGIC CORPORATION
WWW.VERSALOGIC.COM

4211 West 11th Ave.
Eugene, OR 97402
(541) 485-8575
Fax (541) 485-5712

Notice:

Although every effort has been made to ensure this document is error-free, VersaLogic makes no representations or warranties with respect to this product and specifically disclaims any implied warranties of merchantability or fitness for any particular purpose.

VersaLogic reserves the right to revise this product and associated documentation at any time without obligation to notify anyone of such changes.

PC/104 and the PC/104 logo are trademarks of the PC/104 Consortium.

Contents

Introduction 1

Description

The EBX-12 is a feature-packed single board computer designed for OEM control projects requiring fast processing, industrial I/O, flexible memory options and designed-in reliability and longevity (product lifespan). Its features include:

- Intel processors:
  - Pentium M 1.8 GHz with 2 MB cache
  - Pentium M 1.6 GHz with 1 MB cache
  - Celeron M 1.3 GHz with 512K cache
  - Celeron M ULV 1.0 GHz with 512K cache
- Up to 2 GB system RAM
- Intel 855GME chipset
- CompactFlash site
- 10/100 /1000 Ethernet interface (dual)
- Extreme Graphics
- Flat Panel Display support
- PC/104-*Plus* expansion site
- Dual ATA100 IDE controller
- Four USB 2.0 Ports.
- TVS devices
- PCI-based audio
- 4 COM + 1 LPT port
- CPU temperature sensor
- PS/2 keyboard and mouse ports
- Industrial I/O
  - Analog input option
  - 32 channel Digital I/O
  - Three spare 16-bit counter/timers
  - Two RS232/422/485 selectable COM ports
- Watchdog timer
- Vcc sensing reset circuit
- EBX-compliant 5.75” x 8.00” footprint
- Field upgradeable BIOS with OEM enhancements
- Latching I/O connectors
- Customizing available
- Three extra 8254-style timer/counters
- Urethane coated versions available

This EBX-compliant single board computer accepts Intel Pentium M® Processors. Processing speeds up to 1.8 GHz are available. The board is compatible with popular operating systems such as Windows, QNX, VxWorks and Linux.

A full complement of standard I/O ports is included on the board and on two “breakout” boards. Additional I/O expansion is available through the high-speed PCI-based PC/104-*Plus* expansion site (which supports both PC/104 and PC/104-*Plus* expansion modules).

System memory expansion is supported with two high-reliability latching 200-pin SODIMM sockets. Low power 2.5V 200-pin SODIMM modules up to 1 GB are available.

The EBX-12 features high reliability design and construction, including latching I/O connectors. It also features a watchdog timer, voltage sensing reset circuits and self-resetting fuse on the 5V supply to the keyboard, mouse and USB.

EBX-12 boards are subjected to 100% functional testing and are backed by a limited two-year warranty.

Technical Specifications

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

Board Size: 5.75" x 8.00" x 1.75"; EBX compliant
Storage Temperature: -40° C to 85° C
Free Air Operating Temperature:
0° C to +60° C EBX-12b, d, g, m, p, pr, r, v
-40° C to +85° C, EBX-12e, er, t, tr
-20° C to +85° C, EBX-12k
Power Requirements: *(with two 512 MB DDR SODIMMS, keyboard and mouse)*
- EBX-12b, bu – 1.6 GHz Pentium M® CPU
  5V ± 5% ≅ 4.6 A (23.0 W) typ.
- EBX-12d – 1.6 GHz Pentium M® CPU
  5V ± 5% ≅ 4.7 A (23.5 W) typ.
- EBX-12e, er, eu, t, tr – 1.0 GHz Pentium M® CPU
  5V ± 5% ≅ 2.3 A (11.5 W) typ. (with 512 MB DDR)
- EBX-12g – 1.3 GHz Celeron M® CPU
  5V ± 5% ≅ 4.6 A (23.0 W) typ.
- EBX-12k – 1.0 GHz Pentium M® CPU
  5V ± 5% ≅ 2.3 A (11.5 W) typ. (with 512 MB DDR)
- EBX-12m, p, pr, r – 1.8 GHz Pentium M® CPU
  5V ± 5% ≅ 4.6 A (23.0 W) typ.
- EBX-12v – 1.0 GHz ULV Celeron M® CPU
  5V ± 5% ≅ 2.3 A (10.5 W) typ. (with 512 MB DDR)

+3.3V or ±12V may be required by some expansion modules
System Reset:
V_{cc} sensing, resets below 4.70V typ.
Watchdog timeout
DRAM Interface:
Two 200-pin DDR SODIMM sockets
Up to 2 GB, 2.50V, non-parity, PC2700
Video Interface:
Intel Extreme Graphics 2, 855GME
3.3V LVDS flat panel display interface
CRT
IDE Interface:
Two-channel, 40-pin. 0.1" connectors. Supports up to and including UDMA5.
Supports up to four IDE devices (hard drives, CD-ROM, etc.).
Ethernet Interface:
- EBX-12b, bu, e, er, eu, g, k, m, p, pr, t, tr, v – two Intel 82551ER based Fast Ethernet Controllers
- EBX-12d, du r – two Intel 82541ER based Gigabit Ethernet Controllers

Audio Interface:
Standard Line Out and Line In support
Analog Input (optional):
8-channel, 12-bit, single-ended, 6 microsecond, channel independent input ranges:
±5, ±10, 0 to +5V, 0 to +10V. Option available for HDW-301 and HDW-302 (extended temp. version).
COM1–2 Interface:
RS-232, 16C550 compatible, 115k baud max.
COM3–4 Interface:
RS-232/422/485, 16C550 compatible, 460k baud max.
LPT Interface:
Bi-directional/EPP/ECP compatible. Floppy disk interface with CBL/CBR-2501.
Digital Interface:
32-channel, ±24 mA outputs
BIOS:
General Software Embedded BIOS© 2000 with OEM enhancements
Field-upgradeable with Flash BIOS Upgrade Utility
Bus Speed:
CPU Bus: 400MHz
DRAM: 200 MHz/266 MHz/333 MHz
PC/104-*Plus* (PCI): 33MHz
PC/104 (ISA): 8MHz
Compatibility:
PC/104 – full compliance
Embedded-PCI (PC/104-*Plus*) – full compliance, 3.3V signaling
EBX – full compliance
Weight:
EBX-12b, d, e, er, g, k – 0.32 kg (0.72 lbs)
EBX-12bu, du, eu – 0.34 kg (0.74 lbs)
EBX-12m – 0.31 kg (0.68 lbs)
EBX-12p, pr, t, tr, v – 0.30 kg (0.66 lbs)
EBX-12r – 0.29 kg (0.65 lbs)
Generated Frequencies:
166, 133, or 100 MHz (memory), 125 MHz, 33.3 MHz, 25 MHz, 24.576 MHz, 14.318 MHz, 8.25 MHz, 2.5 MHz, 350 kHz, 32.768 kHz

Specifications are subject to change without notice.

EBX-12 Block Diagram

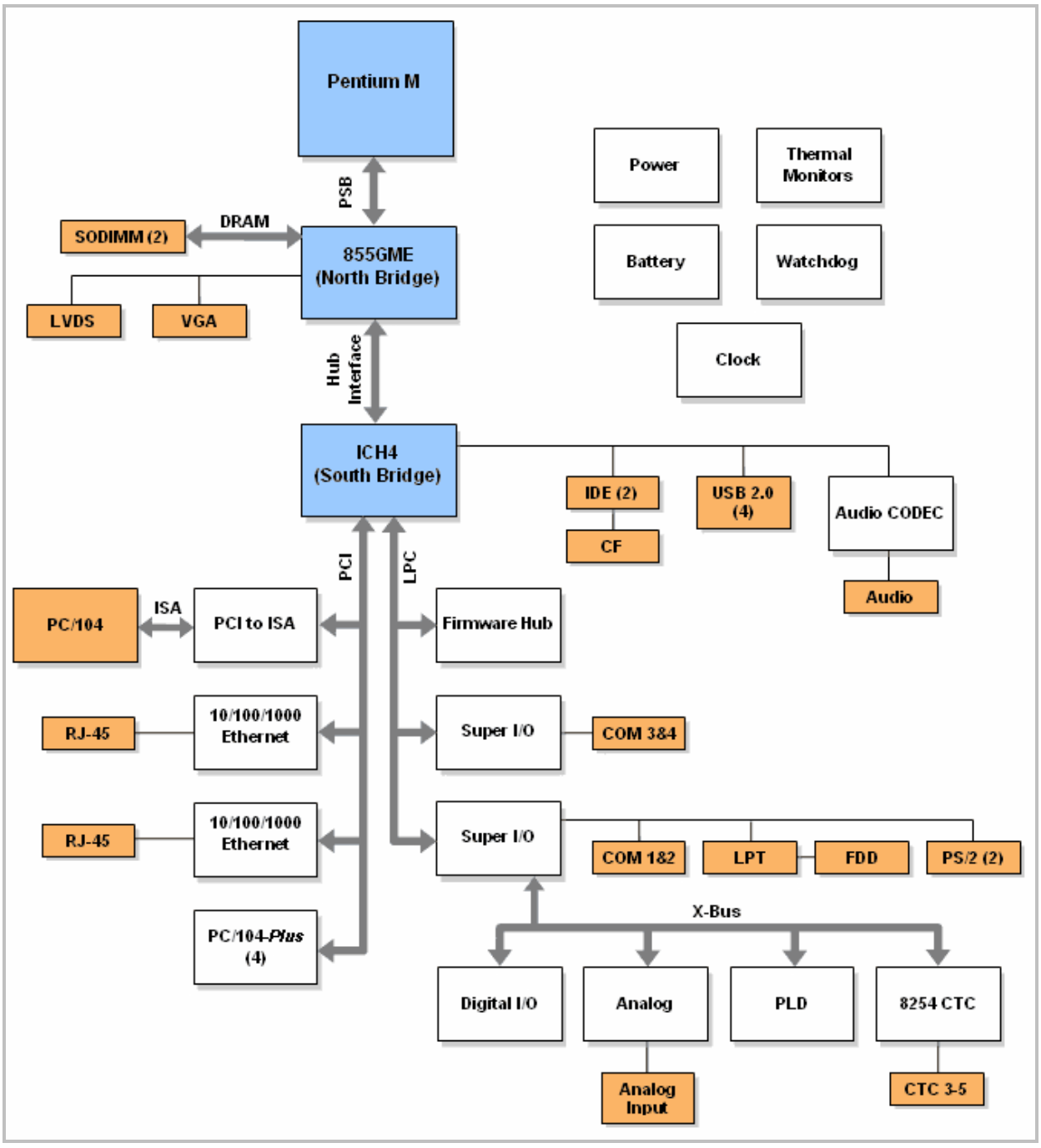


Figure 1. EBX-12 Block Diagram

Technical Support

If you are unable to solve a problem with this manual please visit the EBX-12 Product Support web page at **http://www.VersaLogic.com/private/cobrasupport.asp**. If you have further questions, contact VersaLogic technical support at (541) 485-8575. VersaLogic technical support engineers are also available via e-mail at Support@VersaLogic.com.

EBX-12 Support Website

http://www.VersaLogic.com/private/cobrasupport.asp

REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (541) 485-8575. VersaLogic's standard turn-around time for repairs is five working days after the product is received.

Please provide the following information:

- Your name, the name of your company and your phone number
- The name of a technician or engineer that can be contact if any questions arise.
- Quantity of items being returned
- The model and serial number (barcode) of each item
- A detailed description of the problem
- Steps you have taken to resolve or recreate the problem
- The return shipping address

Warranty Repair All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair All non-warranty repairs are subject to diagnosis and labor charges, parts charges and return shipping fees. Please specify the shipping method you prefer and provide a purchase order number for invoicing the repair.

Note: Please mark the RMA number clearly on the outside of the box before returning. Failure to do so can delay the processing of your return.

RoHS-Compliance

The EPM-12p, pr, r, t, tr and v are RoHS-compliant.

ABOUT ROHS

In 2003, the European Union issued Directive 2002/95/EC regarding the Restriction of the use of certain Hazardous Substances (RoHS) in electrical and electronic equipment.

The RoHS directive requires producers of electrical and electronic equipment to reduce to acceptable levels the presence of six environmentally sensitive substances: lead, mercury, cadmium, hexavalent chromium, and the presence of polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) flame retardants, in certain electrical and electronic products sold in the European Union (EU) beginning July 1, 2006.

VersaLogic Corporation is committed to supporting customers with high-quality products and services meeting the European Union's RoHS directive.

Configuration / Operation 2

Overview

ELECTROSTATIC DISCHARGE

Warning! Electrostatic discharge (ESD) can damage boards, disk drives and other components. The circuit board must only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an antistatic foam pad if available.

The board should also be protected inside a closed metallic anti-static envelope during shipment or storage.

Note: The exterior coating on some metallic antistatic bags is sufficiently conductive to cause excessive battery drain if the bag comes in contact with the bottom-side of the EBX-12.

LITHIUM BATTERY

Warning! To prevent shorting, premature failure or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble or dispose of in fire. Dispose of used batteries promptly.

MOUNTING SUPPORT

Warning! The single board computer must be supported at all eight mounting points to prevent excessive flexing when expansion modules are mated and demated. Flex damage caused by excessive force on an improperly mounted circuit board is not covered under the product warranty. See page 11 for more details.

Initial Configuration and Setup

The following list describes the recommended components and gives an abbreviated outline for setting up a typical development system.

RECOMMENDED COMPONENTS

- EBX-12 Single Board Computer
- 200-pin SODIMM DDR200, DDR266 or DDR333
- ATX Power Supply
- SVGA Video Monitor
- Keyboard with PS2 Connector
- LPT 3.5" Floppy Disk Drive (optional)
- IDE Hard Drive (optional)
- IDE CD ROM Drive (optional)

DRAM MODULE

- Insert DRAM module into the SODIMM socket and latch into place.

CABLES / PERIPHERAL DEVICES

- Plug video adapter cable (p/n CBL/CBR-1007) into socket J7, and attach video monitor.
- Plug breakout board (p/n CBL-8003 or CBR-8005) into socket J4, and attach keyboard to the PS/2 connector (J2) of breakout board.
- Plug floppy data cable (p/n CBL/CBR-2501) into LPT port, and attach floppy drive.
- Plug hard drive data cable (p/n CBL/CBR-4003) into socket J6 and attach hard drive and CD-ROM drive to the connectors at the opposite end of the cable.
- Plug power adapter cable (p/n CBL/CBR-2022) into socket J2, and attach ATX power supply.
- Attach power supply cables to external drives.
- Set hard drive jumpers for master device operation.

CMOS Setup / Boot Procedure Preliminary

To enter CMOS Setup, turn on the power and press the DEL key the instant that video is displayed (during the memory test). The default CMOS Setup parameters are shown below. See table below. See VersaLogic Knowledgebase article VT1456 – EBX-12 CMOS Setup Reference for more information about these parameters.

Basic CMOS Configuration

```
+-------------------------------------------------------------------------+
|                System Bios Setup - Basic CMOS Configuration             |
|           (C) 2004 General Software, Inc. All rights reserved           |
+--------------------------+------------------+---------------------------+
| DRIVE ASSIGNMENT ORDER:  | Date:>Nov 03, 2010 | Typematic Delay  : 250 ms  |
| Drive A: (None)          | Time: 00 : 00 : 00 | Typematic Rate   : 30 cps  |
| Drive B: (None)          | NumLock:  Disabled | Seek at Boot     : Floppy  |
| Drive C: Ide 0/Pri Master +--------------------+ Show "Hit Del"   : Enabled |
| Drive D: (None)          | BOOT ORDER:        | Config Box       : Enabled |
| Drive E: (None)          | Boot 1st: Drive C: | F1 Error Wait    : Enabled |
| Drive F: (None)          | Boot 2nd: (None)   | Parity Checking  : (Unused)|
| Drive G: (None)          | Boot 3rd: (None)   | Memory Test Tick : Enabled |
| Drive H: (None)          | Boot 4th: (None)   | Debug Breakpoints: (Unused)|
| Drive I: (None)          | Boot 5th: (None)   | Debugger Hex Case: Upper   |
| Drive J: (None)          | Boot 6th: (None)   | Memory Test :StdLo FastHi  |
| Drive K: (None)          +--------------------+-----------------+----------+
| Boot Method: Boot Sector | ATA DRV ASSIGNMENT:  Sect  Hds  Cyls | Memory   |
+--------------------------+ Ide 0: 3 = AUTOCONFIG, LBA           |  Base:   |
| FLOPPY DRIVE TYPES:      | Ide 1: Not installed                 |   633KB  |
| Floppy 0: Not installed  | Ide 2: Not installed                 |  Ext:    |
| Floppy 1: Not installed  | Ide 3: Not installed                 |  1011MB  |
+--------------------------+--------------------------------------+----------+
```

Custom Configuration

```
+-------------------------------------------------------------------------+
|                System BIOS Setup - Advanced Configuration               |
|           (C) 2004 General Software, Inc. All rights reserved           |
+-----------------------------------+-------------------------------------+
| BIOS Extension           : Disabled | COM1 (0x3F8)Enable/IRQ    : IRQ4    |
| Legacy USB and Booting   : Enabled  | COM2 (0x2F8)Enable/IRQ    : IRQ3    |
| COM3 (0x3E8) Mode        : RS-232   | COM3 (0x3E8)Enable/IRQ    : Disabled|
| COM4 (0x2E8) Mode        : RS-232   | COM4 (0x2E8)Enable/IRQ    : Disabled|
| Parallel Port Mode       : SPP      | LPT1 (0378) Enable/IRQ    : IRQ7    |
| BCR Base Address         : 0x1D0    | Mouse Enable/IRQ          : IRQ12   |
| CPU Temperature Threshold : 70°C    | Digital I/O 30            : No IRQ  |
| Processor Speed          : 1800 MHz | Digital I/O 31            : No IRQ  |
| Display Type             : CRT      | A/D Conversion Done       : No IRQ  |
| LVDS Flat Panel          : 640x480  | PCI INT A                 : IRQ11   |
| LVDS Flat Panel Fitting  : Stretch  | PCI INT B                 : IRQ11   |
| Video Memory             : 8 MB     | PCI INT C                 : IRQ11   |
| Splash Screen            : Disabled | PCI INT D                 : IRQ11   |
| Audio                    : Enabled  | PC/104-Plus Slot Disable  : None    |
| USB                      : Enabled  | Pri/Sec IDE Cable Types   : 40/40Wire|
| Ethernet Disable         : None     | PCI Option ROM Disable    : None    |
| Write Protect BIOS       : Disabled | Primary Video Controller  : Detect  |
+-----------------------------------+-------------------------------------+
```

Shadow Configuration

```
+-------------------------------------------------------------------------+
|                System BIOS Setup - Shadow/Cache Configuration           |
|           (C) 2004 General Software, Inc. All rights reserved           |
+-----------------------------------+-------------------------------------+
| Shadowing                : Chipset  | Shadow 16KB ROM at C000   : Enabled |
| Shadow 16KB ROM at C400  : Enabled  | Shadow 16KB ROM at C800   : Enabled |
| Shadow 16KB ROM at CC00  : Enabled  | Shadow 16KB ROM at D000   : Disabled|
| Shadow 16KB ROM at D400  : Disabled | Shadow 16KB ROM at D800   : Disabled|
| Shadow 16KB ROM at DC00  : Disabled | Shadow 16KB ROM at E000   : Enabled |
| Shadow 16KB ROM at E400  : Enabled  | Shadow 16KB ROM at E800   : Enabled |
| Shadow 16KB ROM at EC00  : Enabled  | Shadow 64KB ROM at F000   : Enabled |
+-----------------------------------+-------------------------------------+
```

Note: Due to system configuration and changes between BIOS revisions, the information on your monitor may differ from that shown above. The date shown on the Basic CMOS Configuration screen is the BIOS build date.

Operating System Installation

The standard PC architecture used on the EBX-12 makes the installation and use of most of the standard x86 processor-based operating systems very simple. The operating systems listed on the VersaLogic OS Compatibility Chart use the standard installation procedures provided by the maker of the OS, unless otherwise noted. Special optimized hardware drivers for a particular operating system, or a link to the drivers, are available at the EBX-12 Product Support web page at **http://www.VersaLogic.com/private/cobrasupport.asp.**

Dimensions and Mounting

The EBX-12 complies with all EBX standards which provide for specific mounting hole and PC/104-*Plus* stack locations as shown in the diagram below.

EBX-12 Dimensions and Mounting

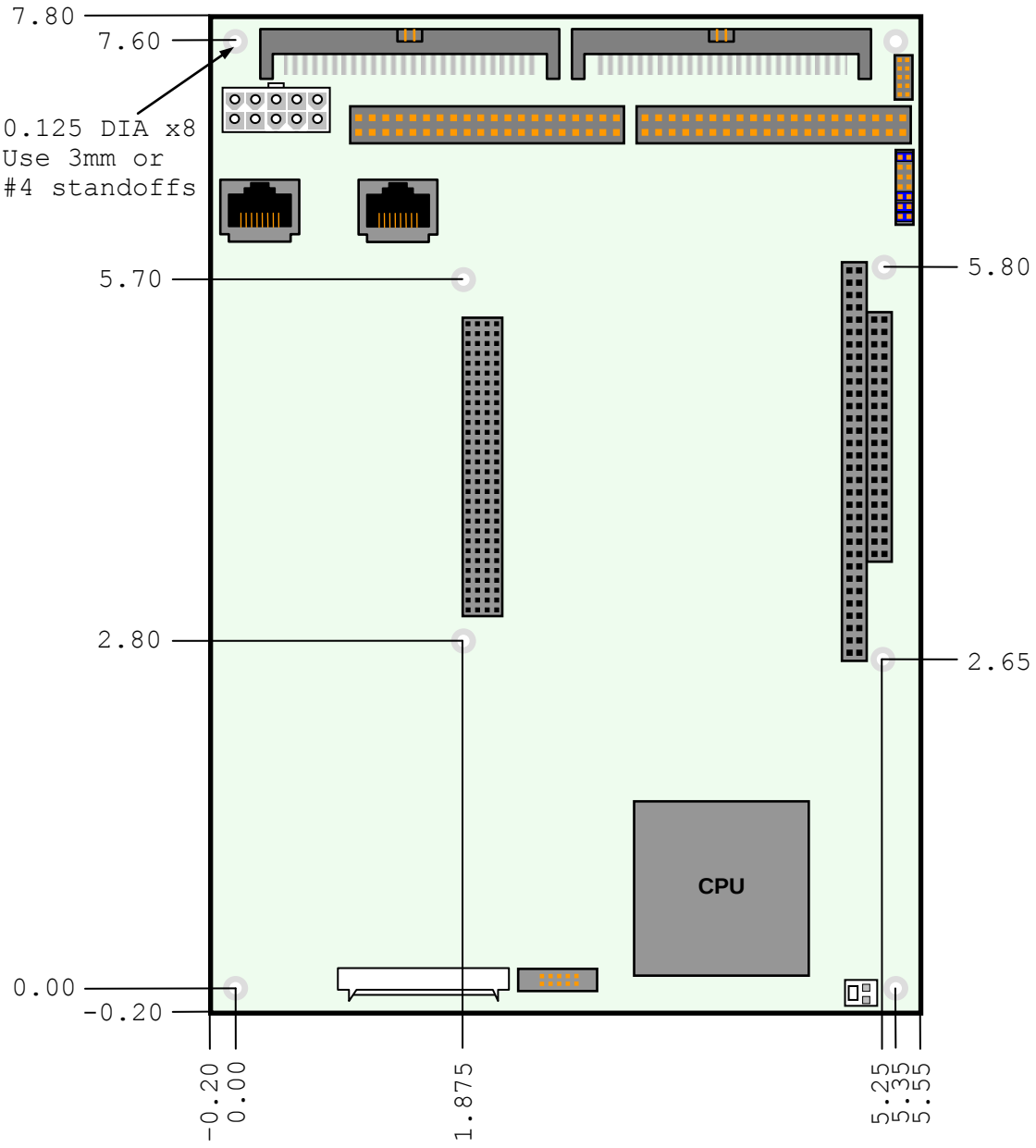


Figure 2. Dimensions and Mounting Holes
(Not to scale. All dimensions in inches.)

Caution The single board computer must be supported at all eight mounting points to prevent excessive flexing when expansion modules are mated and demated. Flex damage caused by excessive force on an improperly mounted circuit board is not covered under the product warranty.

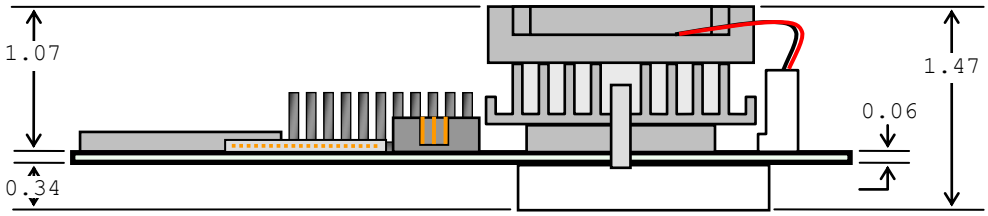


Figure 3. Height Dimensions (Non-pass-through)
(Not to scale. All dimensions in inches.)

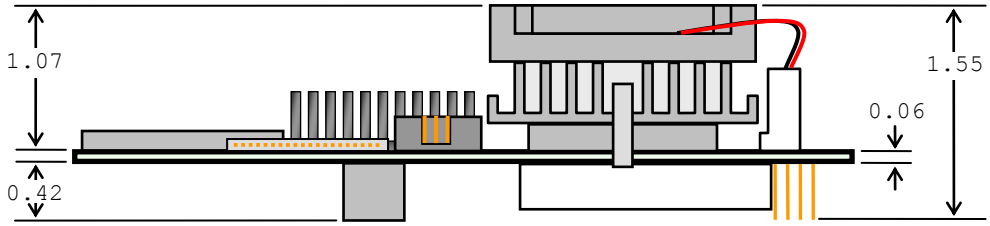


Figure 4. Height Dimensions (Pass-through)
(Not to scale. All dimensions in inches.)

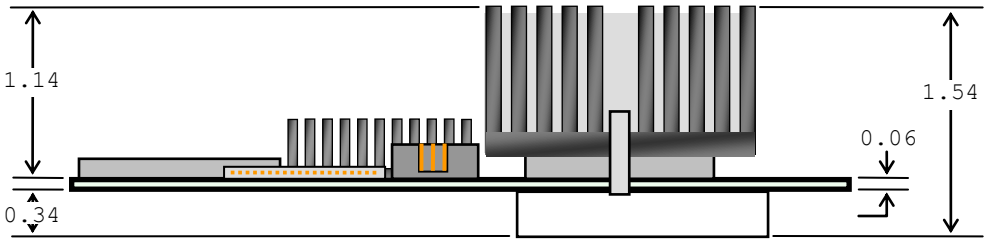


Figure 5. Height Dimensions (Fanless)
(Not to scale. All dimensions in inches.)

BREAKOUT BOARD DIMENSIONS AND MOUNTING

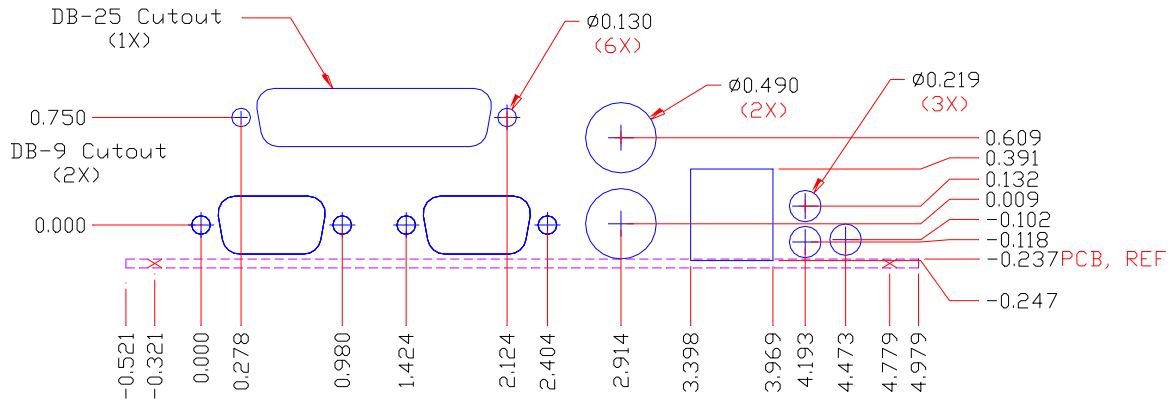


Figure 6. CBL-8003 and CBR-8005 Dimensions and Mounting

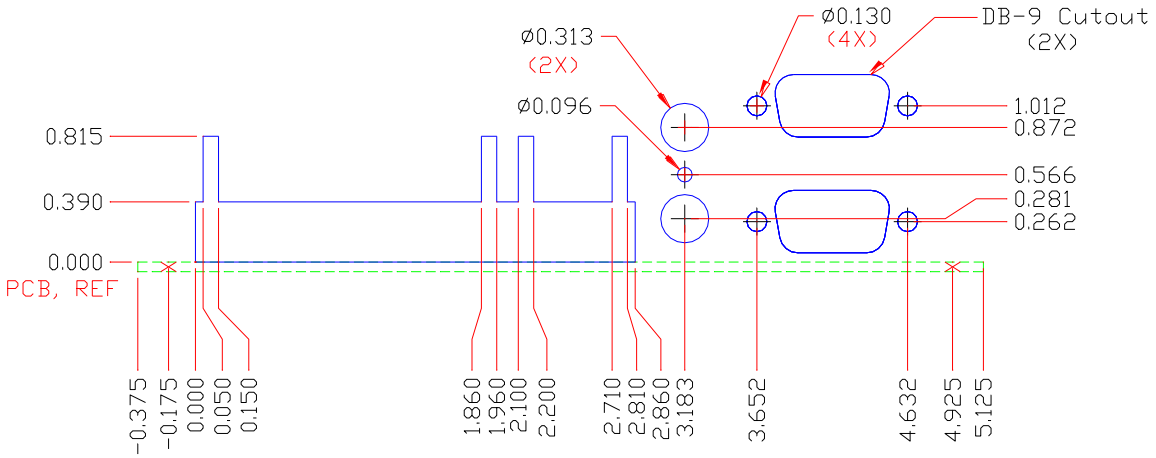


Figure 7. CBL/CBR-8004 Dimensions and Mounting

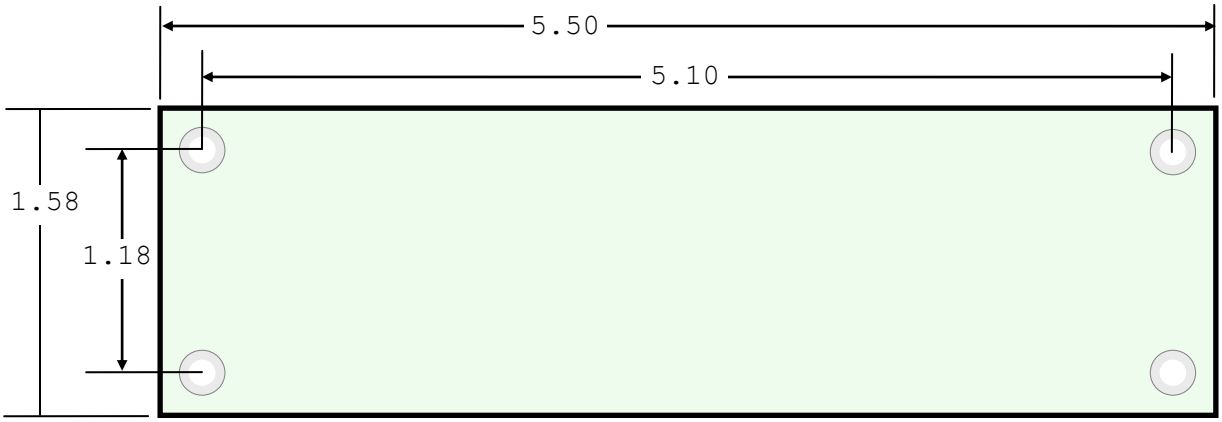


Figure 8. Breakout Board Dimensions

HARDWARE ASSEMBLY

The EBX-12 mounts on four hardware standoffs using the corner mounting holes (A). These standoffs are secured to the underside of the circuit board using pan head screws.

Four additional standoffs (B) must be used under the circuit board to prevent excessive flexing when expansion modules are mated and demated. These are secured with four male-female standoffs (C), threaded from the top side, which also serve as mounting struts for the PC/104 stack.

The entire assembly can sit on a table top or be secured to a base plate. When bolting the unit down, make sure to secure all eight standoffs (A and B) to the mounting surface to prevent circuit board flexing. See page 11 for dimensional details.

An extractor tool is available (part number VL-HDW-201) to separate the PC/104 modules from the stack.

Note: Standoffs and screws are available as part number VL-HDW-101.

STANDOFF LOCATIONS

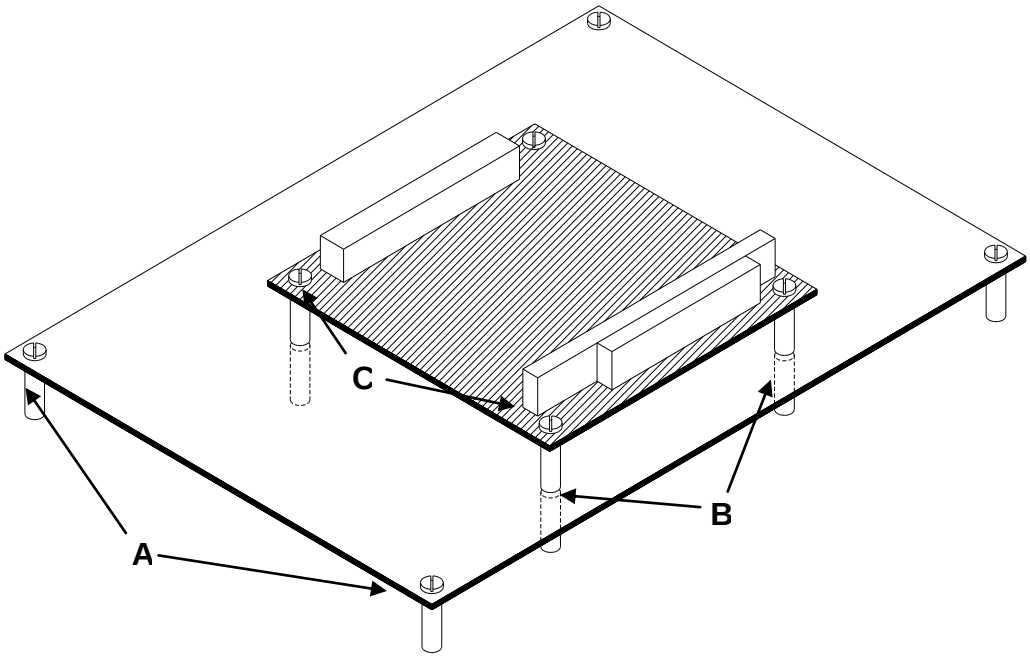


Figure 9. Standoff Locations

External Connectors

EBX-12 Connectors – Top Side

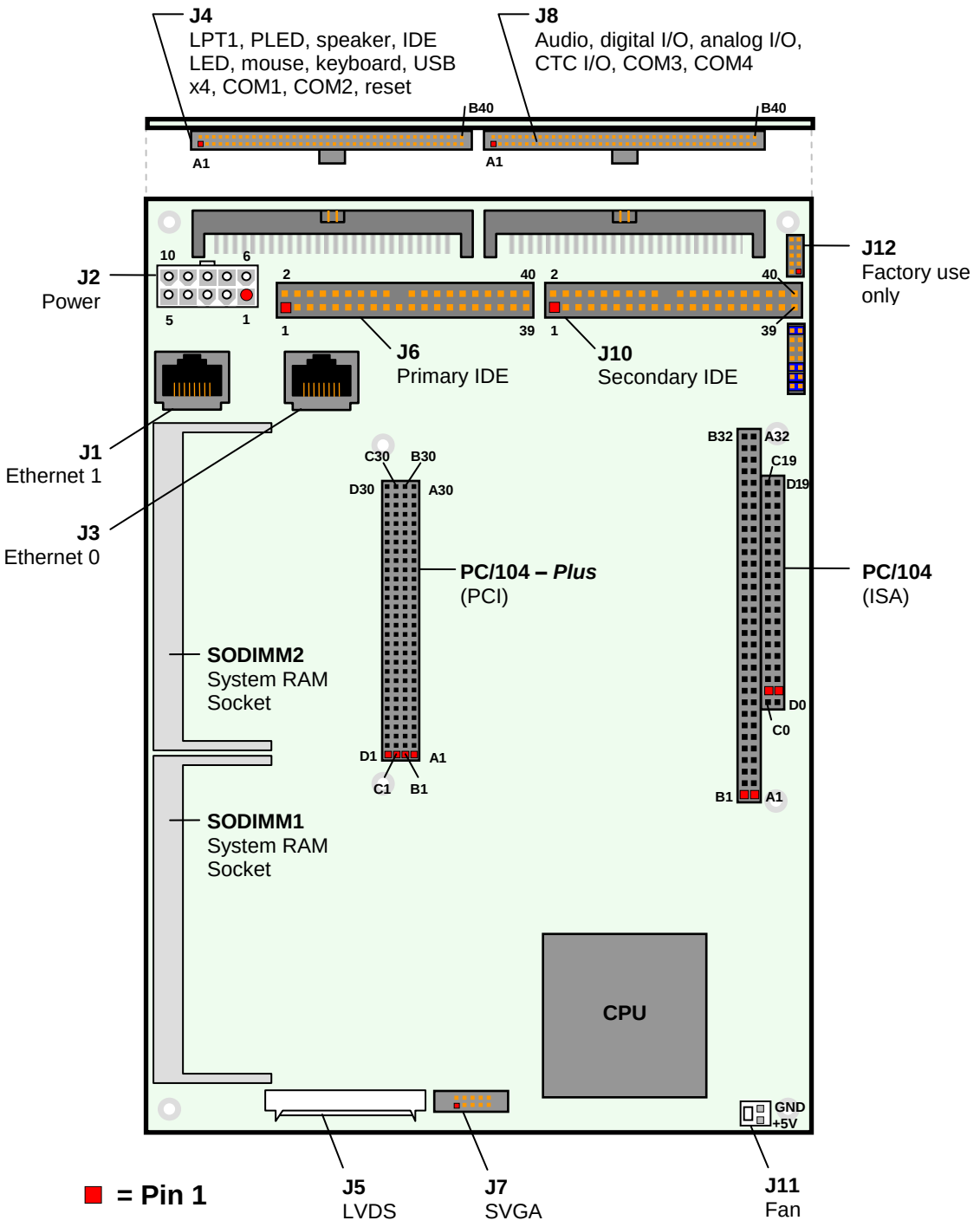


Figure 10. EBX-12 Connector Locations – Top

EBX-12 CONNECTORS – BOTTOM SIDE

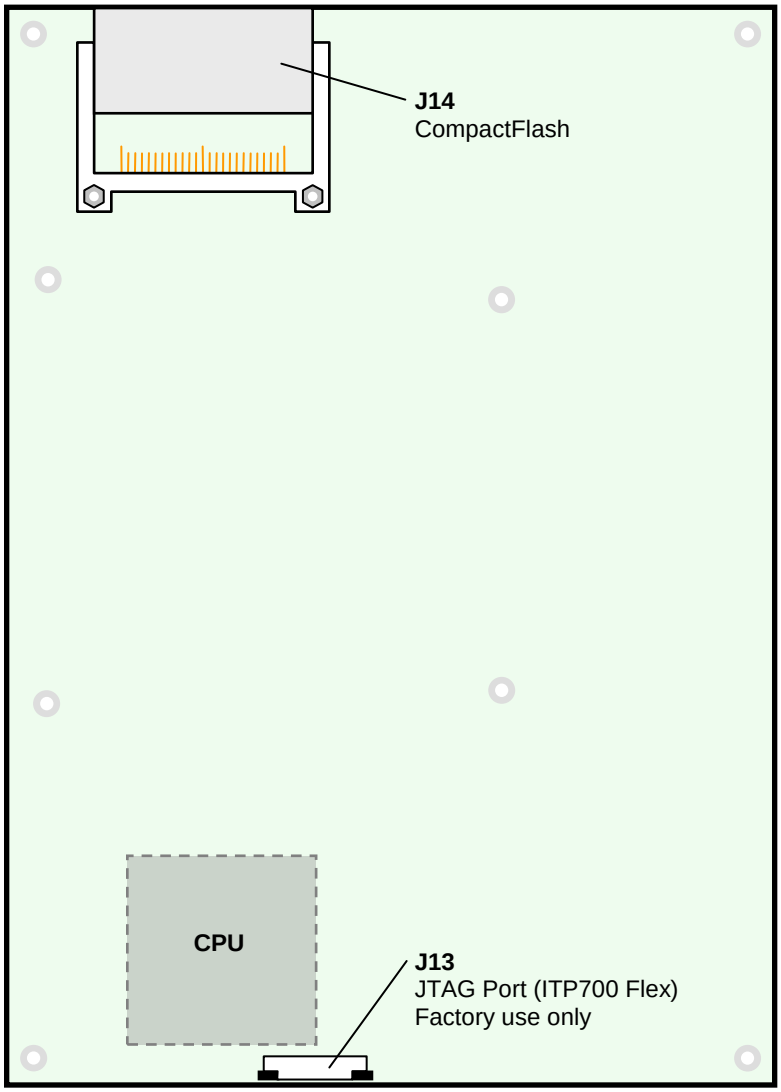


Figure 11. EBX-12 Connector Locations – Bottom

EBX-12 Connector Functions and Interface Cables

The following table notes the function of each connector, as well as mating connectors and cables, and the page where a detailed pinout or further information is available.

Note: Most VersaLogic adapter cables are available in RoHS compliant and RoHS noncompliant versions. Compliance or noncompliance is indicated by the part number prefix. "CBR" indicates RoHS compliance. "CBL" indicates RoHS noncompliance. For applications that do not require RoHS compliance, either cable can be used.

Table 1: Connector Functions and Interface Cables

Connector[1]	Function	Mating Connector	Transition Cable	Cable Description	Page
J1	Ethernet 1	RJ-45 Crimp-on Plug	—	—	47
J2	Main Power Input (EBX Compliant)	Molex 39-01-2100 + Molex 39-00-0059 (10ea.)	CBL/CBR-2022	0.5 foot ATX to EPIC power cable	25
J3	Ethernet 0	RJ-45 Crimp-on Plug	—	—	47
J4	LPT1, COM1, COM2, USB 0-3, Keyboard, PS/2 Mouse, Speaker, IDE LED, Reset Button, Program-mable LED	AMP 104892-8 AMP 104891-8	CBL-8003 or CBR-8005[3]	1.5 foot dual 40-pin cable with "breakout board"	19
J5	Flat Panel	Molex 51146-2000	—	—	43
J6[2]	IDE Hard Drive Channel 0	3M 3417-7600	CBL/CBR-4003	1.5 foot 40-pin dual IDE drive interface cable ATA 100	29
J7	SVGA Video Output	2mm 10-pin	CBL/CBR-1007	1 foot 10-pin socket to 15-pin D-sub SVGA connector	42
J8	Analog I/O, CTC I/O, Digital I/O, Audio, COM3, COM4	AMP 104892-8 AMP 104891-8	CBL/CBR-8004	1.5 foot dual 40-pin cable with "breakout board"	21
J10	IDE Hard Drive Channel 1	3M 3425-7600	CBL/CBR-4003	1.5 foot 40-pin dual IDE drive interface cable ATA 100	29
J11	Fan Power Output (+5V)	Molex 22-01-3027 or Molex 22-01-2025	Provided with fan assembly	—	—
J12	PLD Reprogramming Port *(Factory use Only)*	—	—	—	—
J13	JTAG Port (ITP700 Flex)	0.020" pitch FFC/FPL	—	—	—
J14	Compact Flash	Type I or Type II Compact Flash	—	—	29

1. Contact the factory for connector pin 1 locations.
2. These standard 0.100" dual-row low profile headers are 3M 2500 series compatible. They are also compatible with 3M polarizing posts and keys.
3. CBL-8003 and CBR-8005 are not interchangeable. Be sure to use CBL-8003 with EBX-12 version 5.xx and earlier, and CBR-8005 with EBX-12 version 6.xx and later.

CBL-8003 AND CBR-8005 CONNECTORS

The CBL-8003 and CBR-8005 breakout boards provide the following ports for the EBX-12:

- Parallel
- Serial (COM1 and COM2)
- PS/2 (for keyboard and mouse)
- USB (four devices, two "A" connectors and one dual-row 10-pin header)

The breakout board also includes a programmable LED, IDE LED, reset button, and external speaker. (See page 41 for a description of these devices.) To connect devices to any of these ports, you must connect the 80-pin connector of the transition cable to connector J4 on the EBX-12 and the two 40-pin connectors to JP1 and JP2 of the breakout board, then plug the devices into the appropriate connector on the breakout board.

CBL-8003 and CBR-8005 are NOT interchangeable. Be sure to use CBL-8003 with EBX-12 version 5.xx and earlier, and CBR-8005 with EBX-12 6.xx and later. Using the incorrect breakout board will cause the USB interface to fail and may cause damage to the circuitry.

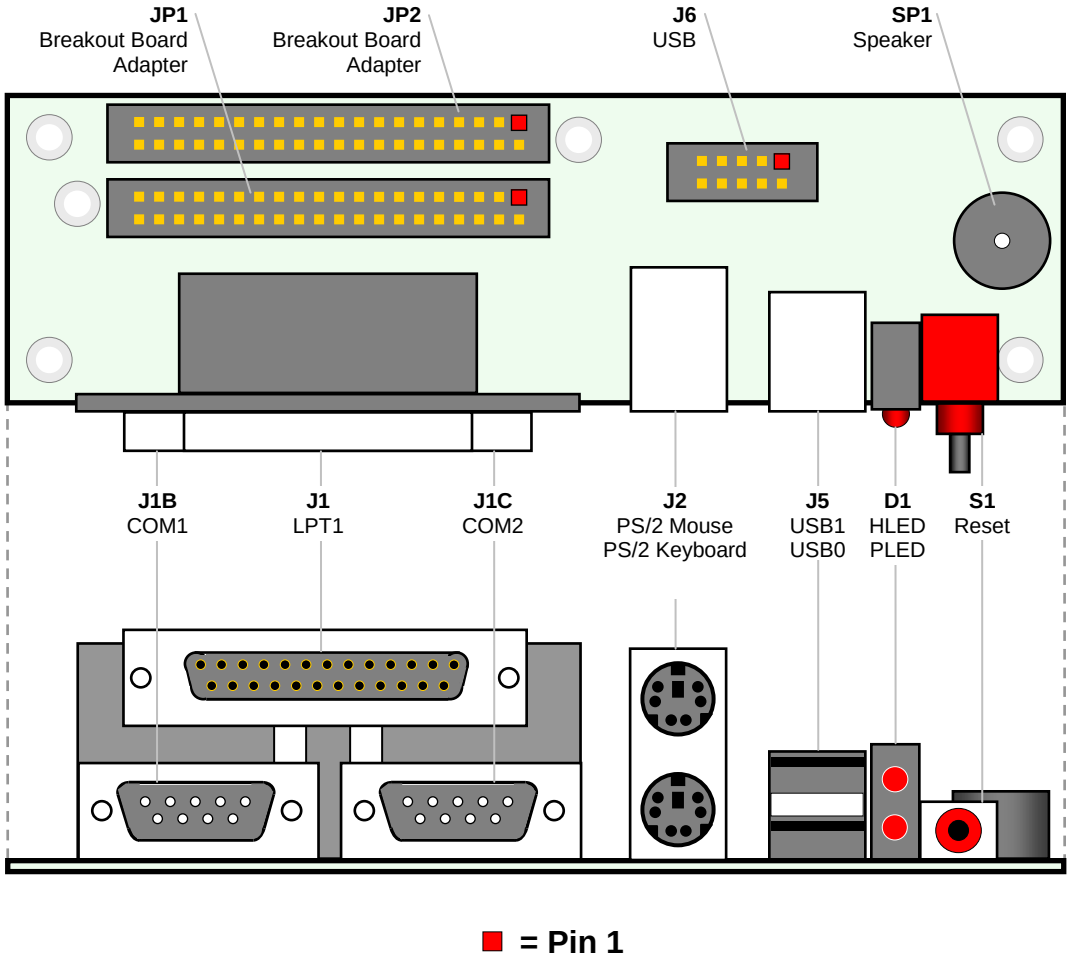


Figure 12. CBL-8003 and CBR-8005 Connector Locations

Note: The two 40-pin connectors are keyed so that they can be attached only in the correct orientation. The red stripe on the cables correlates to pin 1 of the connectors. Do not cross the cables when connecting them to JP1 and JP2.

Table 2: CBL-8003 and CBR-8005 Connector Functions and Interface Cables

Connector	Function	Mating Connector	Transition Cable	Cable Description	Page
JP1	Breakout Board Adapter 1	40-pin IDC female	A-C80034 for CBL-8003, or CBR-8004A for CBR-8005	1.5 foot dual 40-pin transition cable	–
JP2	Breakout Board Adapter 2	40-pin IDC female	A-C80034 for CBL-8004, or CBR-8004A for CBR-8004	1.5 foot dual 40-pin transition cable	–
J1A	LPT	DB25 male	–	–	39
J1B-C	COM1, COM2	DB9 female	–	–	34
J2	PS/2 x 2 – Keyboard, Mouse	PS/2 male	–	–	40
J5	USB “A” x 2	USB A male	–	–	58
J6	USB 10-pin header	10-pin female	–	–	58

CBL/CBR-8004 CONNECTORS

The CBL/CBR-8004 breakout board provides the following ports for the EBX-12:

- Audio-In, Audio-Out (Stereo)
- Digital I/O
- Analog I/O
- Serial Ports (COM3 and COM4)
- Auxiliary Timer/Counter Channels (CTC I/O)

To connect devices to any of these ports, you must connect the 80-pin connector of the A-C80034 transition cable to connector J8 on the EBX-12 and the two 40-pin connectors to JP1 and JP2 of the breakout board, then plug the devices into the appropriate connector on the breakout board.

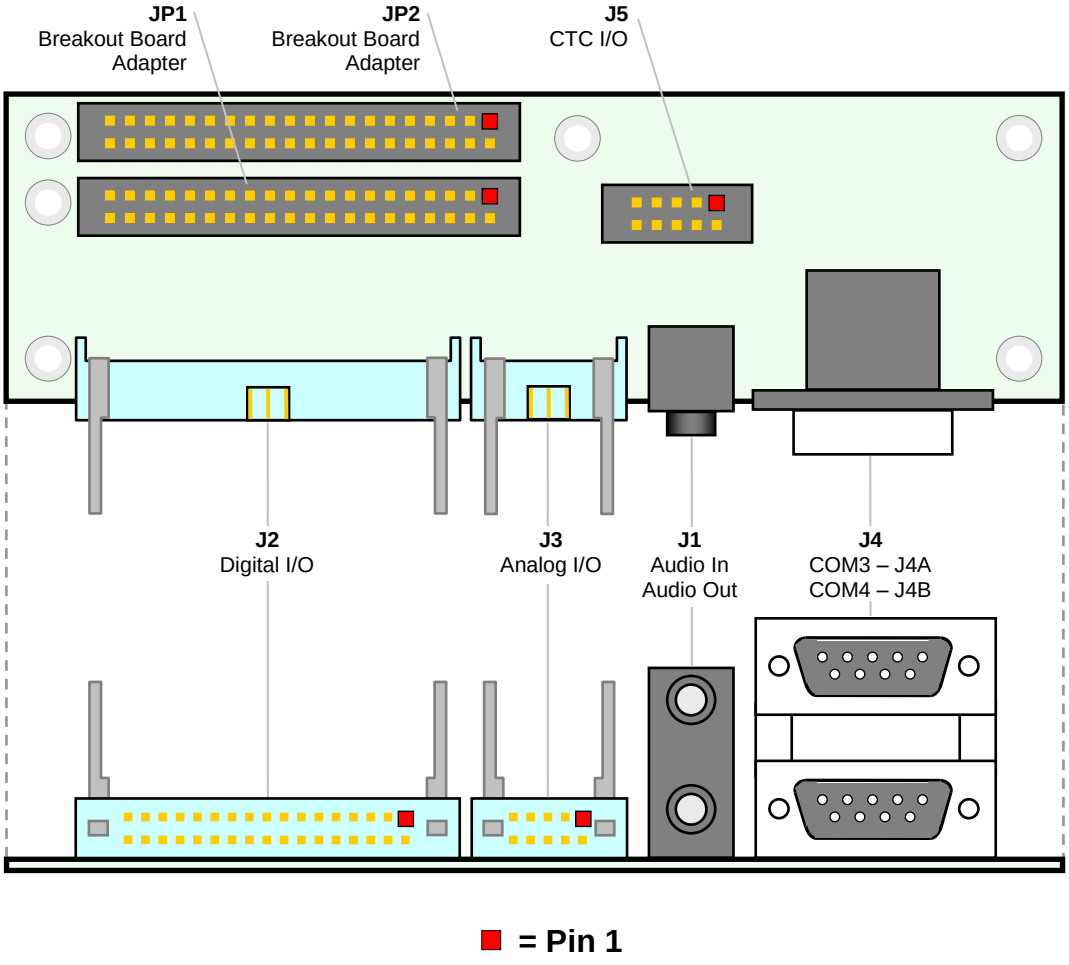


Figure 13. Connector Location Diagram CBL/CBR-8004 Front View

Note: The two 40-pin connectors are keyed so that they can be attached only in the correct orientation. The red stripe on the cables correlates to pin 1 of the connectors. Do not cross the cables when connecting them to JP1 and JP2.

Table 3: CBL/CBR-8004 Connector Functions and Interface Cables

Connector	Function	Mating Connector	Transition Cable	Cable Description	Page
JP1	Breakout Board Adapter 1	40-pin IDC female	A-C80034 for CBL-8004, or CBR-8004A for CBR-8004	1.5 foot dual 40-pin transition cable	–
JP2	Breakout Board Adapter 2	40-pin IDC female	A-C80034 for CBL-8004, or CBR-8004A for CBR-8004	1.5 foot dual 40-pin transition cable	–
J1	Audio-In (Top), Audio-Out (Bottom)	2 mm Audio Jack	–	–	48
J2	Digital I/O	CA-34FID-A-SPT 34-pin female	–	–	60
J3	Analog I/O	3M 3473-7600 10-pin female	–	–	51
J4	COM3, COM4	DB9 female	–	–	34
J5	CTC I/O	10-pin female	–	–	62

Jumper Blocks

JUMPERS AS-SHIPPED CONFIGURATION.

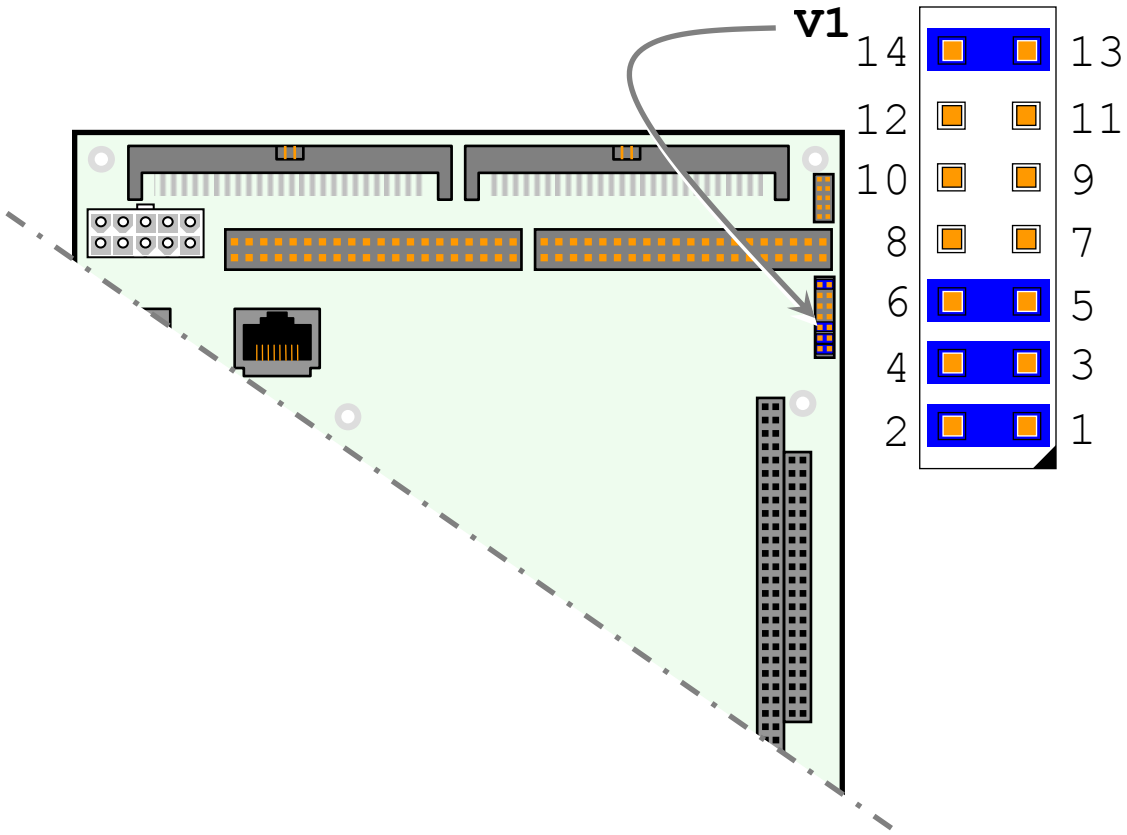


Figure 14. Jumper Block Location

JUMPER SUMMARY

Table 4: Jumper Summary

Jumper Block	Description	As Shipped	Page
V1[1-2]	**System BIOS Selector** In – Run time system BIOS selected Out – Master system BIOS selected. ***Note:*** *The Run time System BIOS is field upgradeable using the BIOS upgrade utility. See www.VersaLogic.com/private/cobrasupport.asp for further information.*	In	—
V1[3-4]	**Video BIOS Selector** In – Primary Video BIOS selected Out – Secondary Video BIOS selected ***Note:*** *The secondary Video BIOS is field-upgradeable using the BIOS upgrade utility. See www.VersaLogic.com/private/cobrasupport.asp for further information*	In	42
V1[5-6]	**General Purpose Input 1** In – CPU reads bit as 1 Out – CPU reads bit as 0	In	—
V1[7-8]	**CMOS RAM and Real Time Clock Erase** In – Erase CMOS RAM and Real-Time Clock Out – Normal	Out	27
V1[9-10]	**COM3 RS-422/485 Endpoint Termination** In – Endpoint Termination Enabled Out – Endpoint Termination Disabled	Out	33
V1[11-12]	**COM4 RS-422/485 Endpoint Termination** In – Endpoint Termination Enabled Out – Endpoint Termination Disabled	Out	33
V1[13-14]	**Compact Flash Master/Slave selection** In – Master Out – Slave	In	29

Power Supply

POWER CONNECTORS

Main power is applied to the EBX-12 through an EPIC-style 10-pin polarized connector.

See page 16 for connector pinout and location information.

Warning! To prevent severe and possibly irreparable damage to the system, it is critical that the power connectors are wired correctly. Make sure to use both +5VDC pins and all ground pins to prevent excess voltage drop.

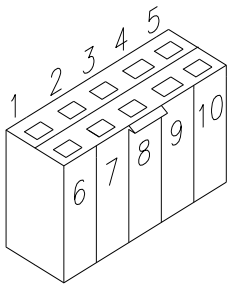


Table 5: Main Power Connector Pinout

J2 Pin	Signal Name	Description
1*	GND	Ground
2	GND	Ground
3	GND	Ground
4	+12VDC	Power Input
5	+3.3VDC	Power Input
6**	NC	Not Connected
7	+5VDC	Power Input
8	+5VDC	Power Input
9	-12VDC	Power Input
10	GND	Ground

** Pin 1 is typically used in EPIC-style power cables as a PS-ON # signal. Since the EBX-12 does not support soft-off, pin 1 is internally connected to ground.*

*** Pin 6 is typically used in EPIC style power cables as a 5VSB (5V Stand By) signal. Since the EBX-12 does not support soft-off, pin 6 is an internal no connect.*

Note: The +3.3VDC, +12VDC and -12VDC inputs on the main power connector are only required for PC/104-*Plus* and PC/104 expansion modules that require the voltages.

POWER REQUIREMENTS

The EBX-12 requires only +5 volts (±5%) for proper operation. The voltage required for the RS-232 ports and analog input sections are generated with a DC/DC converter. A variable low-voltage supply circuit provides power to the CPU and other on-board devices.

The exact power requirement of the EBX-12 depends on several factors, including memory configuration, CPU speed, peripheral connections, type and number of expansion modules and attached devices. For example, PS/2 keyboards typically draw their power directly from the EBX-12, and driving long RS-232 lines at high speed can increase power demand.

LITHIUM BATTERY

Warning! To prevent shorting, premature failure or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble or dispose of in fire. Dispose of used batteries promptly.

Nominal battery voltage is 3.0V. If the voltage drops below 2.7V, contact the factory for a replacement (part number HB3/0-1). The life expectancy under normal use is approximately 10 years.

Note: The EBX-12 is designed to boot even with a dead or removed battery. See page 28 for further information.

CPU

PROCESSOR REPLACEMENT

Removal or replacement of the CPU is not recommended; doing so may damage the CPU. These CPUs have the chip dies mounted on a thin substrate. If the substrate is flexed too far, damage will occur to the die bonds. Such damage will not be covered under the board warranty. The CPU on is soldered down on some models, so removal is not possible.

CPU SPEED

The processor speed can be changed using CMOS Setup. The speed options available are 600 MHz, 800 MHz, 1000 MHz, 1200 MHz, 1400 MHz, 1600 MHz, and 1800 MHz. Reducing the CPU speed will decrease system power consumption and performance. Extended temperature versions of the board do not allow operation above 1000 MHz. The CPU speed of the 1300 MHz *g* version and the 1000 MHz *v* version cannot be changed. The CPU speed of 1800 MHz is available on the *m*, *p*, *pr* and *r* versions only.

System RAM

COMPATIBLE MEMORY MODULES

The EBX-12 accepts two 200-pin SODIMM memory modules with the following characteristics:

- Size Up to 1 GB
- Voltage 2.5V
- Error Detection Non-Parity
- Type Unbuffered PC1600 (DDR200), PC2100 (DDR266) or PC2700 (DDR333)

RAM must be installed in order for the EBX-12 to function properly. Failure to install RAM will result in errors such as: failure to boot, no video output, or a 3-beep error code (if a speaker is attached.

CMOS RAM

CLEARING CMOS RAM

A jumper may be installed into V1[7-8] to erase the contents of the CMOS RAM and the Real-Time Clock. The jumper should be installed when the EBX-12 is turned off, left installed for a minimum of three seconds and removed before powering on the EBX-12.

CMOS Setup Defaults

The EBX-12 permits users to modify the CMOS Setup defaults. This allows the system to boot up with user-defined settings from cleared or corrupted CMOS RAM, battery failure or battery-less operation. All CMOS setup defaults can be changed, except the time and date. The CMOS Setup defaults can be updated with the Flash BIOS Update (FBU) Utility, available from the General BIOS Information page.

Warning! If the CMOS Setup default settings make the system unbootable and prevent the user from entering CMOS Setup, the EBX-12 needs to be serviced by the factory.

DEFAULT CMOS RAM SETUP VALUES

After the CMOS RAM is cleared, the system will load default CMOS RAM parameters the next time the board is powered on. The default CMOS RAM setup values will be used in order to boot the system whenever the main CMOS RAM values are blank, or when the system battery is dead or has been removed from the board.

SAVING CMOS SETUP PARAMETERS AS CUSTOM DEFAULTS

To save CMOS Setup parameters to custom defaults, you will need a DOS bootable floppy with the FBU utility on it.

1. Boot the EBX-12 and enter CMOS Setup by pressing Delete during the early boot cycle.
2. Change the CMOS parameters as desired and configure the floppy drive as the first boot device:

   ```
   Basic CMOS Configuration | BOOT ORDER | Boot 1st = Drive A:
   ```

3. Save the settings and exit CMOS Setup.
4. Reboot the system from the DOS boot floppy.
5. Run FBU and select **Save CMOS contents**. A file named CMOS.BIN is created and saved to the floppy.
6. Select the FBU option **Load Custom CMOS defaults**. A directory of the floppy is displayed.
7. Select the CMOS.BIN file and press the **P** key to program the new CMOS defaults.
8. Reboot the system from the hard disk. The custom CMOS parameters are now saved as defaults.

Real Time Clock

The EBX-12 features a year 2000-compliant, battery-backed 146818-compatible real-time clock/calendar chip. Under normal battery conditions, the clock maintains accurate timekeeping functions when the board is powered off.

SETTING THE CLOCK

The CMOS Setup utility (accessed by pressing the [DEL] key during a system boot) can be used to set the time/date of the real-time clock.

IDE Hard Drive / CD-ROM Interfaces

Two IDE interfaces are available to connect up to four IDE devices, such as hard disks, CD-ROM drives or Compact Flash. Connector J6 is the primary IDE controller with a 40-pin .1" connector and connector J10 is the secondary IDE controller with a 40-pin .1" connector. The secondary controller also has a Compact Flash socket (J14). Jumper V1[13-14] determines if the Compact Flash plugged into J14 is the master device or slave. Use the CMOS setup to specify the drive parameters of the attached drives.

Warning! Cable length must be 18" or less to maintain proper signal integrity. The grounds in this connector should not be used to carry motor current.

Table 6: IDE Hard Drive Connector Pinout

J6, J10 Pin	Signal Name	EIDE Signal Name	Function
1	HRST*	Host Reset	Reset signal from CPU
2	Ground	Ground	Ground
3	IDE7	DATA 7	Data bit 7
4	HD8	DATA 8	Data bit 8
5	HD6	DATA 6	Data bit 6
6	HD9	DATA 9	Data bit 9
7	HD5	DATA 5	Data bit 5
8	HD10	DATA 10	Data bit 10
9	HD4	DATA 4	Data bit 4
10	HD11	DATA 11	Data bit 11
11	HD3	DATA 3	Data bit 3
12	HD12	DATA 12	Data bit 12
13	HD2	DATA 2	Data bit 2
14	HD13	DATA 13	Data bit 13
15	HD1	DATA 1	Data bit 1
16	HD14	DATA 14	Data bit 14
17	HD0	DATA 0	Data bit 0
18	HD15	DATA 15	Data bit 15
19	Ground	Ground	Ground
20	NC	NC	Key
21	NC	NC	No connection
22	Ground	Ground	Ground
23	HWR*	HOST IOW*	I/O write
24	Ground	Ground	Ground
25	HRD*	HOST IOR*	I/O read
26	Ground	Ground	Ground
27	NC	NC	No connection
28	HAEN	ALE	Address latch enable
29	NC	NC	No connection
30	Ground	Ground	Ground
31	HINT	HOST IRQ14	IRQ14
32	XI16*	HOST IOCS16*	Drive register enabled
33	HA1	HOST ADDR1	Address bit 1
34	CBLID	CBLID	Cable Identification
35	HA0	HOST ADDR0	Address bit 0
36	HA2	HOST ADDR2	Address bit 2
37	HCS0*	HOST CS0*	Reg. access chip select 0
38	HCS1*	HOST CS1*	Reg. access chip select 1
39	NC	NC	No connection
40	Ground	Ground	Ground

High-Density 80-Pin Connector – J4

The J4 80-pin utility connector incorporates the parallel port, COM ports, USB ports, LEDs, speaker, PS/2 mouse and keyboard, and push button reset. Tables 7 and 8 show the function of each J4 pin and the pinout to the connectors of the breakout board. The USB interface wiring changed from EBX-12 version 5.xx to 6.xx to improve USB performance. The two versions are not compatible. Table 7 shows the pinout for version 5.xx and earlier boards. Table 8 shows the pinout for version 6.xx and later boards.

Table 7 High-Density 80-Pin Connector (J4) Pinout Rev. 5.xx and Earlier

J4 Pin	Breakout Connector	Pin	Signal
A1	**LPT1 J1 DB25**	1	Strobe
A2		14	Auto Feed
A3		2	Data Bit 1
A4		15	Printer Error
A5		3	Data Bit 2
A6		16	Reset
A7		4	Data Bit 3
A8		17	Select Input
A9		5	Data Bit 4
A10		18	Ground
A11		6	Data Bit 5
A12		19	Ground
A13		7	Data Bit 6
A14		20	Ground
A15		8	Data Bit 7
A16		21	Ground
A17		9	Data Bit 8
A18		22	Ground
A19		10	Acknowledge
A20		23	Ground
A21		11	Port Busy
A22		24	Ground
A23		12	Paper End
A24		25	Ground
A25		13	Select
A26	**–**	–	No connection
A27	**PLED – D1 Green**	–	Protected +5V
A28		–	Programmable LED
A29	**Speaker SP1**	–	Protected +5V
A30		–	Speaker Drive
A31	**IDE LED – D1 Orange**	–	Protected +5V
A32		–	IDE LED
A33	**Mouse J2 Top**	4	Protected +5V
A34		1	Mouse Data
A35		3	Ground
A36		5	Mouse Clock
A37	**Keyboard J2 Bottom**	4	Protected +5V
A38		1	Keyboard Data
A39		3	Ground
A40		5	Keyboard Clock

J4 Pin	Breakout Connector	Pin	Signal
B1	**USB0 J5 Bottom**	1	Protected +5V
B2		4	Ground
B3		2	Channel 0 Data -
B4		–	Cable Shield
B5		3	Channel 0 Data +
B6	**USB1 J5 Top**	3	Channel 1 Data +
B7		–	Cable Shield
B8		2	Channel 1 Data -
B9		4	Ground
B10		1	Protected +5V
B11	**USB2 J6**	1	Protected +5V
B12		4	Ground
B13		2	Channel 2 Data -
B14		5	Cable Shield
B15		3	Channel 2 Data +
B16	**USB3 J6**	8	Channel 3 Data +
B17		6	Cable Shield
B18		9	Channel 3 Data -
B19		7	Ground
B20		10	Protected +5V
B21	**COM1 J1 Left DB9**	1	Data Carrier Detect
B22		6	Data Set Ready
B23		2	Receive Data
B24		7	Request to Send
B25		3	Transmit Data
B26		8	Clear to Send
B27		4	Data Terminal Ready
B28		9	Ring Indicator
B29		5	Ground
B30	**COM2 J1 Right DB9**	1	Data Carrier Detect
B31		6	Data Set Ready
B32		2	Receive Data
B33		7	Request to Send
B34		3	Transmit Data
B35		8	Clear to Send
B36		4	Data Terminal Ready
B37		9	Ring Indicator
B38		5	Ground
B39	**Push Button Reset – S1**	–	Ground
B40		–	Push Button Reset

Table 8 High-Density 80-Pin Connector (J4) Pinout Rev. 6.xx and Later

J4 Pin	Breakout Connector	Pin	Signal
A1	**LPT1 J1 DB25**	1	Strobe
A2		14	Auto Feed
A3		2	Data Bit 1
A4		15	Printer Error
A5		3	Data Bit 2
A6		16	Reset
A7		4	Data Bit 3
A8		17	Select Input
A9		5	Data Bit 4
A10		18	Ground
A11		6	Data Bit 5
A12		19	Ground
A13		7	Data Bit 6
A14		20	Ground
A15		8	Data Bit 7
A16		21	Ground
A17		9	Data Bit 8
A18		22	Ground
A19		10	Acknowledge
A20		23	Ground
A21		11	Port Busy
A22		24	Ground
A23		12	Paper End
A24		25	Ground
A25		13	Select
A26	**–**	–	No connection
A27	**PLED – D1 Green**	–	Protected +5V
A28		–	Programmable LED
A29	**Speaker SP1**	–	Protected +5V
A30		–	Speaker Drive
A31	**IDE LED – D1 Orange**	–	Protected +5V
A32		–	IDE LED
A33	**Mouse J2 Top**	4	Protected +5V
A34		1	Mouse Data
A35		3	Ground
A36		5	Mouse Clock
A37	**Keyboard J2 Bottom**	4	Protected +5V
A38		1	Keyboard Data
A39		3	Ground
A40		5	Keyboard Clock

J4 Pin	Breakout Connector	Pin	Signal
B1	**USB0 J5 Bottom**	B1	Protected +5V
B2		B3	Channel 0 Data +
B3		B2	Channel 0 Data -
B4		B4	Ground
B5		–	Cable Shield
B6	**USB1 J5 Top**	–	Cable Shield
B7		T4	Ground
B8		T2	Channel 1 Data -
B9		T3	Channel 1 Data +
B10		T1	Protected +5V
B11	**USB2 J6**	1	Protected +5V
B12		3	Channel 2 Data +
B13		2	Channel 2 Data -
B14		4	Ground
B15		5	Ground
B16	**USB3 J6**	6	Ground
B17		7	Ground
B18		9	Channel 3 Data -
B19		8	Channel 3 Data +
B20		10	Protected +5V
B21	**COM1 J1 Left DB9**	1	Data Carrier Detect
B22		6	Data Set Ready
B23		2	Receive Data
B24		7	Request to Send
B25		3	Transmit Data
B26		8	Clear to Send
B27		4	Data Terminal Ready
B28		9	Ring Indicator
B29		5	Ground
B30	**COM2 J1 Right DB9**	1	Data Carrier Detect
B31		6	Data Set Ready
B32		2	Receive Data
B33		7	Request to Send
B34		3	Transmit Data
B35		8	Clear to Send
B36		4	Data Terminal Ready
B37		9	Ring Indicator
B38		5	Ground
B39	**Push Button Reset – S1**	–	Ground
B40		–	Push Button Reset

The 5V power supplied to pins on this connector is protected by three 1 Amp., self-resetting fuses. USB0 and USB1 power is protected by one fuse; USB2 and USB3 power is protected by a second fuse; and the keyboard, mouse, speaker, and LEDs are protected by a third fuse.

High-Density 80-Pin Connector – J8

The J8 80-pin utility connector incorporates the audio, digital I/O, analog I/O, CTC, COM3 and COM4 features. The following table shows the function of each pin and the pinout to the connectors of the CBL/CBR-8004 breakout board.

Table 9 High-Density 80-Pin Connector (J8) Pinout

J8 Pin	CBL/CBR-8004 Connector	Pin	Signal
A1	**Audio J1**	3	Ground
A2		1	Line-in-Left
A3		2	Line-in-Right
A4		4	Line-out-Left
A5		5	Line-out-Right
A6		6	Ground
A7	**Digital I/O J2**	–	Ground
A8		1	Digital I/O 0
A9		2	Digital I/O 1
A10		3	Digital I/O 2
A11		4	Digital I/O 3
A12		5	Digital I/O 4
A13		6	Digital I/O 5
A14		7	Digital I/O 6
A15		8	Digital I/O 7
A16		9	Digital I/O 8
A17		10	Digital I/O 9
A18		11	Digital I/O 10
A19		12	Digital I/O 11
A20		13	Digital I/O 12
A21		14	Digital I/O 13
A22		15	Digital I/O 14
A23		16	Digital I/O 15
A24		17	Digital I/O 16
A25		18	Digital I/O 17
A26		19	Digital I/O 18
A27		20	Digital I/O 19
A28		21	Digital I/O 20
A29		22	Digital I/O 21
A30		23	Digital I/O 22
A31		24	Digital I/O 23
A32		25	Digital I/O 24
A33		26	Digital I/O 25
A34		27	Digital I/O 26
A35		29	Digital I/O 27
A36		29	Digital I/O 28
A37		30	Digital I/O 29
A38		31	Digital I/O 30
A39		32	Digital I/O 31
A40		–	Ground

J8 Pin	CBL/CBR-8004 Connector	Pin	Signal
B1	**Analog I/O J3**	9	Ground
B2		1	Ch 0 Analog Input
B3		2	Ch 1 Analog Input
B4		3	Ch 2 Analog Input
B5		4	Ch 3 Analog Input
B6		5	Ch 4 Analog Input
B7		6	Ch 5 Analog Input
B8		7	Ch 6 Analog Input
B9		8	Ch 7 Analog Input
B10		10	Ground
B11	**CTC J5**	1	Ch 3 CTC Output
B12		2	Ch 3 CTC Gate Input
B13		3	Ch 4 CTC Input
B14		4	Ground
B15		5	Ch 4 CTC Output
B16		6	Ch 4 CTC Gate Input
B17		7	Ch 5 CTC Input
B18		8	Ground
B19		9	Ch 5 CTC Output
B20		10	Ch 5 CTC Gate Input
B21	**COM3 J4**	1	Data Carrier Detect
B22		6	Data Set Ready
B23		2	Receive Data
B24		7	Request to Send
B25		3	Transmit Data
B26		8	Clear to Send
B27		4	Data Terminal Ready
B28		9	Ring Indicator
B29		5	Ground
B30	**COM4 J4**	10	Data Carrier Detect
B31		15	Data Set Ready
B32		11	Receive Data
B33		16	Request to Send
B34		12	Transmit Data
B35		17	Clear to Send
B36		13	Data Terminal Ready
B37		18	Ring Indicator
B38		14	Ground
B39		–	No connection
B40		–	No connection

Serial Ports

The EBX-12 features four on-board 16550-based serial channels located at standard PC I/O addresses. COM1 and COM2 are RS-232 (115.2K baud) serial ports. IRQ lines are chosen in the CMOS Setup.

COM3 and COM4 can be operated in RS-232, RS-422 or RS-485 modes. Additional non-standard baud rates are also available (programmable in the normal baud registers) of up to 460k baud. IRQ lines are chosen in the CMOS Setup.

Each COM port can be independently enabled or disabled in the CMOS setup screen.

COM Port Configuration

There are no configuration jumpers for COM1 and COM2 since they only operate in RS-232 mode.

Use the CMOS setup to select between RS-232/RS-422/RS485 operating modes for COM3 and COM4.

Jumper V1[9-10] is used to enable the RS-422/485 termination resistor for COM3. Jumper V1[11-12] is used to enable the RS-422/485 termination resistor for COM4. The termination resistor should be enabled for RS-422 and the RS-485 endpoint station. It should be disabled for RS-232 and the RS-485 intermediate station.

COM3 / COM4 RS-485 Mode Line Driver Control

The TxD+/TxD– differential line driver can be turned on and off by manipulating the COM3DIR and COM4DIR bits in offset 0 of the Special Control Registers. See page 66.

The following code example shows how to toggle the line driver for COM3 when the base address for the Board Control Registers (BCRs) is set to 1D0h.

```
MOV   DX,1D0H    ; POINT TO SPECIAL CONTROL REGISTER
IN    AL,DX      ; FETCH EXISTING VALUE
OR    AL,04H     ; SET BIT D2, COM3DIR
OUT   DX,AL      ; WRITE MODIFIED VALUE
```

SERIAL PORT CONNECTORS

See the *Connector Location Diagrams* on page 16 for connector and cable information. The pinouts of the DB9M connectors apply to the serial connectors on the VersaLogic breakout boards, CBL-8003 and CBL/CBR-8004.

These connectors use IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 10: Connectors J1 CBL-8003 — Serial Port Pinout

COM1	COM2	
DB9 J1B Pin	DB9 J1C Pin	RS-232
1	1	DCD
2	2	RXD*
3	3	TXD*
4	4	DTR
5	5	Ground
6	6	DSR
7	7	RTS
8	8	CTS
9	9	RI

Table 11: Connectors J4 CBL/CBR-8004 — Serial Port Pinout

COM3	COM4			
DB9 J4A Pin	DB9 J4B Pin	RS-232	RS-422	RS-485
1	1	DCD	—	—
2	2	RXD*	TxD+	—
3	3	TXD*	—	—
4	4	DTR	RxD–	TxD/RxD–
5	5	Ground	Ground	Ground
6	6	DSR	—	—
7	7	RTS	TxD–	—
8	8	CTS	Ground	Ground
9	9	RI	RxD+	TxD/RxD+

SETTING COM3 AND COM4 TO HIGH SPEED BAUD RATES

Two high speed baud rates are available for COM3 and COM4: 230400 bps and 460800 bps. COM3 and COM4 are controlled by the second of two SMSC Super I/O chips on the EBX-12. The base address of the second Super I/O chip (Super I/O #1) is 4Eh.

To use a high speed baud rate for COM3 or COM4, you must:

- Set a high speed mode bit in the appropriate logical device Mode Register
- Program a special baud rate divisor in the appropriate UART

As shown in the figure below, COM3 is Logical Device 4 (also known as "Serial Port 1") in the Super I/O chip architecture. UART 1 within the Super I/O chip contains the standard set of 65550 compatible COM port registers.

COM4 is Logical Device 5 (also known as "Serial Port 2") in the Super I/O chip architecture.

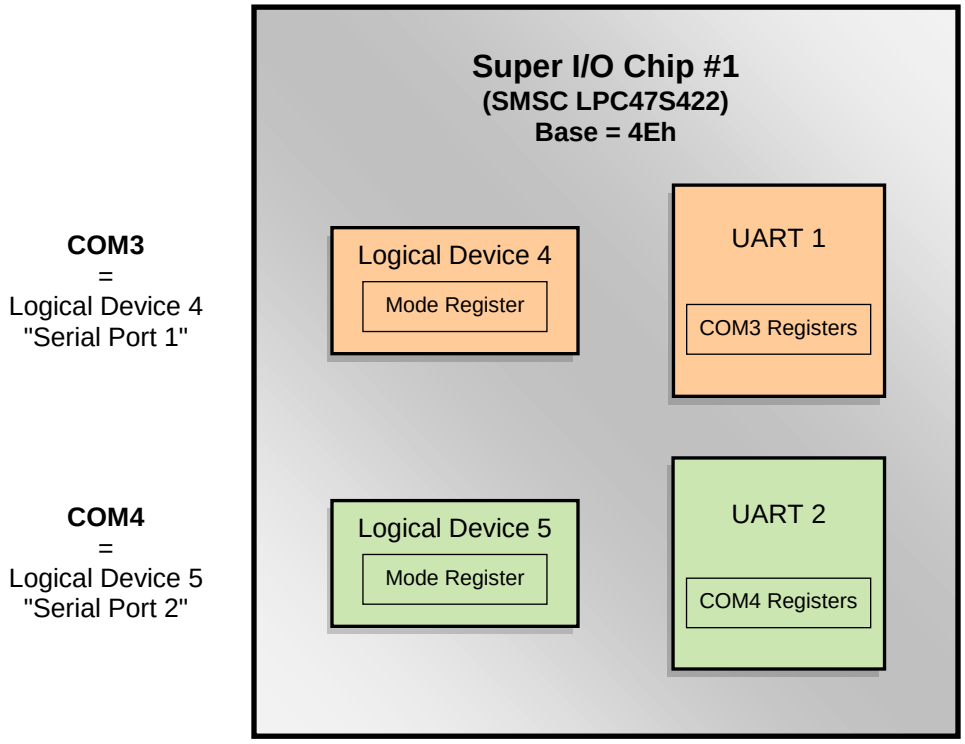


Figure 15. Super I/O Chip COM Ports

Procedure for Setting the High Speed Mode Bit

The following procedure summarizes the steps for setting the high speed mode bit.

1. Place the Super I/O Chip into Configuration Mode by writing 55h to port 4Eh.
2. Point to the Logical Device Configuration Register by writing 07h to port 4Eh.
3. Point to the appropriate logical device (Logical Device 4 for COM3, or Logical Device 5 for COM4) by writing 04h or 05h to port 4Fh.
4. Use a read-modify-write technique to change the high speed bit in the Mode Register (F0h) of the logical device.
    a. Point to the Mode Register by writing F0h to port 4Eh.
    b. Read the Mode Register by reading port 4Fh.
    c. Set the high speed bit (bit D1).
    d. Refresh the Mode Register by writing the updated value to port 4Fh.
5. Exit Configuration Mode by writing AAh to port 4Eh.

Procedure for Programming a High Speed Baud Rate Divisor

The following procedure summarizes the steps for writing a high speed baud rate divisor to the COM port registers.

1. Set the Divisor Latch Access Bit (DLAB) in the Line Control register. To do this, write 80h to port 3E8h (for COM3) or port 2E8h (for COM4).
2. Program the special baud rate divisor. To do this, write the divisor value shown below to the Divisor Latch LSB and MSB registers.

Baud Rate	Divisor	Hex
230400	32770	8002
460800	32769	8001

    For a baud rate of 230400, set the divisor as follows:

    Divisor Latch LSB (COM base + 0) = 02h
    Divisor Latch MSB (COM base + 1) = 80h

    For a baud rate of 460800, set the divisor as follows:

    Divisor Latch LSB (COM base + 0) = 01h
    Divisor Latch MSB (COM base + 1) = 80h

3. Set the communication format in COM base + 3, making sure to clear the DLAB bit.

Code Example

```
'EBX-12 Code Example for operating COM3 at 460800 bps, N81

'Select COM port
comport = 3

Select Case comport
Case 3
  com_base = &H3E8
  config_port = &H4E
  logical_device = 4
Case 4
  com_base = &H2E8
  config_port = &H4E
  logical_device = 5
End Select

'Enter configuration mode
out config_port, &H55

'Point to LOGICAL DEVICE CONFIGURATION reg
out config_port, &H7

'Point to appropriate serial port
out config_port + 1, logical_device

'Read the value of the SERIAL PORT CONFIGURATION reg
out config_port, &HF0
config = inp(config_port + 1)

'Set the HIGH SPEED BIT
config = (config Or &H2)

'Update the SERIAL PORT CONFIGURATION reg
out config_port, &HF0
out config_port + 1, config

'Exit configuration mode
out config_port, &HAA

'Set DLAB bit to gain access to baud rate registers
out com_base + 3, &H80

'Baud rate register LSB
out com_base + 0, &H1

'Baud rate register MSB
out com_base + 1, &H80

'Communication format = N81
out com_base + 3, &H3
```

Super I/O Chip References

For details, see the SMSC Super I/O datasheet for the LPC47S422 chip at:

www.VersaLogic.com/Support/Downloads/PDF/47s42x.pdf

Some pertinent sections are listed below.

- Baud Rate Chart – page 83
- High Speed Bit – page 220
- Configuration Register Information – page 17
- Standard UART Registers – page 72
- Configuration Access Procedure – page 200
- Logical Device 4/5 Configuration Registers – page 204

Parallel Port

The EBX-12 includes a standard bi-directional/EPP/ECP compatible LPT port which resides at the PC standard address of 378h. The port can be enabled or disabled and interrupt assignments can be made via the CMOS setup screen. The LPT mode is also set via the CMOS setup screen. The pinout of the DB25F connector applies to use of the VersaLogic transition cable (CBL-8003).

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 12: LPT1 Parallel Port Pinout

CBL-8003 J1A Pin	Centronics Signal	Floppy Signal	Signal Direction
1	Strobe	DS0*	Out
2	Data bit 1	INDEX*	In/Out
3	Data bit 2	TRK0*	In/Out
4	Data bit 3	WP*	In/Out
5	Data bit 4	RDATA*	In/Out
6	Data bit 5	DSKCHG	In/Out
7	Data bit 6	N.C.	In/Out
8	Data bit 7	MTR0*	In/Out
9	Data bit 8	N.C.	In/Out
10	Acknowledge	DS1*	In
11	Port Busy	MTR1*	In
12	Paper End	WDATA*	In
13	Select	WGATE*	In
14	Auto feed	RPM	Out
15	Printer error	HDSEL*	In
16	Reset	FDIR	Out
17	Select input	STEP*	Out
18	Ground	GND	—
19	Ground	GND	—
20	Ground	GND	—
21	Ground	GND	—
22	Ground	GND	—
23	Ground	GND	—
24	Ground	GND	—
25	Ground	GND	—

PARALLEL PORT FLOPPY DISK

The parallel port on the EBX-12 can be used as a floppy disk interface. Select “Floppy” as the LPT mode in the CMOS setup and connect a floppy disk drive to the parallel port via the CBL/CBR-2501 cable to use this feature.

DB-25 FEMALE CONNECTOR

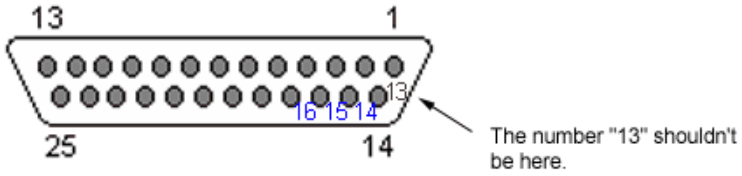


Figure 16. DB-25 Female Connector

The large outer numbers are correct. The manufacturer's marking for pin 13 is incorrectly placed.

Keyboard and Mouse

A standard PS/2 keyboard and mouse interface is accessible through connector J2 of the VersaLogic breakout board, CBL-8003 or CBR-8005. The breakout board is connected to connector J4 of the EBX-12. The 5V power provided to the keyboard and mouse is protected by a 1 Amp fuse.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 13: PS/2 Mouse and Keyboard

Breakout J2 Top Pin	Signal	Description
1	MSDATA	Mouse Data
2	–	No Connection
3	GND	Ground
4	MKPWR	Protected +5V
5	MSCLK	Mouse Clock
6	–	No Connection
Breakout J2 Bottom Pin	**Signal**	**Description**
1	KBDATA	Keyboard Data
2	–	No Connection
3	GND	Ground
4	MKPWR	Protected +5V
5	KBCLK	Keyboard Clock
6	–	No Connection

Programmable LED

Connector J4 includes an output signal for attaching a software controlled LED. Connect the cathode of the LED to J4, pin A28, connect the anode to +5V. An on-board resistor limits the current to 15 mA when the circuit is turned on. A programmable LED is provided on the CBL-8003 or CBR-8005 breakout board.

To turn the LED on and off, set or clear bit D7 in I/O port 1D0h (or 1E0h). When changing the register, make sure not to alter the value of the other bits.

The following code examples show how to turn the LED on and off. Refer to page 66 for further information:

LED On

```
MOV   DX,1D0H
IN    AL,DX
OR    AL,80H
OUT   DX,AL
```

LED Off

```
MOV   DX,1D0H
IN    AL,DX
AND   AL,7FH
OUT   DX,AL
```

Note: The LED is turned on by the BIOS during system startup. This causes the light to function as a "power on" indicator if it is not otherwise controlled by user code. The BIOS also flashes the LED in sync with “Beep Codes” when an error occurs.

External Speaker

A miniature 8 ohm speaker can be connected between J4, pin 30A (SPKO*) and J4, pin 29A (MKPWR). A speaker is provided on the CBL-8003 or CBR-8005 breakout board.

Push-Button Reset

Connector J4 (see page 30) includes an input for a push-button reset switch. Shorting J4, pin B40 to ground causes the EBX-12 to reboot.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

A reset button is provided on the CBL-8003 or CBR-8005 breakout board.

IDE LED

Connector J4 includes an output signal for attaching an IDE Activity LED. Connect the cathode of the LED to J4, pin A32, and connect the anode to +5V. An on-board resistor limits the current to 15 mA when the circuit is turned on. An IDE LED is provided on the CBL-8003 or CBR-8005 breakout board.

Video Interface

An on-board video controller integrated into the chipset provides high performance video output for the EBX-12.

CONFIGURATION

The video interface uses PCI interrupt "INTA*". The CMOS setup screen is used to select the IRQ line routed to INTA*.

The EBX-12 uses shared memory architecture. This allows the video controller to use variable amounts of system DRAM for video RAM. The amount of RAM used for video is set with a CMOS setup option.

The EBX-12 supports two types of video output, SVGA and LVDS Flat Panel Display. A CMOS setup option is used to select which output is enabled after POST.

VIDEO BIOS SELECTION

Jumper V1[3-4] can be removed to allow the system to boot off of the Secondary Video BIOS. Unlike the Primary Video BIOS, the Secondary Video BIOS can be reprogrammed in the field.

SVGA OUTPUT CONNECTOR

See the connector location diagram on page 16 for pin and connector location information. An adapter cable, part number CBL/CBR-1007, is available to translate J7 into a standard 15-pin D-Sub SVGA connector.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 14: Video Output Pinout

J7 Pin	Signal Name	Function	Mini DB15 Pin
1	GND	Ground	6
2	CRED	Red video	1
3	GND	Ground	7
4	CGRN	Green video	2
5	GND	Ground	8
6	CBLU	Blue video	3
7	GND	Ground	5
8	CHSYNC	Horizontal Sync	13
9	GND	Ground	10
10	CVSYNC	Vertical Sync	14

LVDS Flat Panel Display Connector

The integrated LVDS Flat Panel Display in the EBX-12 is an ANSI/TIA/EIA-644-1995 specification-compliant interface. It can support up to 24 bits of RGB pixel data plus 3 bits of timing control (HSYNC/VSYNC/DE) on the 4 differential data output pairs. The LVDS clock frequency ranges from 25 MHz to 112 MHz.

CMOS setup provides several options for standard LVDS Flat Panel types. If these options do not match the requirements of the panel you are attempting to use, contact support@VersaLogic.com for a custom video BIOS.

The 3.3V power provided to pins 19 and 20 of J5 is protected by a 1 Amp fuse.

See the connector location diagram on page 16 for pin and connector location information.

Table 15: LVDS Flat Panel Display Pinout

J5 Pin	Signal Name	Function
1	GND	Ground
2	NC	Not Connected
3	LVDSA3	Diff. Data (+)
4	LVDSA3#	Diff. Data 3 (–)
5	GND	Ground
6	LVFSCLK0	Differential Clock (+)
7	LVDSCLK0#	Differential Clock (–)
8	GND	Ground
9	LVDSA2	Diff. Data 2 (+)
10	LVDSA2#	Diff. Data 2 (–)
11	GND	Ground
12	LVDSA1	Diff. Data 1 (+)
13	LVDSA1#	Diff. Data 1 (–)
14	GND	Ground
15	LVDSA0	Diff. Data 0 (+)
16	LVDSA0#	Diff. Data 0 (–)
17	GND	Ground
18	GND	Ground
19	+3.3V	Protected Power Supply
20	+3.3V	Protected Power Supply

Note: The physical pin configuration for the EBX-12 Rev 4 and earlier boards was correct, but the board silkscreen was incorrect. On Rev 4 and earlier boards the pinout was labeled as shown below.

Table 16: LVDS Flat Panel Display EBX-12 Rev 4 Pinout

J5 Pin	Signal Name	Function
1	+3.3V	Protected Power Supply
2	+3.3V	Protected Power Supply
3	GND	Ground
4	GND	Ground
5	LVDSA0#	Diff. Data 0 (–)
6	LVDSA0	Diff. Data 0 (+)
7	GND	Ground
8	LVDSA1#	Diff. Data 1 (–)
9	LVDSA1	Diff. Data 1 (+)
10	GND	Ground
11	LVDSA2#	Diff. Data 2 (–)
12	LVDSA2	Diff. Data 2 (+)
13	GND	Ground
14	LVDSCLK0#	Differential Clock (–)
15	LVFSCLK0	Differential Clock (+)
16	GND	Ground
17	LVDSA3#	Diff. Data 3 (–)
18	LVDSA3	Diff. Data (+)
19	NC	Not Connected
20	GND	Ground

COMPATIBLE LVDS PANEL DISPLAYS

The following list of flat panel displays are reported to work properly with the integrated graphics video controller chip used on the EBX-12:

Manufacture	Model Number	Panel Size	Resolution	Interface	Panel Technology
eVision Displays	xxx084S01 series	8.4”	800 x 600 18-bit	LVDS	TFT
au Optronix	B084SN01	8.4”	800 x 600 18-bit	LVDS	TFT
eVision Displays	xxx104S01 series	10.4”	800 x 600 18-bit	LVDS	TFT
au Optronix	B104SN01	10.4”	800 x 600 18-bit	LVDS	TFT
eVision Displays	xxx141X01 series	14.1”	1024 x 768 18-bit	LVDS	TFT

CONSOLE REDIRECTION

The EBX-12 can operate with either a standard keyboard and VGA video monitor or a special emulation of a console. The emulation is transmitted over an RS-232 cable connected to a host computer that is running a terminal emulation program such as HyperTerminal.

Console input and output can be redirected to COM1 and requires the following:

- A remote console device (such as a laptop computer) connected to the Cobra's COM1 port using a full-handshake null-modem cable (see Null Modem below).
- Communication parameters set to 115200 bps, 8 data bits, 1 stop bit, no parity, and no hardware or software flow control.
- A terminal program (such as Windows HyperTerminal) on COM1.
- Ctrl-C, Enter, or ESC detected on COM1 early during the power-on self-test (POST).

To configure the EBX-12 COM1 port for console redirection:

1. Connect the remote console device to COM1 using a null-modem cable.
2. Turn on the remote console and start HyperTerminal.
3. Restart the Cobra.
4. Press Ctrl-C, Enter, or ESC continuously until the console is redirected.

Null Modem

The following diagram illustrates a typical DB9 to DB9 RS-232 null-modem adapter.

Note: There is no firm standard for null-modem cables. We strongly recommend that you measure the pinout of your cable to verify compatibility with this diagram.

```
System 1    <-->    System 2
Name  Pin           Pin   Name
----------------------------
TX     3    <-->    2     RX
RX     2    <-->    3     TX
RTS    7    <-->    1     DCD
CTS    8
DSR    6    <-->    4     DTR
DCD    1    <-->    7     RTS
                    8     CTS
DTR    4    <-->    6     DSR
```

Notes:

- Pins 7 and 8 are shorted together on each connector.
- Unlisted pins have no connection.

Ethernet Interface

The EBX-12 features two on-board Ethernet controllers. These controllers can be either the Intel 82551ER Fast Ethernet controller or the Intel 82541ER Gigabit Ethernet controller. Contact the factory for custom controller configurations. While these controllers are not NE2000-compatible, they are widely supported. Drivers are readily available to support a variety of operating systems. See VersaLogic website for latest OS support.

BIOS CONFIGURATION

Each Ethernet controller can be enabled or disabled in the CMOS setup. Ethernet interface 1 (J1) uses PCI interrupt "INTD#". The CMOS setup screen is used to select the IRQ line routed to each PCI interrupt line. Ethernet interface 0 (J3) uses PCI interrupt and "INTC#"

STATUS LED

Each Ethernet controller has a two-colored LED located next to its RJ-45 connector to provide an indication of the Ethernet status as follows:

Green LED (Link)

- ON — Active Ethernet cable plugged in
- OFF — Active cable not plugged in or cable not plugged into active hub

Yellow LED (Activity)

- ON — Activity detected on cable
- OFF — No Activity detected on cable

ETHERNET CONNECTOR

Board-mounted RJ-45 connectors are provided to make connections with Category 5 Ethernet cables. The 82541ER Ethernet controller autodetects 10BaseT/100Base-TX/1000BaseT connections. The 82551ER Ethernet controller autodetects 10BaseT/100Base-TX connectors.

These connectors use IEC 61000-4-2-rated TVS components to help protect against ESD damage.

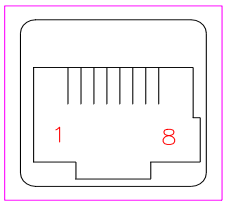


Table 17: RJ45 Ethernet Connector

J1/J3 Pin	Fast Ethernet Signal Name	Fast Ethernet Function	Gigabit Ethernet Signal Name	Gigabit Ethernet Function
1	T+	Transmit Data +	MID0+	Media Dependent Interface [0]+
2	T–	Transmit Data –	MID0–	Media Dependent Interface [0]–
3	R+	Receive Data +	MID1+	Media Dependent Interface [1]+
4	IGND	Isolated Ground	MID2+	Media Dependent Interface [2]+
5	IGND	Isolated Ground	MID2–	Media Dependent Interface [2]–
6	R–	Receive Data –	MID1–	Media Dependent Interface [1]–
7	IGND	Isolated Ground	MID3+	Media Dependent Interface [3]+
8	IGND	Isolated Ground	MID3–	Media Dependent Interface [3]–

Audio

The audio interface on the EBX-12 is implemented using the Analog Devices AD1981B Audio Codec. This interface is AC ’97 2.3 compatible. Drivers are available for most Windows-based operating systems. To obtain the most current versions, consult the EBX-12 product support page at **www.VersaLogic.com/private/cobrasupport.asp.**

J8 provides the line-level stereo input and line-level stereo output connection points. The outputs will drive any standard-powered PC speaker set.

These connectors uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

SOFTWARE CONFIGURATION

The audio interface uses PCI interrupt “INTB#”. The CMOS setup screen is used to select the IRQ line routed to INTB#.

The audio controller can be disabled within the CMOS setup.

Table 18: Audio Connector

CBL/CBR-8004 J1 Top Pin	Signal Name	Function
1	AUDINL	Line-In Left
2	AUDINR	Line-In Right
3	Ground	Ground
CBL/CBR-8004 J1 Bottom Pin	**Signal Name**	**Function**
1	AUDOUTL	Line-Out Left
2	AUDOUTR	Line-Out Right
3	Ground	Ground

Watchdog Timer

A watchdog timer circuit is included on the EBX-12 to reset the CPU or issue a NMI if proper software execution fails or a hardware malfunction occurs.

ENABLING THE WATCHDOG

Bit D0 in I/O port 1D0h (or 1E0h) is used to enable or disable the watchdog from resetting the CPU on timer expiration. Bit D1 in I/O port 1D0h (or 1E0h) is used to enable or disable the watchdog from issuing a NMI on timer expiration. When changing the contents of the register, make sure not to alter the value of the other bits. The following procedure should be used when enabling the watchdog to prevent erroneous resets or NMI generation.

The following code example enables the watchdog reset:

```
        MOV   DX,1D2H  ;CLEAR BIT D2 (WDOGSTA) IN THE JSR REGISTER
        IN    AL,DX
        OR    AL,04H
        OUT   DX,AL

LOOP:   IN    AL,DX    ;LOOP WHILE BIT D2 (WDOGSTA) = 0
        AND   AL,04H
        JZ    LOOP
        IN    AL,DX    ;CLEAR BIT D2 (WDOGSTA) IN THE JSR REGISTER
        OR    AL,04H
        OUT   DX,AL

        MOV   DX,1D0H  ;ENABLE THE WATCHDOG (RESET MODE)
        IN    AL,DX
        OR    AL,01H
        OUT   DX,AL
```

NOTE: The watchdog is disabled when the EBX-12 is powered on or reset.

DISABLING THE WATCHDOG

The watchdog may be disabled at any time by clearing the above mentioned bits; no special procedure is required.

REFRESHING THE WATCHDOG

If the watchdog timer is enabled, software must periodically refresh the watchdog timer at a rate faster than the timer is set to expire (1.0 sec minimum). Outputting a 5Ah to the *Watchdog Timer Hold-Off Register* at 1D1h (or 1E1h) resets the watchdog time-out period, see page 67 for additional information.

There is no provision for selecting a different timeout period using software.

The following code example refreshes the watchdog:

```
MOV   DX,1D1H
MOV   AL,5AH
OUT   DX,AL
```

CPU Temperature Monitor

A thermometer circuit constantly monitors the die temperature of the CPU. This circuit can be used to detect over-temperature conditions which can result from fan or heat sink failure or excessive ambient temperatures.

The system can be configured to generate a Non-Maskable Interrupt (NMI) when the temperature exceeds the threshold.

The CMOS setup is used to set the temperature detection threshold. A status bit in the *Special Control Register* bit D5 if I/O port 1D0h (or 1E0h), can be read to determine if the die temperature is above the threshold.

Contact the factory for information on clearing the status bit or reading and writing to the thermometer circuit. See page 66 for additional information.

Analog Input

The EBX-12 may employ an optional multi-range, 12-bit A/D converter which accepts up to eight single-ended input signals. The converter features fast 6 microsecond conversion time, with channel-independent input ranges of 0 to +5V, ±5V, 0 to +10V and ±10V.

> **Note:** Analog input is an optional feature. If you have difficulty accessing the A/D converter, verify that a chip is installed in socket U15.

SOFTWARE CONFIGURATION

The EBX-12 can be configured to issue an interrupt when the analog-to-digital converter has completed a conversion. IRQ selection is done in the CMOS setup.

EXTERNAL CONNECTIONS

Single-ended analog voltages are applied to connector J8 as shown in the following table.

Table 19: Analog Input Connector

CBL/CBR-8004 J3 Pin	Signal Name	Function
–	Ground	Analog Ground
1	ADCH0	Channel 0 Analog Input
2	ADCH1	Channel 1 Analog Input
3	ADCH2	Channel 2 Analog Input
4	ADCH3	Channel 3 Analog Input
5	ADCH4	Channel 4 Analog Input
6	ADCH5	Channel 5 Analog Input
7	ADCH6	Channel 6 Analog Input
8	ADCH7	Channel 7 Analog Input
9	Ground	Analog Ground
10	Ground	Analog Ground

Warning! All analog inputs are fault-protected to ±16V (board power on or off). Exceeding these maximums can cause permanent damage to the A/D converter circuitry. Such damage is not covered under warranty.

CALIBRATION

There are no calibration adjustments. Calibration, if desired, is accomplished by mathematical transformation in software.

ANALOG CONTROL REGISTER

ACR (WRITE) 1D8h (or 1E8h via the CMOS setup)

D7	D6	D5	D4	D3	D2	D1	D0
PD1	PD0	ACQMD	RNG	BIP	A2	A1	A0

Table 20: Analog Control Register Bit Assignments

Bit	Mnemonic	Description
D7, D6	PD1, PD0	**Clock and Power-Down Selection —** These bits select the power savings mode and clock source for the A/D circuit. **PD1 PD0 Mode** 0 0 Normal Operation / External Clock Mode 0 1 Normal Operation / Internal Clock Mode 1 0 Standby Power-Down (STBYPD) 1 1 Full Power-Down (FULLPD) ***Note:*** *STBYPD and FULLPD selections do not affect the clock mode.*
D5	ACQMD	**Acquisition Mode —** This bit selects the type of acquisition mode. ACQMD = 0 Internal Acquisition. A write to the ACR register initiates an acquisition interval whose duration is internally timed. Conversion starts when this six-clock-cycle acquisition interval (3.26µs) ends. ACQMD = 1 External Acquisition. Use this mode for precise control of the sampling aperture and/or independent control of acquisition and conversion times. The acquisition and start-of-conversion is controlled with two separate writes to the ACR register. The first write, written with ACQMD = 1, starts and acquisition interval of indeterminate length. The second write, written with ACQMD = 0, terminates acquisition and starts conversion. However, if the second write contains ACQMD = 1, an indefinite acquisition interval is restarted. ***Note:*** *The address bits for the input mux (A0–A2) must have the same values on the first and second write pulses. Power-down mode bits (PD0, PD1) can assume new values on the second write.*
D4, D3	RNG, BIP	**Range and Polarity Selection —** These bits select the input range and polarity on a channel-by-channel basis. **RNG BIP Input Range** 0 0 0 to +5V 1 0 0 to +10V 0 1 ±5V 1 1 ±10V ***Warning!*** *The board can be damaged if voltages in excess of ±16V are applied.*
D2-D0	A2, A1, A0	**Input Channel Address —** These bits select which input channel you wish to convert. **A2 A1 A0 Channel** 0 0 0 Channel 0 0 0 1 Channel 1 0 1 0 Channel 2 0 1 1 Channel 3 1 0 0 Channel 4 1 0 1 Channel 5 1 1 0 Channel 6 1 1 1 Channel 7

INDUSTRIAL I/O CONTROL REGISTER

IIOCR (READ/WRITE) 1D3H (or 01E3h via the CMOS setup)

D7	D6	D5	D4	D3	D2	D1	D0
DONE	CTC5MODE1	CTC5MODE0	CTC4MODE	DIR3	DIR2	DIR1	DIR0

Table 21: Industrial I/O Control Register Bit Assignments

Bit	Mnemonic	Description
D7	DONE	**Analog Input Conversion Complete** — This status bit is used to determine when it is all right to read data from the A/D converter. DONE = 0 Conversion underway, data not yet available DONE = 1 Analog input conversion has completed. Valid data is available to read from the ADCLO and ADCHI registers. Done value is reset to "0" when a new conversion is started. ***Note:*** *This bit is cleared by reading either ADCHI or ADCLO registers or by writing to the ACR register.*
D6-D5	CTC5MODE1-CTC5MODE0	**Counter/Timer 5 Clock Source** — 00 = 6 MHz 01 = CTC4 10 = External Input 11 = Reserved
D4	CTC4MODE	**Counter/Timer 4 Clock Source** — 0 = 6 MHz 1 = External Input
D3	DIR3	**Direction Control for Digital I/O Port** — This bit controls the input/output direction of the digital I/O signals DIO31 – DIO24 DIR3 = 0 Input DIR3 = 1 Output
D2	DIR2	**Direction Control for Digital I/O Port** — This bit controls the input/output direction of the digital I/O signals DIO23 – DIO16. DIR2 = 0 Input DIR2 = 1 Output
D1	DIR1	**Direction Control for Digital I/O Port** — This bit controls the input/output direction of the digital I/O signals DIO15 – DIO8. DIR1 = 0 Input DIR1 = 1 Output
D0	DIR0	**Direction Control for Digital I/O Port** — This bit controls the input/output direction of the digital I/O signals DIO7 – DIO0. DIR0 = 0 Input DIR0 = 1 Output

ADC DATA HIGH REGISTER

ADCHI (READ) 1D9h (or 1E9h via the CMOS setup)

D7	D6	D5	D4	D3	D2	D1	D0
AD11 / 0	AD11 / 0	AD11 / 0	AD11 / 0	AD11	AD10	AD9	AD8

The ADCHI register is a read register containing the upper four bits of data from the A/D conversion results. It is used in conjunction with the ADCLO register to read the complete 12-bit data word.

When reading data, it is normal convention to read the ADCLO register first, followed by the ADCHI register.

Table 22: ADCHI Bit Assignments

Bit	Mnemonic	Description
D7-D4	AD11 / 0	**Sign Extension** — These four bits read as “0” in unipolar input mode (BIP = 0) In bipolar input mode, AD11 is duplicated (sign extended) into these four bits. ***Note:*** *These are read-only bits.*
D3-D0	AD11-AD8	**A/D Input Data (Most Significant Nibble)** — These bits contain data bits AD11 through AD8 of the conversion results. ***Note:*** *These are read-only bits.*

ADC DATA LOW REGISTER

ADCLO (READ) 1D8h (or 1E8h via the CMOS setup)

D7	D6	D5	D4	D3	D2	D1	D0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

The ADCLO register is a read register containing the lower eight bits of data from the A/D conversion results. It is used in conjunction with the ADCHI register to read the complete 12-bit data word.

After a conversion is complete (as reported by the DONE bit in the IIOCR register) the ADCLO register should be read first, followed by the ADCHI register. A word-wide input instruction from the ADCLO register (in ax,dx) fetches data from both registers in the proper sequence.

The data registers are located on an even address boundary to facilitate efficient single-cycle reading of the A/D data.

Table 23: ADCLO Bit Assignments

Bit	Mnemonic	Description
D7-D0	ADCDATA	**A/D Input Data (Least Significant Byte) —** These bits contain data bits AD7 through AD0 of the conversion results. ***Note:*** *These are read-only bits.*

TWO'S COMPLEMENT DATA FORMAT (±5V AND ±10V ONLY)

The A/D converter translates applied analog voltages into 12-bit, two's complement digital words. The full analog input range is divided into 4096 steps. The output code (0000h) is associated with a mid-range analog value of 0 Volts (ground).

The following formulas are used for calculating analog and digital values.

$$Digital = \left[\frac{Analog}{Step} \right] \qquad Analog = Step \times Digital$$

Where:

Analog = Applied voltage

Digital = A/D Conversion Data

Step = 0.004882813 Volts (±10V)
0.002441406 Volts (±5V)

Sample values are shown in the following table:

Table 24: Two's Complement Data Format

±5V Input Voltage	±10V Input Voltage	Hex	Decimal	Comment
+5.000000	+10.000000	—	—	Out of range
+4.997559	+9.995117	07FFh	2047	Maximum positive voltage
+2.500000	+5.000000	0400h	1024	Positive half scale
+1.250000	+2.500000	0200h	512	Positive quarter scale
+0.002441	+0.004883	0001h	1	Positive 1 LSB
0.000000	0.000000	0000h	0	Zero (ground input)
–0.002441	–0.004883	FFFFh	–1	Negative 1 LSB
–1.250000	–2.500000	FE00h	–512	Negative quarter scale
–2.500000	–5.000000	FC00h	–1024	Negative half scale
–5.000000	–10.000000	F800h	–2048	Maximum negative voltage

BINARY FORMAT (0 TO +5V AND 0 TO +10V ONLY)

The full analog input range is divided into 4096 steps. The output code (0000h) is associated with an analog input voltage of 0 Volts (ground). All codes are considered positive.

The following formulas are used for calculating analog and digital values:

$$Digital = \left[\frac{Analog}{Step} \right] \qquad Analog = Step \times Digital$$

Where:

Analog = Applied voltage

Digital = A/D Conversion Data

Step = 0.002441406 Volts (0 to +10V Range)
0.001220703 Volts (0 to +5V Range)

Sample values are shown in the following table:

Table 25: Binary Data Format

0 to +5V Input Voltage	0 to +10V Input Voltage	Hex	Decimal	Comment
+5.000000	+10.000000	—	—	Out of range
+4.998779	+9.997559	0FFFh	4095	Maximum voltage
+2.500000	+5.000000	0800h	2048	Half scale
+1.250000	+2.500000	0400h	1024	Quarter scale
+0.001220	+0.002441	0001h	1	1 LSB
0.000000	0.000000	0000h	0	Zero (ground input)

ANALOG INPUT CODE EXAMPLE

The following code example illustrates the procedure for reading ±10V analog voltage from channel 0:

```
        MOV   DX,1D8h
        MOV   AL,18H
        OUT   DX,AL       ;Select channel 0 and begin conversion
BUSY:   MOV   DX,1D3h
        IN    AL,DX       ;Get A/D status
        AND   AL,80h      ;Isolate the DONE bit
        JZ    BUSY        ;Loop back if conversion isn't complete
        MOV   DX,1D8h     ;Point to ADCLO register
        IN    AX,DX       ;16-bit input reads ADCLO and ADCHI into AX
```

USB Interface

The USB interface on the EBX-12 is UHCI (Universal Host Controller Interface) and EHCI (Enhance Host Controller Interface) compatible, which provides a common industry software/hardware interface. There are four USB ports available on the CBL-8003 or CBR-8005 breakout board, two at connector J5 and two at connector J6.

Note: The USB interface wiring changed from EBX-12 version 5.xx to 6.xx to improve USB performance. The USB interfaces are incompatible between the two versions. Be sure to use the correct breakout board assembly: CBL-8003 for version 5.xx and earlier, and CBR-8005 for version 6.xx and later. Using the incorrect breakout board will cause the USB interface to fail and may cause damage to the circuitry.

BIOS CONFIGURATION

The USB controller can be enabled or disabled in the CMOS setup. The USB controller uses PCI interrupt "INTA#" and "INTD#". The CMOS setup screen is used to select the IRQ line routed to each PCI interrupt line.

Table 26: USB Interface – Breakout Board Connector J5

Breakout J5 Top Pin	Signal Name	Function
1	USBP1PWR	+5V (Protected)
2	USBP1–	Channel 0 Data –
3	USBP1+	Channel 0 Data +
4	GND	Ground
Breakout J5 Bottom Pin	**Signal Name**	**Function**
1	USBP0PWR	+5V (Protected)
2	USBP0–	Channel 1 Data –
3	USBP0+	Channel 1 Data +
4	GND	Ground

Table 27: USB Interface – Breakout Board Connector J6

Breakout J6 Pin	Signal Name	Function
1	USBP2PWR	+5V (Protected)
2	USBP2–	Channel 2 Data –
3	USBP2+	Channel 2 Data +
4	GND	Cable Shield
5	GND	Ground
6	GND	Ground
7	GND	Cable Shield
8	USBP3+	Channel 3 Data +
9	USBP3–	Channel 3 Data –
10	USBP3PWR	+5V (Protected)

Warning! Connector J6 on the breakout board is not numbered in the conventional manner for dual-row headers. Care must be taken to attach the USB adapter cables, as shown in Figure 17, to prevent voltage reversal.

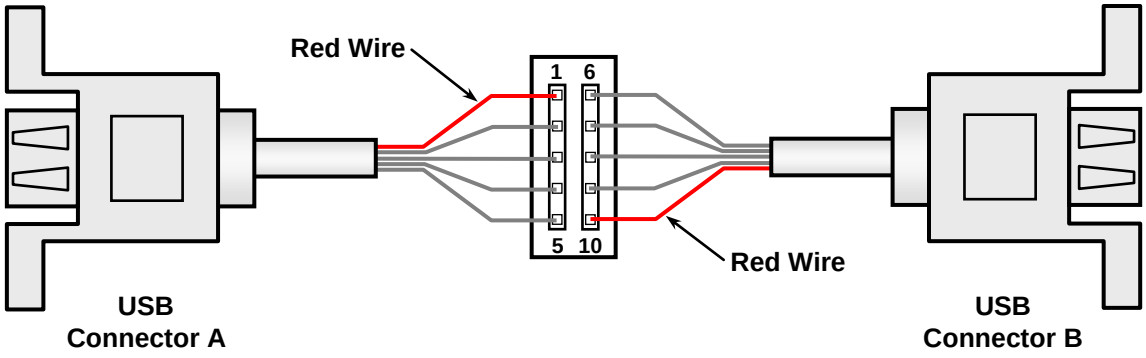


Figure 17. USB Connector Orientation Diagram

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Digital I/O Interface

The EBX-12 includes a 32-channel digital I/O interface. The digital lines are grouped as four 8-bit bi-directional ports. The direction of each port is controlled by software, and each signal is pulled up to +5V with a 10K ohm resistor.

The 24 mA source/sink drive and short protected outputs are an excellent choice for industrial TTL interfacing.

EXTERNAL CONNECTIONS

Table 28: Digital I/O Connector

CBL/CBR-8004 J2 Pin	Signal Name	Function
–	Ground	Ground
1	DIO0	Digital I/O 0
2	DIO1	Digital I/O 1
3	DIO2	Digital I/O 2
4	DIO3	Digital I/O 3
5	DIO4	Digital I/O 4
6	DIO5	Digital I/O 5
7	DIO6	Digital I/O 6
8	DIO7	Digital I/O 7
9	DIO8	Digital I/O 8
10	DIO9	Digital I/O 9
11	DIO10	Digital I/O 10
12	DIO11	Digital I/O 11
13	DIO12	Digital I/O 12
14	DIO13	Digital I/O 13
15	DIO14	Digital I/O 14
16	DIO15	Digital I/O 15
17	DIO16	Digital I/O 16
18	DIO17	Digital I/O 17
19	DIO18	Digital I/O 18
20	DIO19	Digital I/O 19
21	DIO20	Digital I/O 20
22	DIO21	Digital I/O 21
23	DIO22	Digital I/O 22
24	DIO23	Digital I/O 23
25	DIO24	Digital I/O 24
26	DIO25	Digital I/O 25
27	DIO26	Digital I/O 26
28	DIO27	Digital I/O 27
29	DIO28	Digital I/O 28
30	DIO29	Digital I/O 29
31	DIO30	Digital I/O 30
32	DIO31	Digital I/O 31
–	Ground	Ground
33	Ground	Ground
34	Ground	Ground

INTERRUPT GENERATION

The EBX-12 can be configured to issue interrupts on the transition (high to low or low to high) of DIO30 and DIO31. IRQ selection is done in the CMOS setup.

SIGNAL DIRECTION

The 32 I/O signals are divided into four 8-bit I/O ports. The direction of each port is controlled by the DIR0, DIR1, DIR2 and DIR3 bits in the IIOCR register. See page 53. All four 8-bit I/O ports are set to inputs on power on reset.

DIGITAL I/O DATA PORTS

DIOB3 (READ/WRITE) 1D7h (or 1E7h via the CMOS setup)

D7	D6	D5	D4	D3	D2	D1	D0
DIO31	DIO30	DIO29	DIO28	DIO27	DIO26	DIO25	DIO24

DIOB2 (READ/WRITE) 1D6h (or 1E6h via the CMOS setup)

D7	D6	D5	D4	D3	D2	D1	D0
DIO23	DIO22	DIO21	DIO20	DIO19	DIO18	DIO17	DIO16

DIOB1 (READ/WRITE) 1D5h (or 1E5h via the CMOS setup)

D7	D6	D5	D4	D3	D2	D1	D0
DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8

DIOB0 (READ/WRITE) 1D4h (or 1E4h via the CMOS setup)

D7	D6	D5	D4	D3	D2	D1	D0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0

Table 29: Register Bit Assignments

Bit	Mnemonic	Description
D7-D0	DIO31 – DIO24 DIO23 – DIO16 DIO15 – DIO8 DIO7 – DIO0	**Digital I/O Data** — Data written to these register is driven onto the Digital I/O port signals when the port direction is set to output mode. When the port is in input mode, these bits reflect the input state of the signal lines. 0 = Signal low (GND) 1 = Signal high (+5V) All bits are set to logic high on power on reset.

Auxiliary Timer/Counter Channels

The EBX-12 includes three uncommitted 8254 type counter/timer channels for general program use. Control signals for the three channels are available on connector J8.

CONFIGURATION

IIOCR Register 1D3h (or 1E3h) selects the clock source for channels 4 and 5. See page 53. Options include:

- Internal 6 MHz timebase
- External clock from connector J8
- Cascading channels 4 and 5 together for 32-bit counter/timer operations

EXTERNAL CONNECTIONS

Table 30: Counter/Timer I/O Connector

CBL/CBR-8004 J5 Pin	Signal Name	Function
1	OCTC3	CTC Channel 3 Output
2	GCTC3	CTC Chan 3 Gate Input
3	ICTC4	CTC Channel 4 Input
4	GND	Digital Ground
5	OCTC4	CTC Channel 4 Output
6	GCTC4	CTC Chan 4 Gate Input
7	ICTC5	CTC Channel 5 Input
8	GND	Digital Ground
9	OCTC5	CTC Channel 5 Output
10	GCTC5	CTC Chan 5 Gate Input

COUNTER / TIMER REGISTERS

Table 31: Counter / Timer Registers

Mnemonic	R/W	Address	Name
T3CNT	R/W	1DCh or 1ECh	Timer 3 Count Load/Read
T4CNT	R/W	1DDh or 1EDh	Timer 4 Count Load/Read
T5CNT	R/W	1DEh or 1EEh	Timer 5 Count Load/Read
TCW	W	1DFh or 1EFh	Timer Control Word

OPERATION

Operational details for this industry standard 8254 type counter/timer chip are beyond the scope of this manual. Register details, operational modes and programming information can be obtained from the VersaLogic website by downloading the 8254.PDF data sheet.

PC/104 Expansion Bus

The EBX-12 will accept up to eight expansion modules, up to four of which can be PC/104-*Plus* (PCI) expansion modules.

ARRANGING THE STACK

If PC/104-*Plus* modules used, they go on the stack first (closest to the EBX-12 circuit board). The first module is called "slot 0", the next module is "slot 1", and the third module is "slot 2". Make sure to correctly configure the "slot position" jumpers on each PC/104-*Plus* module to match its physical position in the stack.

PC/104 modules are stacked on top of the PC/104-*Plus* modules; 16-bit modules first, followed by 8-bit PC/104 modules. Lastly, non-standard modules, which lack feed through connectors, should be assembled on top of the stack.

I/O CONFIGURATION

PC/104 (ISA) Modules

PC/104 I/O modules should be addressed in the 100h – 3FFh, address range. Care must be taken to avoid the I/O addresses shown in the *On-Board I/O Devices* table on page 64. These ports are used by on-board peripherals and video devices.

PC/104-Plus *(PCI) Modules*

The BIOS automatically configures the I/O, memory and interrupt resources of PC/104-*Plus* modules. The CMOS setup may be used to disable modules or select IRQ assignment.

Memory and I/O Map

MEMORY MAP

The lower 1 MB memory map of the EBX-12 is arranged as shown in the following table.

Various blocks of memory space between C0000h and FFFFFh can be shadowed. The CMOS setup is used to enable or disable this feature.

Table 32: Memory Map

Start Address	End Address	Comment
E0000h	FFFFFh	System BIOS
D0000h	DFFFFh	PC/104
C0000h	CFFFFh	Video BIOS
A0000h	BFFFFh	Video RAM
00000h	9FFFFh	System RAM

I/O MAP

The following table lists the I/O devices in the EBX-12 I/O map. User I/O devices should be added with care to avoid the devices already in the map as shown in the following table.

Table 33: On-Board I/O Devices

I/O Device	Standard I/O Addresses	Alternate * I/O Addresses
Super I/O	02Eh-02Fh	
Super I/O (COM 3 & 4)	4Eh-4Fh	
Secondary Hard Drive Controller	170h – 177h	
Special Control Register	1D0h	1E0h
Watchdog Hold-Off Register	1D1h	1E1h
Jumper and Status Register	1D2h	1E2h
Industrial I/O Control Register	1D3h	1E3h
Digital I/O Data Register Byte 0	1D4h	1E4h
Digital I/O Data Register Byte 1	1D5h	1E5h
Digital I/O Data Register Byte 2	1D6h	1E6h
Digital I/O Data Register Byte 3	1D7h	1E7h
Analog Control / ADC Low Register	1D8h	1E8h
ADC High Data Register	1D9h	1E9h
Timer 3 Count Load/Read	1DCh	1ECh
Timer 4 Count Load/Read	1DDh	1EDh
Timer 5 Count Load/Read	1DEh	1EEh
Timer Control Word	1DFh	1EFh
Primary Hard Drive Controller	1F0h– 1F7h	
COM4 Serial Port	2E8h– 2EFh	
COM2 Serial Port	2F8h– 2FFh	
LPT1 Parallel Port	378h– 37Fh	
SVGA Video	3B0h– 3DFh	
COM3 Serial Port	3E8h– 3EFh	
Floppy Disk Controller	3F0h– 3F7h	
COM1 Serial Port	3F8h– 3FFh	

** User selectable via CMOS setup*

Note: The I/O ports occupied by on-board devices are freed up when the device is disabled in the CMOS setup.

Interrupt Configuration

The EBX-12 has the standard complement of PC type interrupts. Ten non-shared interrupts are routed to the PC/104 bus, and up to four IRQ lines can be allocated as needed to PCI devices.

There are no interrupt configuration jumpers. All configurations are handled through the CMOS setup. The switches in Figure 18 indicate the various CMOS setup options. Closed switches show factory default settings.

Note: If your design needs to use interrupt lines on the PC/104 bus, IRQ5, IRQ9 and/or IRQ10 are recommended.

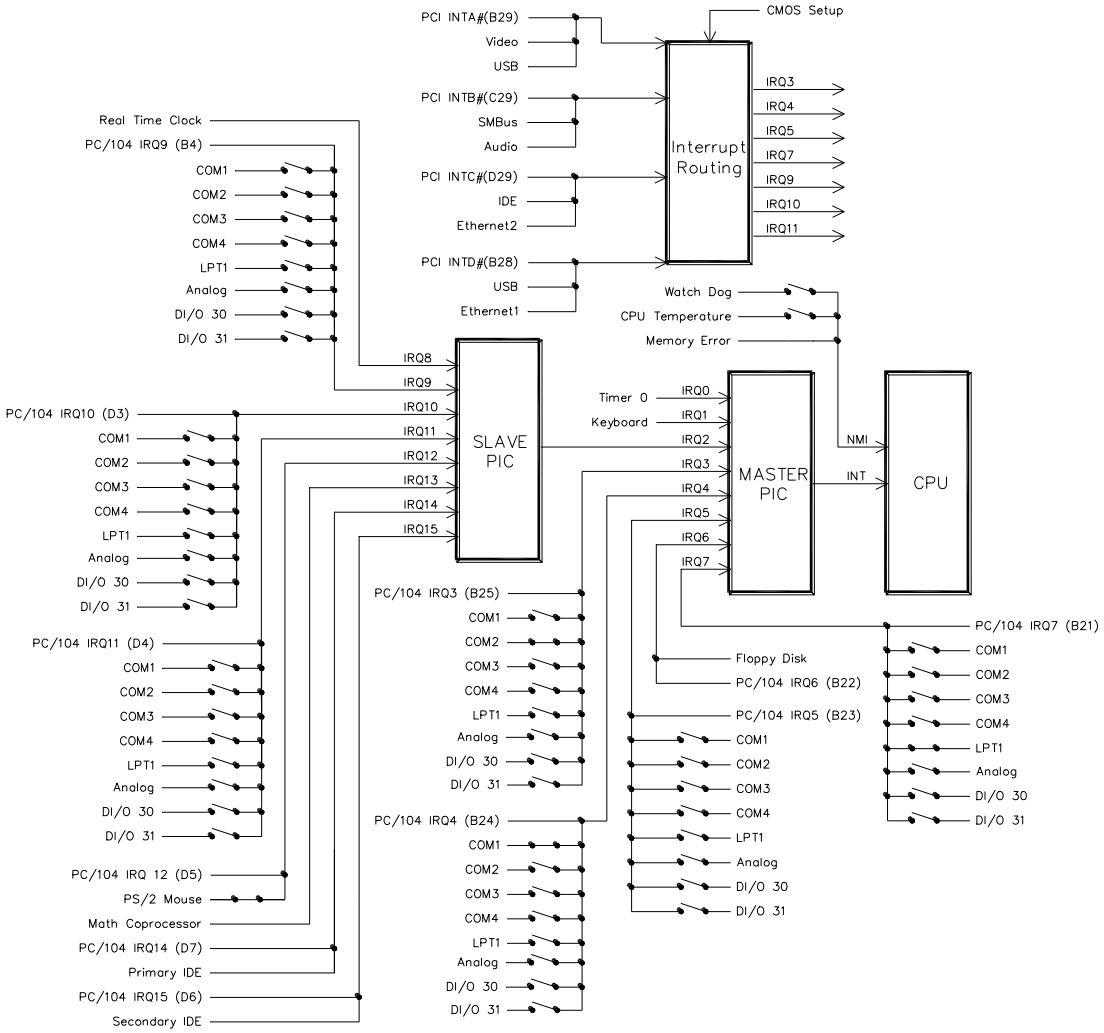


Figure 18. Interrupt Circuit Diagram

Special Control Register

SCR (READ/WRITE) 1D0h (or 1E0h via the CMOS setup)

D7	D6	D5	D4	D3	D2	D1	D0
PLED	Reserved	OVERTEMP	HDOGNMI	COM4DIR	COM3DIR	WDOG_NMI	WDOG_RST

Table 34: Special Control Register Bit Assignments

Bit	Mnemonic	Description
D7	PLED	**Light Emitting Diode** — Controls the programmable LED on connector J4 0 = Turns LED off 1 = Turns LED on
D6	Reserved	**Reserved** — This bit has no function.
D5	OVERTEMP	**Temperature Status —** Indicates CPU temperature. 0 = CPU temperature is below value set in the CMOS setup 1 = CPU temperature is above value set in the CMOS setup ***Note:*** *This bit is a read-only bit.*
D4	HDOGNMI	**Non-Maskable Interrupt Enable** — Controls the generation of NMI whenever the CPU temperature sensor detects an over-temperature condition 0 = Disable 1 = Enable
D3	COM4DIR	**COM4 RS-485 Transmit Enable** — Enables the RS-485 transmitter 0 = Receive 1 = Transmit
D2	COM3DIR	**COM3 RS-485 Transmit Enable** — Enables the RS-485 transmitter 0 = Receive 1 = Transmit
D1	WDOG_NMI	**Watchdog Non-Maskable Interrupt Enable** — Enables the generation of a NMI when the watchdog timer expires 0 = Disabled 1 = Enabled
D0	WDOG_RST	**Watchdog Reset Enable** — Enables and disables the watchdog timer reset circuit 0 = Disabled 1 = Enabled

Revision Indicator Register

REVIND (READ ONLY) 1D1h (or 1E1h via the CMOS setup)

D7	D6	D5	D4	D3	D2	D1	D0
PC4	PC3	PC2	PC1	PC0	REV2	REV1	REV0

This register is used to indicate the revision level of the EBX-12.

Table 35: Revision Indicator Register Bit Assignment

Bit	Mnemonic	Description
D7-D3	PC4-PC0	**Product Code —** These bits are hard-coded to represent the product type. The EBX-12 always reads as 11000. Other codes are reserved for future products. **PC4 PC3 PC2 PC1 PC0 Product Code** 1 1 0 0 0 EBX-12 ***Note:*** *These bits are read-only.*
D2-D0	REV2-REV0	**Revision Level —** These bits represent the EBX-12 circuit revision level. **REV2 REV1 REV0 Revision Level** 0 0 0 Initial product release, all EBX-12b, d, f, bu, du revisions before Rev 5.01 1 0 0 Initial product release, all EBX-12e revisions before Rev 5.01. 0 0 1 Rev 5.01 or later EBX-12b, d, g, bu, du Rev 6.01 or later EBX-12p, r, v 1 0 1 Rev 5.01 or later EBX-12e, er, eu, k Rev 6.01 or later EBX-12t ***Note:*** *These bits are read-only.*

Watchdog Timer Hold-Off Register

WDHOLD (WRITE ONLY) 1D1h (or 1E1h via the CMOS setup)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0

A watchdog timer circuit is included on the EBX-12 board to reset the CPU and/or generate a NMI if proper software execution fails or a hardware malfunction occurs. The watchdog timer is controlled by the SCR.

If the watchdog timer is enabled, software must periodically refresh the watchdog timer at a rate faster than the timer is set to expire (1000 ms minimum). Writing 5Ah to WDHOLD resets the watchdog timeout period.

Jumper and Status Register

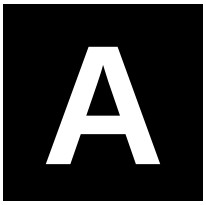
JSR (READ/WRITE) 1D2h (or 1E2h via the CMOS setup)

D7	D6	D5	D4	D3	D2	D1	D0
GPI	VB-SEL	SB-SEL	Reserved	Reserved	WDOG_STA	DINTHI	DINTLO

Table 36: Jumper and Status Register Bit Assignments

Bit	Mnemonic	Description
D7	GPI	**General Purpose Input** — Indicates the status of jumper V1[5-6] 0 = Jumper Out 1 = Jumper In ***Note:*** *This is a read-only bit.*
D6	VB-SEL	**Video BIOS Selection** — Indicates the status of jumper V1[3-4] 0 = Jumper out, Secondary Video BIOS selected. 1 = Jumper in, Primary Video BIOS selected. ***Note:*** *This is a read-only bit.*
D5	SB-SEL	**System BIOS Selection** — Indicates the status of jumper V1[1-2] 0 = Jumper out, Master System BIOS selected. 1 = Jumper in, Run Time System BIOS selected. ***Note:*** *This is a read-only bit.*
D4-D3	Reserved	**Reserved** — These bits have no function.
D2	WDOG_STA	**Watchdog Status** — Indicates if the watchdog timer has expired 0 = Timer has not expired 1 = Timer has expired ***Note:*** *Clear bit by writing a 1 to it.*
D1	DINTHI	**Digital Interrupt High** — Indicates transition was detected on DI/0 31 0 = No Transition Detected 1 = Transition Detected ***Note:*** *Clear bit by writing a 1 to it.*
D0	DINTLO	**Digital Interrupt Low** — Indicates transition was detected on DI/0 30 0 = No Transition Detected 1 = Transition Detected ***Note:*** *Clear bit by writing a 1 to it.*

Appendix A — Other References



PC Chipset *855GME Chipset*	Intel Corporation (http://developer.intel.com/sites/developer)
Ethernet Controller *Intel 82541ER* *Intel 82551ER*	Intel Corporation (http://developer.intel.com/sites/developer)
Video Controller Extreme Graphics 2 Chip Set	Intel Corporation (http://developer.intel.com/sites/developer)
PC/104 Specification *PC/104 Resource Guide*	PC/104 Consortium (www.controlled.com/pc104)
PC/104-*Plus* Specification *PC/104 Resource Guide*	VersaLogic Corporation (www.VersaLogic.com)
CPU Chips *Pentium M® /Celeron M®*	Intel Corporation (http://developer.intel.com/sites/developer)
General PC Documentation *The Programmer's PC Sourcebook*	Microsoft Press (www.microsoft.com/learning/books)
General PC Documentation *The Undocumented PC*	Powell's Books (www.powells.com)