EC6696

4-Channel WD1(960H)/D1 Video Decoders and Audio Codecs
For Security Surveillance Application

Preliminary Data Sheet from ECHIP, Inc

Disclaimer

Catalog

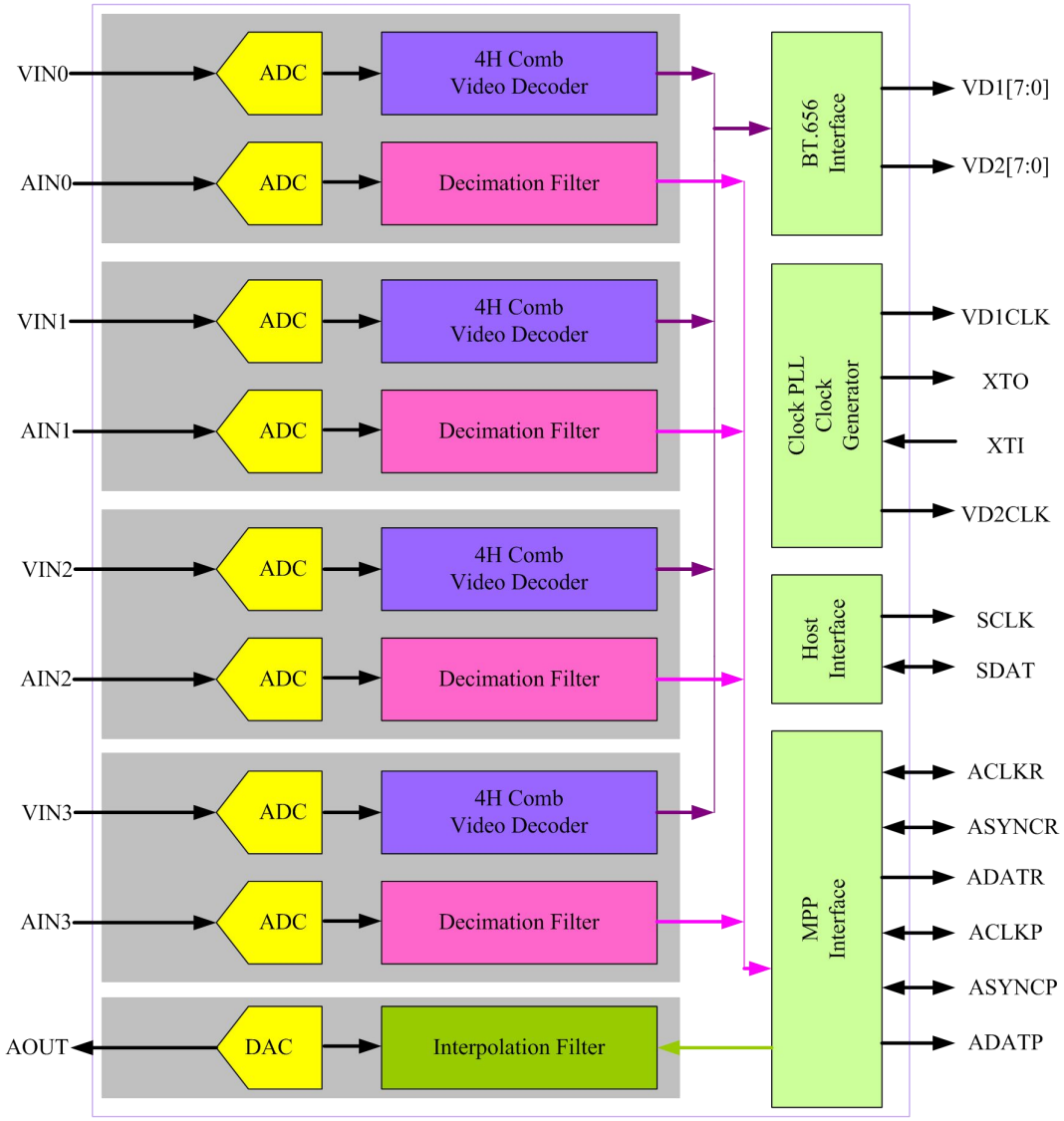
1. Introduction

The EC6696 includes four high quality NTSC/PAL video decoders that convert analog composite video signal to digital component YCbCr data for security application. Each channel contains 10 bit ADC and proprietary clamp and gain controllers and utilizes 3H comb filter for separating luminance & chrominance to reduce cross noise artifacts. The EC6696 adopts the image enhancement techniques such as IF compensation filter, CTI and programmable peaking. The EC6696 also includes audio CODEC which has four audio Analog-to-Digital converters and one Digital-to-Analog converter. A built-in audio controller can generate digital outputs for recording/mixing and accepts digital input for playback.

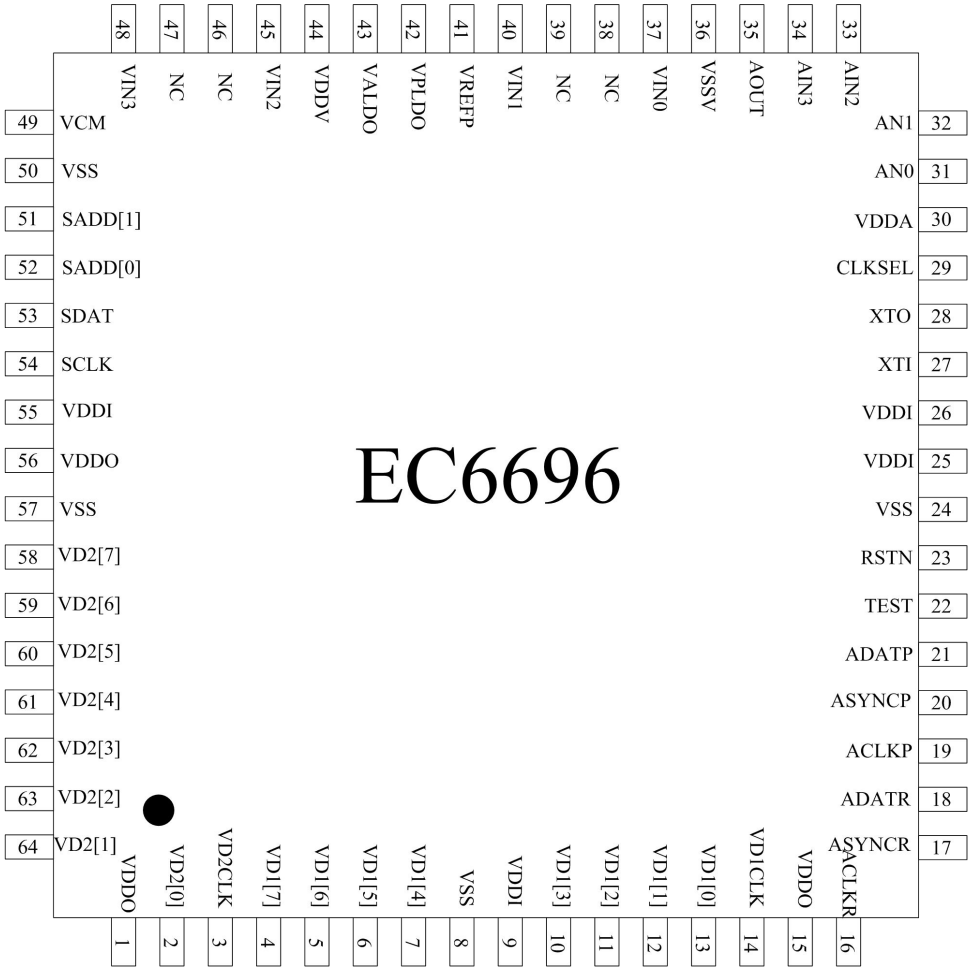
1.1 Features

- WD1(960H) and D1 compatible video decoding operation and it is programmable each channel
- Accepts all NTSC(M) / PAL(B/D/G/H/I/K/L/M) standards with auto detection.
- Integrated four video analog anti-aliasing filter and 10 bit CMOS ADCs.
- High performance adaptive 4H comb filters for all NTSC/PAL standards.
- IF compensation filter for improvement of color demodulation.
- Color Transient Improvement.
- Automatic white peak control.
- Programmable hue, saturation, contrast, brightness and sharpness.
- Proprietary fast video locking system for non-realtime application.
- ITU-R BT.656 like YCbCr(4:2:2) output or time multiplexed output with 27/54/108MHz for D1 or 36/72/144MHz for WD1 format.
- Provides simultaneous four channel Full D1 with 108MHz or Full WD1 with 144MHz.
- Integrated four audio ADCs and one audio DAC.
- Provides multi-channel audio mixed analog output.
- Supports I2S/DSP Master/Slave interface for record output and playback input.
- PCM 8/16 bit and u-Law/A-Law 8bit for audio word length.
- Programmable audio sample rate that covers popular frequencies of 8/16/32/44.1/48kHz.
- Supports a two-wire serial host interface.
- Integrated clock PLL for 108MHz clock output.
- Ultra low power consumption.
- 64pin LQFP package.

1.2 Block Diagram



1.3 Pin Diagram



1.4 Pin Description

Analog Video/Audio Interface Pins

Name	Number	Type	Description
VIN0	37	A	Composite video input of channel 1.
VIN1	40	A	Composite video input of channel 2.
VIN2	45	A	Composite video input of channel 3.
VIN3	48	A	Composite video input of channel 4.
AIN0	31	A	Audio input of channel 1.
AIN1	32	A	Audio input of channel 2.
AIN2	33	A	Audio input of channel 3.
AIN3	34	A	Audio input of channel 4.
AOUT	35	A	Audio mixing output.
VREFP	41	A	0.66V voltage reference for video ADC.
VPLDO	42	A	PGA LDO de-cap pin, not connect.
VALDO	43	A	ADC LDO de-cap pin, connect to 2uf and 0.1uf.
VCM	49	A	ADC VCM de-cap, connect to 1uf to GND.

Digital Video/Audio Interface Pins

Name	Number	Type	Description
VD1[7:0]	4,5,6,7,10, 11,12,13	O	Video data output of channel 1.
VD2[7:0]	2,58,59,60, 61,62,63,64	O	Video data output of channel 2.
VD1CLK	14	O	The clock of channel 1 video data output.
VD2CLK	3	O	The clock of channel 2 video data output.
ACLKR	16	IO	Audio serial clock input/output of record.
ASYNCR	17	IO	Audio serial sync input/output of record.
ADATR	18	O	Audio serial data output of record.
ACLKP	19	IO	Audio serial clock input/output of playback.
ASYNCP	20	IO	Audio serial sync input/output of playback.
ADATP	21	I	Audio serial data input of playback.

System Control Pins

Name	Number	Type	Description
RSTN	23	I	System reset.
XTI	27	I	Crystal 27MHz connection or Oscillator clock input.
XTO	28	O	For crystal 27MHz connection.
TEST	22	I	Test pin. Connect to ground.
SCLK	54	I	Serial control clock line.
SDAT	53	IO	Serial control data line.
SADD[1:0]	51,32	I	Serial control address.
CLKSEL	29	I	Clock for chip mode select pin, 1 for 960h, 0 for D1.
TEST	22	I	For test, connect to GND.

Power and Ground Pins

Name	Number	Type	Description
VDDI	9,25,26,55	P	1.2V Power for internal logic.
VDDO	1,15,56	P	3.3V Power for output driver.
VSS	8,24,50,57	G	Ground for internal logic and output driver.
VDDV	44	P	3.3V Power for analog video ADC.
VSSV	36	G	Ground for analog video and audio ADC .
VDDA	30	P	3.3V Power for analog audio.

2. Function Description

2.1 Video Input Formats

The EC6696 has build-in automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency and frame rate to identify NTSC, PAL color signals. The standards that can be identified are NTSC(M) and PAL(B,D,G,H,I,M),. Each standard can be included or excluded in the standard recognition process by software control. The exceptions are the base standard NTSC and PAL, which are always enabled. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection.

EC6696 supports all common video formats as shown in Table1.

Table1. Video Input Formats Supported by the EC6696

Format	Lines	Fields	Fsc	Country
NTSC-M	525	60	3.5795 MHz	U.S,. many others
NTSC-Japan	525	60	3.5795 MHz	Japan
PAL-B,G,N	625	50	4.4336 MHz	Many
PAL-D	625	50	4.4336 MHz	China
PAL-H	625	50	4.4336 MHz	Belgium
PAL-I	625	50	4.4336 MHz	Great Britain, others
PAL-M	525	60	3.5795MHz	Brazil

2.2 Analog Frontend

The EC6696 contains four 10-bit ADC (Analog to Digital Converters) to digitize the analog video inputs. The EC6696 also contains an anti-aliasing filter to prevent out-of-band frequency in analog video input signal. So there is no need of external components in analog input pin except ac coupling capacitor and termination resistor. The following Fg1 shows the frequency response of the anti-aliasing filter.

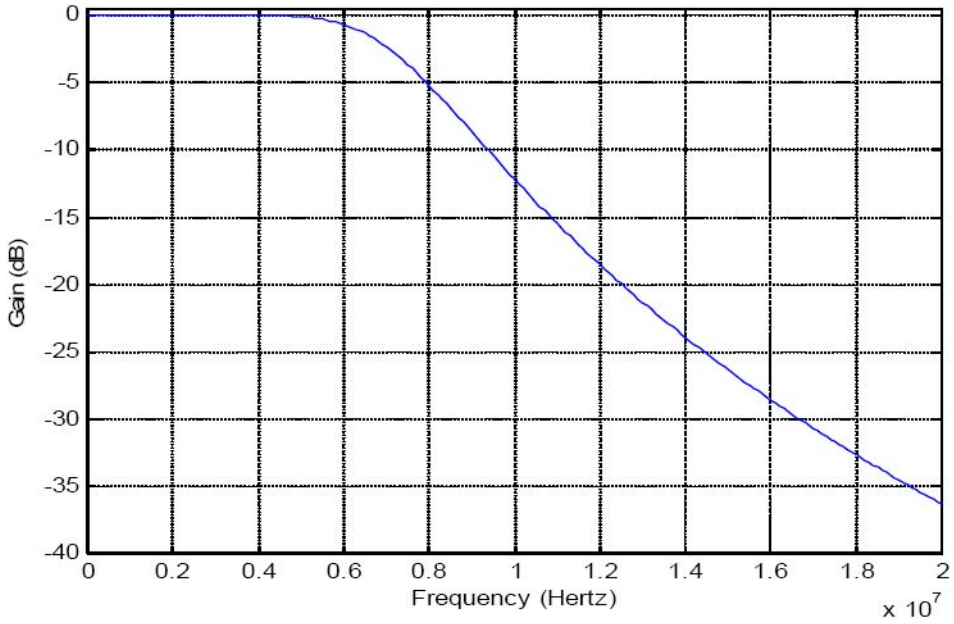


Fig1 The frequency response of anti-aliasing filter

2.2.1 Decimation Filter

The digitized composite video data are over-sampled to simplify the design of analog filter. The decimation filter is required to achieve optimum performance and prevent high frequency components form being aliased back into the video image when down-sampled. Fig2 shows the characteristic of the decimation filter.

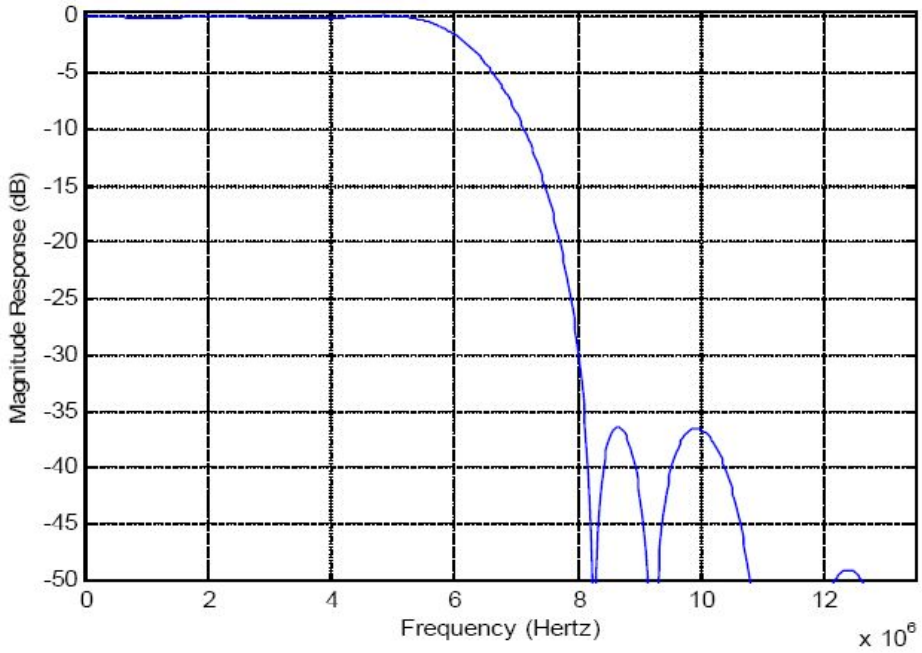


Fig2 The Characteristic of the Decimation Filter

2.3 Automatic Gain Control and Clamping

All four analog channels have built-in clamping circuit that restores the signal DC level. The Y channel restores the back porch of the digitized video to a programmable level (default is 64). This operation is automatic through internal feedback loop. The Automatic Gain Control (AGC) of the Y channel adjusts input gain so that the sync tip is at a desired level. Programmable white peak protection logic is included to prevent saturation in the case of abnormal signal proportion between sync and white peak level.

2.4 Sync Processing

The sync processor of EC6696 detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal of an S-video or component signal. The processor contains decision logic to achieve reliable sync detection in stable signal as well as in unstable signals such as those from VCR fast forward or backward.
The vertical sync separator detects the vertical synchronization pattern in the input video signals. In addition, the actual sync determination is controlled by a detection window to provide more reliable synchronization. An option is available to provide faster responses for certain applications. The field status is determined at vertical synchronization time. The field logic can also be controlled to toggle automatically while tracking the input

2.5 Y/C Separation

The color-decoding block contains the luma/chroma separation for the composite video signal and multi-standard color demodulation. For NTSC and PAL standard signals, the luma/chroma separation can be done either by comb filter or notch/band-pass filter combination. The default selection for NTSC/PAL is comb filter.

In the case of comb filter, the EC6696 separates luma (Y) and chroma (C) of a NTSC/PAL composite video signal using a proprietary 4H adaptive comb filter. The filter uses a four-line buffer. Adaptive logic combines the upper-comb and the lower-comb results based on the signal changes among the previous, current and next lines. This technique leads to excellent Y/C separation with small cross luma and cross color at both horizontal and vertical edges

Due to the line buffer used in the comb filter, there are always two lines processing delay at the output except for the component input mode which has only one line delay.

If notch/band-pass filter is selected, the characteristics of the filters are shown in the filter curve section.

The Fig3 shows the frequency response of notch filter for each system NTSC and PAL. The Fig4 shows the frequency response of Chroma Band Pass Filter Curves.

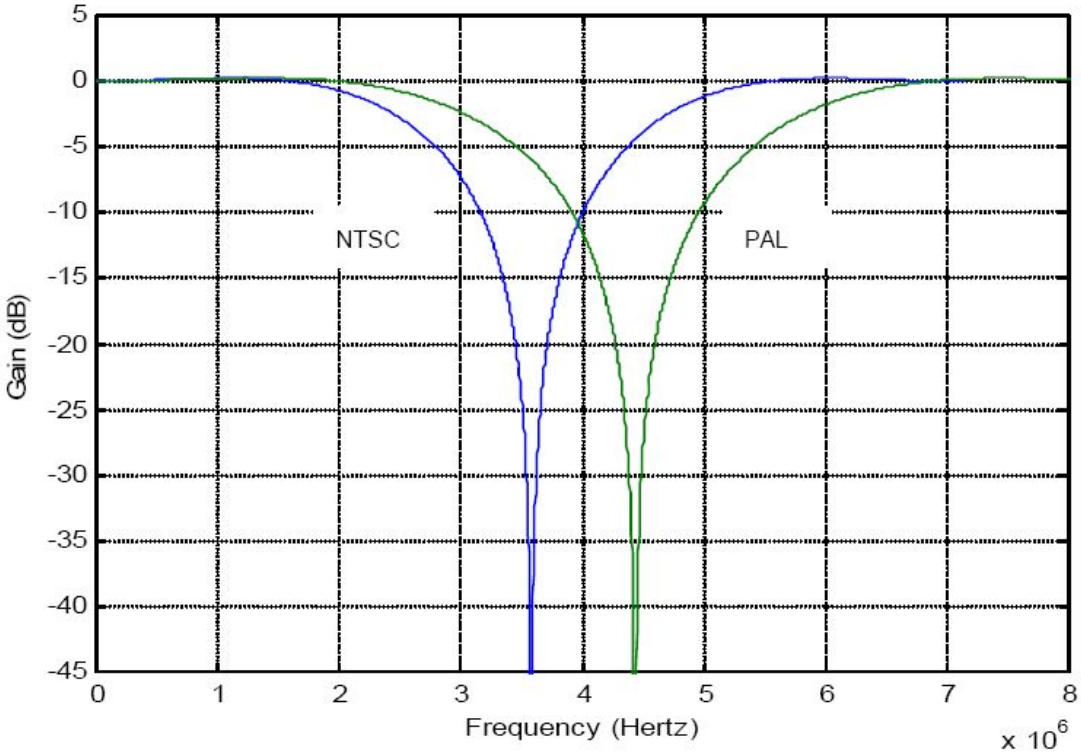


Fig3 The Characteristics of Luminance Notch Filter for PAL

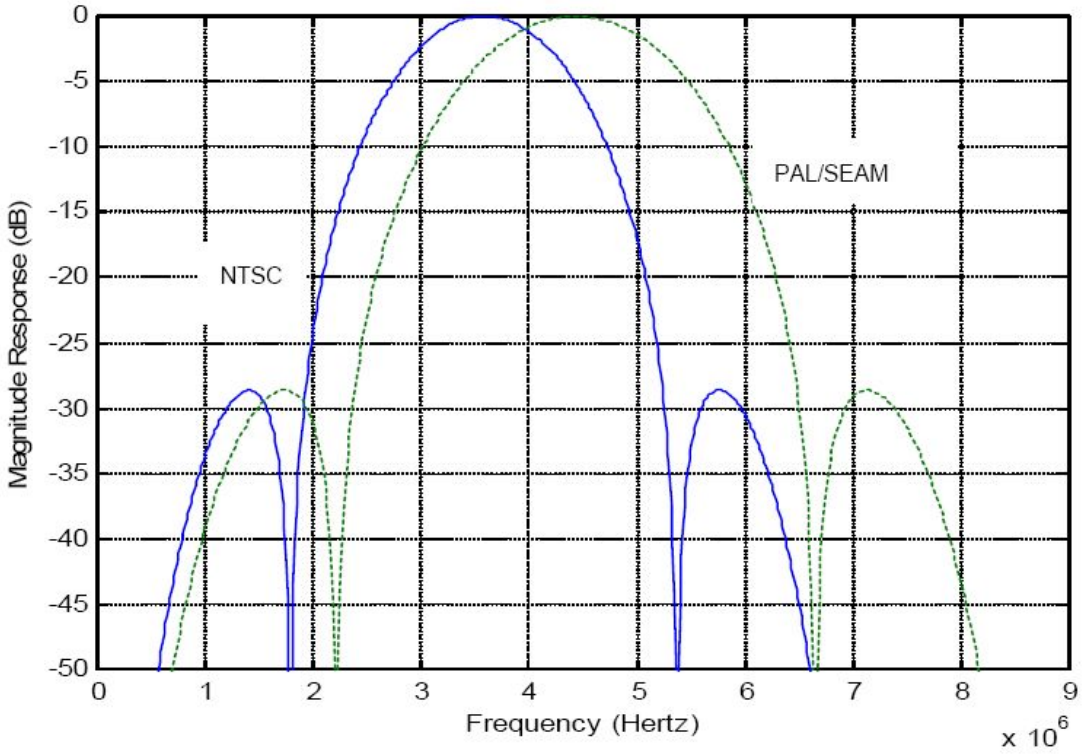


Fig4 Chroma Band Pass Filter Curves

2.6 Color Decoding

2.6.1 Chrominance Demodulation

The color demodulation for NTSC and PAL standard is done by first quadrature mixing the chroma signal to the base band. A low-pass filter is then used to remove carrier signal and yield chroma components. The low-pass filter characteristic can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

The sub-carrier signal for use in the color demodulator is generated by direct digital synthesis PLL that locks onto the input sub-carrier reference (color burst). This arrangement allows any sub-standard of NTSC and PAL to be demodulated easily with single crystal frequency.

2.6.2 ACC (Automatic Color gain control)

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by high-frequency loss in video signal. In the NTSC/PAL standard, the color reference signal is the burst on the back porch.

2.7 Chrominance Processing

2.7.1 Chrominance Gain, Offset and Hue Adjustment

When decoding NTSC signals, EC6696 can adjust the hue of the chroma signal. The hue is defined as a phase shift of the subcarrier with respect to the burst. This phase shift of NTSC decoding can be programmed through a control register. For the PAL standard, the PAL delay line is provided to compensate any hue error; therefore, there is no hue adjustment available. The color saturation can be adjusted by changing the gain of Cb and Cr signals for all NTSC and PAL formats. The Cb and Cr gain can be adjusted independently for flexibility.

2.7.2 CTI (Color Transient Improvement)

The EC6696 provides the Color Transient Improvement function to further enhance the image quality. The CTI enhance the color edge transient without any overshoot or under-shoot.

2.8 Luminance Processing

The EC6696 adjusts brightness by adding a programmable value to the Y signal. It adjusts the picture contrast by changing the gain of the Y signal.

The EC6696 also provide programmable peaking function to further enhance the video sharpness. The peaking control has built-in coring function to prevent enhancement of noise.

2.9 Video Cropping

Cropping allows only subsection of a video image to be output. The active video region is determined by HDELAY, HACTIVE, VDELAY and VACTIVE register as illustrated in Fig5.The VACTIVE signal can be programmed to indicate the number of active lines to be displayed in a video field, and the HACTIVE signal can be programmed to indicate the number of active pixels to be displayed in a video line. The start of the field or frame in the vertical direction is indicated by the leading edge of VSYNC. The start of the line in the horizontal direction is indicated by the leading edge of the HSYNC. The start of the active lines from vertical sync edge is indicated by the VDELAY register. The start of the active pixels from the horizontal edge is indicated by the HDELAY register. The sizes and location of the active video are determined by HDELAY, HACTIVE, VDELAY and VACTIVE registers.

The Horizontal crop register (HDELAY) determines the number of pixels delay between the leading edge of HSYNC and the leading edge of the HACTIVE. Note that this value is referenced to the un-scaled pixel number. The Horizontal active register (HACTIVE) determines the number of active pixels to be output or scaled after the delay from the sync edge is met. This value is also referenced to the un-scaled pixel number. Therefore, if the scaling ratio is changed, the active video region used for scaling remain unchanged as set by the HACTIVE register, but the valid pixels output are equal or reduced due to down scaling. In order for the cropping to work properly, the following equation should be satisfied.

HDELAY + HACTIVE < Total number of pixels per line.

For NTSC output at 13.5 MHz pixel rate, the total number of pixels is 858.For PAL output at 13.5 MHz rate, the total number of pixels is 864. HACTIVE should be set to 720.

The Vertical crop register (VDELAY) determines the number of lines delay between the leading edge of the VSYNC and the start of the active video lines. It indicates number of lines to skip at the start of a frame before asserting the VACTIVE signal. This value is referenced to the incoming scan lines before the vertical scaling. The number of scan lines is 525 for the 60Hz systems and 625 for the 50Hz systems. The Vertical active register (VACTIVE) determines the number of lines to be used in the vertical scaling. Therefore, the number of scan lines output is equal or less than the value set in this register depending on the vertical scaling ratio. In order for the vertical cropping to work properly, the following equation should be observed.

VDELAY + VACTIVE < Total number of lines per field

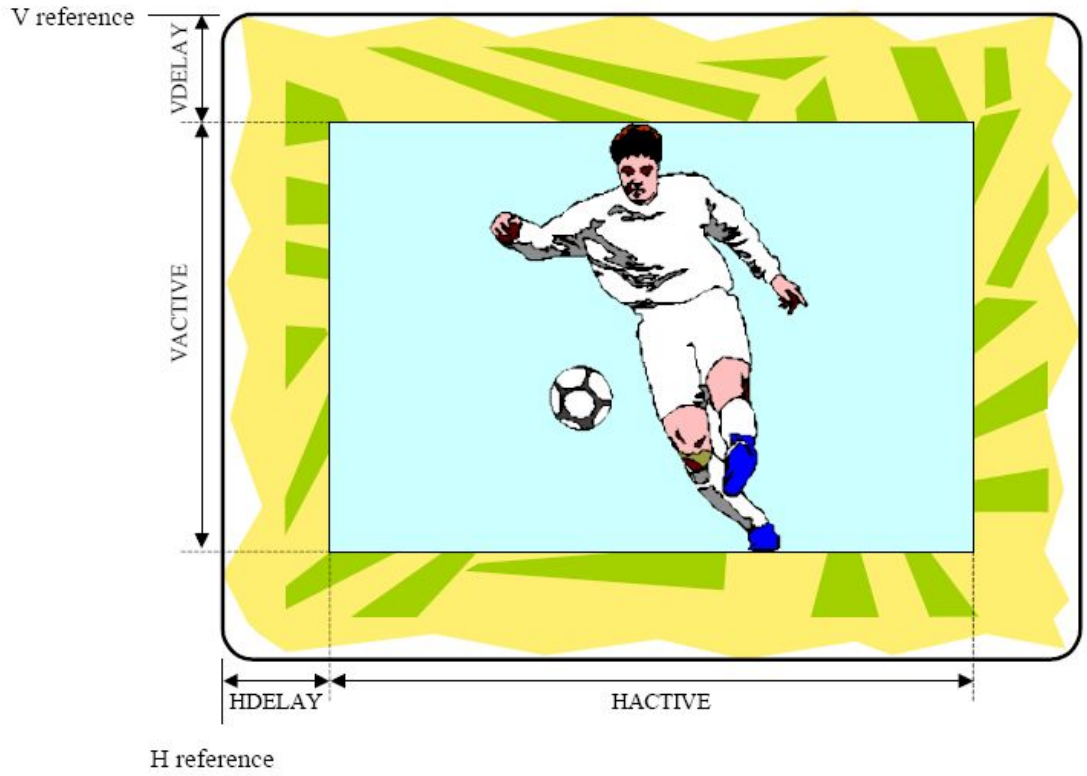


Fig5 The Effect of Cropping Registers

2.10 Video Scaler

The EC6696 can independently reduce the output video image size in both horizontal and vertical directions using the HOR_DEC and VER_DEC. The HOR_DEC register's value can decide the point picked from every one, two or four points. The VER_DEC register's value can decide the line picked from every one, two or four lines.

2.11 Output Format

The EC6696 supports a standard ITU-R BT.656 format. All video data and timing signal of four channels are synchronous with the pins CLKPOn and CLKNOn output. Therefore, CLKPOn or CLKNOn can be connected to four channel interfaces for synchronizing data. And, (the phase of CLKPOn or CLKNOn can be contr) the polarity of the CLKPOn and CLKNOn can be controlled via the CLKPOn_POL or CLKNOn_POL registers independently.

2.11.1 ITU-R BT.656 Format

In ITU-R BT.656 format, SAV and EAV sequences are inserted into the data stream to indicate the active video time. It is noted that the number of active pixels per line is constant in this mode regardless of the actual incoming line length. The output timing is illustrated in Fig6. The SAV and EAV sequences are shown in Table2. An optional set of 656 SAV/EAV code sequence can be enabled to identify no-video status using the NOVID_656 bit.

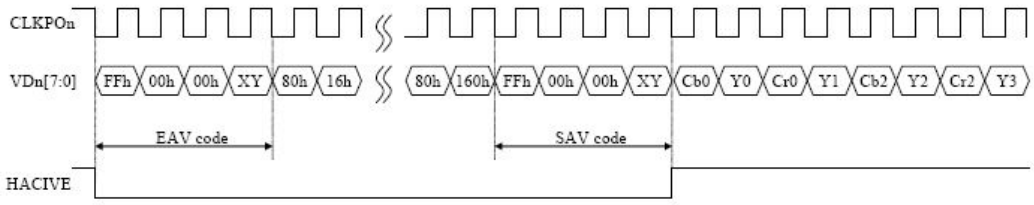


Fig6 Timing Diagram of ITU-R BT.656 format

Table2 ITU-R BT.656 SAV and EAV Code Sequence

Condition			656 FVH Value			SAV/EAV Code Sequence				
Field	V time	H time	F	V	H	First	Second	Third	Fourth	
									Normal	Option
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF1	0x71
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xEC	0x6C
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xDA	0x5A
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC7	0x47
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB6	0x36
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xAB	0x2B
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x9D	0x1D
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x00

2.11.2 Two Channel ITU-R BT.656 Time-multiplexed Format with 54/72MHz

The EC6696 supports two channels ITU-R BT.656 time-multiplexed format with (54MHz/72MHz) that is useful to security application requiring two channel outputs through one channel video port. The CHMDn register enables the dual ITU-R BT.656 time-multiplexed with its own channel ID can be inserted in the data stream using the CHID_MD register. Two kinds of channel ID format can be supported. One is horizontal blanking code with channel ID and the other is ITU-R BT.656 sync code with channel ID. The following Fig7 illustrates the logical timing diagram in the case of CH1 and CH2 time-multiplexed output through CH1 video output port. Fig8 illustrate VDn[7:0]/CLKPOn/CLKNOn pin default timing with (54MHz/72MHz) clock output mode.

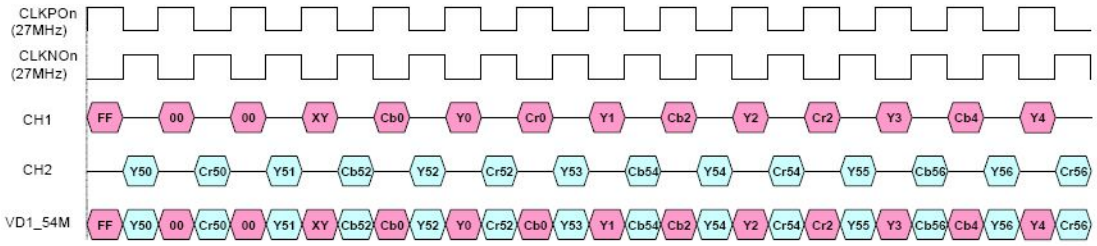


Fig7 Timing Diagram of Two Channel Time-multiplexed Format

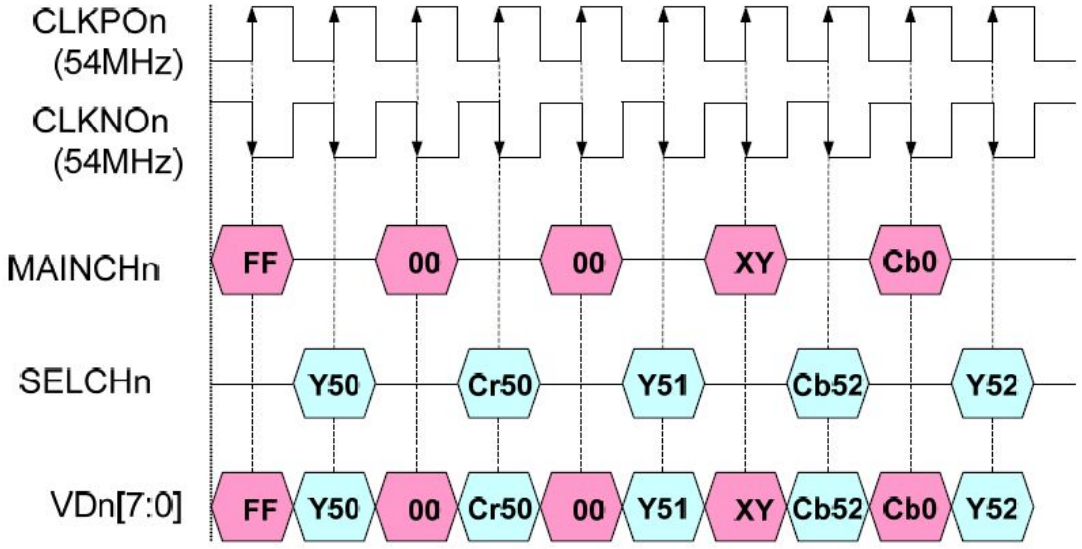


Fig8 Pin output timing of Two Channel Time-multiplexed Format with clock

2.11.3 Four Channel D1 Time-division-multiplexed Format with 108MHz/144MHz

Four channel of 720H/960H at 27MHz/36MHz video stream that are time-division-multiplexed at 108MHz/144MHz data rate format is implemented in EC6696 for security surveillance application. In order to reduce pin counts (thus shrink chip size) on both decoder's digital output port and the input port of the back end compression Codec devices, EC6696 implements single 8 bit bus at 4 times the base band pixel clock rate of 27MHz/36MHz. While quadrupling the data rate on a single bus to meet the new requirement, individually, each channel data arrangement still retains the base band 27MHz/36MHz ITU-R BT.656 specification. For interface that can accept the new 108MHz/144MHz clock bus, only one single clock at 108MHz/144MHz is required. Embedded timing (SAV-EAV) code and Channel ID are inserted into each channel for de-multiplexing and separation of channel data.

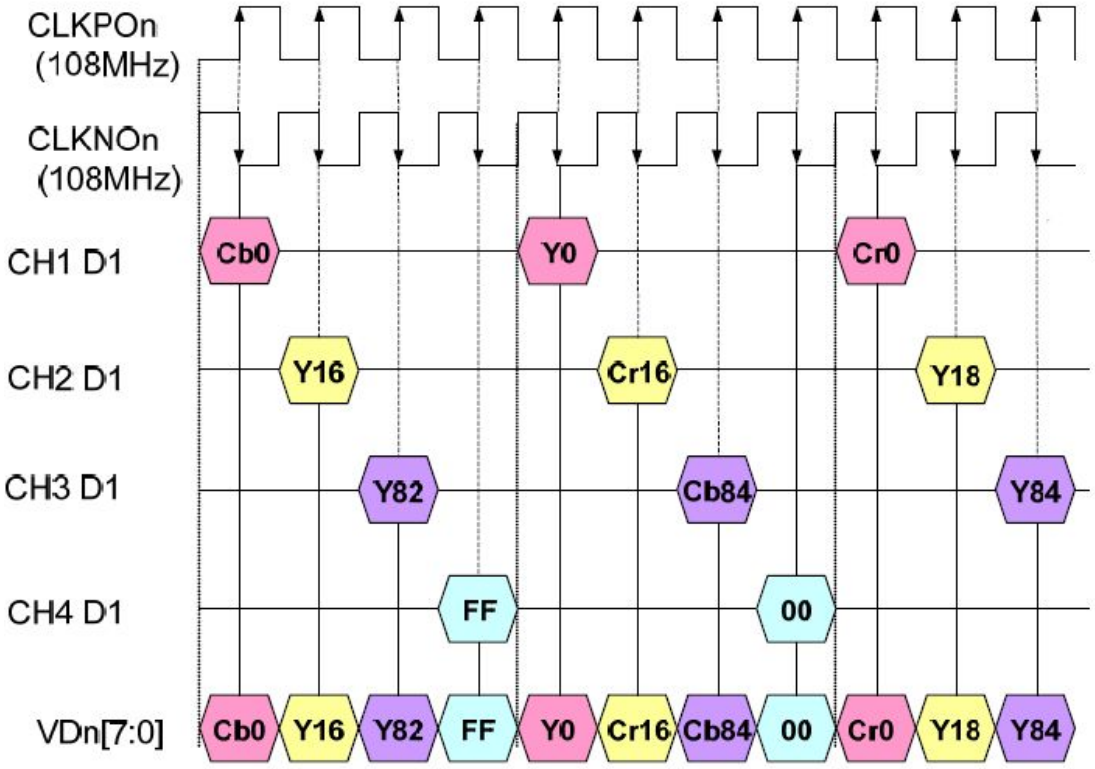


Fig9 Pin output Timing of 108MHz 4 ch D1 Time-Division-Multiplexed Video data with 108MHz clock.

Table3 ITU-R BT.656 Embedded timing code and Channel ID code

Condition			656 FVH Value			SAV/EAV Code Sequence						
Field	V time	H time	F	V	H	First	Second	Third	Fourth			
									Ch0	Ch1	Ch2	Ch3
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF0	0xF1	0xF2	0xF3
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xE0	0xE1	0xE2	0xE3
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xD0	0xD1	0xD2	0xD3
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC0	0xC1	0xC2	0xC3
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB0	0xB1	0xB2	0xB3
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xA0	0xA1	0xA2	0xA3
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x90	0x91	0x92	0x93
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x81	0x82	0x83

2.11.4 Output Enabling Act

After power-up, the EC6696 registers have unknown values. The RSTB pin must be asserted and released to bring all registers to its default values. After reset, the EC6696 data outputs are tri-stated. The OE register should be written after reset to enable outputs desired.

2.11.5 Video Output Channel Selection

If CHMDn[1:0] in Reg0x12 of Format registers is set to 0hex, MAINCH_VDn[1:0] in Reg0x10 of Format registers selects one number of Video Channels to be output on VDn[7:0] pin as Single Channel ITU-R BT.656(D1/WD1) Format output. If CHMDn[1:0] in Reg0x12 of Format registers is set to 1hex, MAINCH_VDn[1:0] in Reg0x10 of Format registers and SELCH_VDn[1:0] in Reg0x11 of Format registers select two numbers of Video Channels to be output on VDn[7:0] pin as Two Channel ITU-R BT.656(D1/WD1) Time-multiplexed Format output. If CHMDn[1:0] in Reg0x12 is set to 2 hex, Four Channel ITU-R BT.656(D1) Time-multiplexed Format is output on VDn[7:0] pin.

2.11.6 Extra Sync Output

The additional timing information such as syncs and field and field flag are also supported through the MPP pins.

2.12 Audio Codec

The audio codec in the EC6696 is composed of four audio Analog-to-Digital converters, one Digital-to-Analog converter, audio mixer, digital serial audio interface and audio detector shown as the Fig10. The EC6696 can accept 4 analog audio signals and 1 digital serial audio data and produce 1 digital serial audio data.

The digital serial audio input data through the ACLKP, ASYNP and ADATP pin are used for playback function. To record audio data, the EC6696 provides the digital serial audio output via the ACLKR, ASYNR and ADATR pin.

The EC6696 can mix all of audio inputs including analog audio signal and digital audio data according to the predefined mixing ratio for each audio via the MIX_RATIO1 ~ MIX_RATIO4 and MIX_RATIOP registers. This mixing audio output can be provided through the analog and digital interfaces. The embedded audio Digital-to-Analog converter supports the analog mixing audio output whose level can be controlled by programmable gain amplifier via the AOGAIN register.

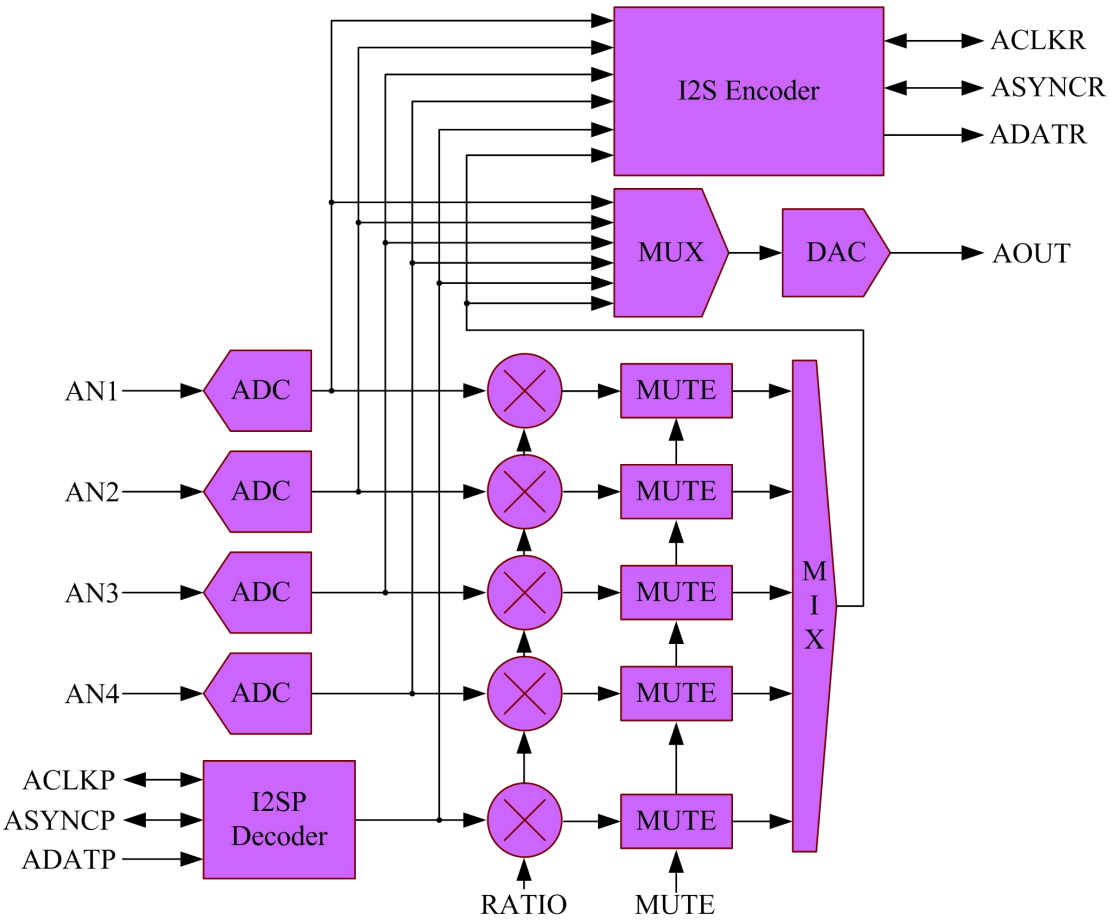


Fig10 Block Diagram of Audio Codec

2.12.1 Audio Clock Master/Slave mode

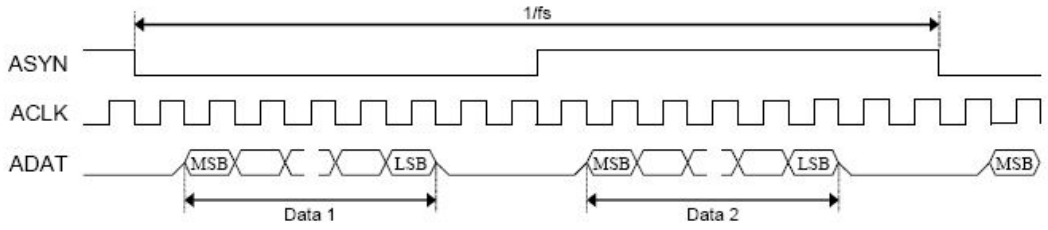
The EC6696 has two types of Audio Clock modes. If ACLKRMASTER register is set to 1, fs audio sample data is processed form audio clock internal ACKG (Audio Clock Generator) generates. In this master mode, ACLKR/ASYNR pins are output mode. ASYNROEN register for ASYNR pin should be set to 0(output enable mode). If ACLKRMASTER register is set to 0, fs audio sample rate is processed from audio clock on ACLKR pin input. 13.5MHz/18MHz audio clock should be connected to ACLKR pin from external master clock source in this slave mode. ASYNR pin can be input or output by external Audio clock master in slave mode. ASYNR signal should change per fs audio sample rate in both master and slave mode. SAMPLE_RATE register set up the frequency of AUDIO sample clock.

2.12.2 Audio Detection

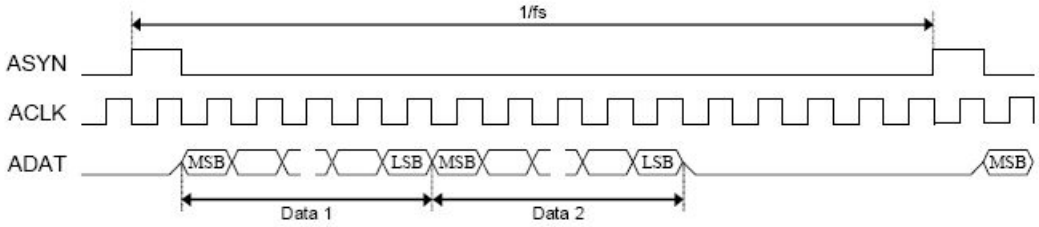
The EC6696 has an audio detector for individual 4 channels. There are 2 kinds of audio detection method defined by the ADET_MTH. One is the detection of absolute amplitude and the other is of differential amplitude. For both detection methods, the accumulation period is defined by the ADET_FILT register and the detecting threshold value is defined by the ADET_TH0 ~ ADET_TH3 registers. The status for audio detection is read by the STATE_AVDET register.

2.12.3 Serial Audio Interface

There are 3 kinds of digital serial audio interfaces in the EC6696, the first is a recording output, the second is a mixing output and the third is a playback input. These 3 digital serial audio interfaces follow a standard I2S or DSP interface as shown in the Fig11



(a) I2S Format



(b) DSP Format

Fig11 Timing Chart of Serial Audio Interface44fgvbtt

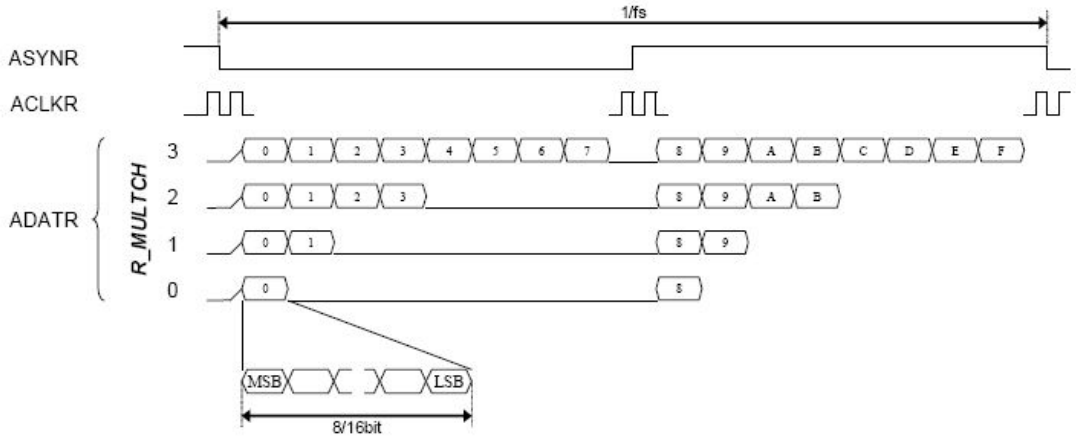
Playback Input

The serial interface using the ACLKP, ASYNP and ADATP pins accepts the digital serial audio data for the playback purpose. The ACLKP and ASYNP pins can be operated as master or slave mode. For master mode, these pins work as output pin and generate the standard audio clock and synchronizing signal. For slave mode, these pins are input mode and accept the standard audio clock and synchronizing signal. The ADATP pin is always input mode regardless of operating mode. One of audio data in left or right channel should be selected for playback audio by the PB_LRSEL.

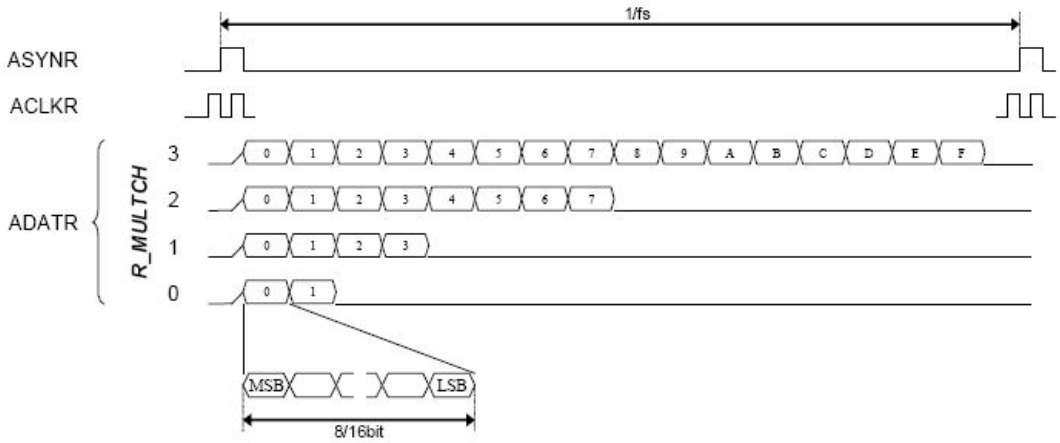
Record Output

To record audio data, the EC6696 provides the digital serial audio data through the ACLKR,

ASYNR and ADATR pins. Sampling frequency comes from 13.5MHz audio system clock setting. Even though the standard I2S and DSP format can have only 2 audio data on left and right channel, the EC6696 can provide an extended I2S and DSP format which can have 16 channel audio data through ADATR pin. The R_MULTCH defines the number of audio data to be recorded by the ADATR pin. ASYNR signal is always fs frequency rate. The frequency of ASYNR is set by the I2S_SAMPLE_RATE register. The Fig12 shows the digital serial audio data organization for multi-channel audio.



(a) I2S Format



(b) DSP Format

Fig12 Timing Chart of Multi-channel Audio Record

2.12.4 Audio Clock Slave Mode Data Output Timing

EC6696 always output ASYNR by ACLKR falling edge triggered timing.
ADATR output data are always changing at next ACLKR falling edge triggered timing after ASYNR signal changes. If ASYNR is output, ADATR output are always fixed to one ACLKR falling edge timing. But if ASYNR is input, ADATR output timing changes by ASYNR input timing.

ASYNR is ACLKR falling edge triggered input/output
If ASYNR is input and ASYNR input is ACLKR falling edge triggered input as ASYNR input signal is changing after ACLKR falling edge, or if ASYNR is output, EC6696 output ADATR by ACLKR falling edge triggered timing as shown on following figures. ASYNR signal is changing during ACLKR = 0. EC6696 output ADATR data after next ACLKR falling edge triggered timing with more than half ACLKR clock delay.

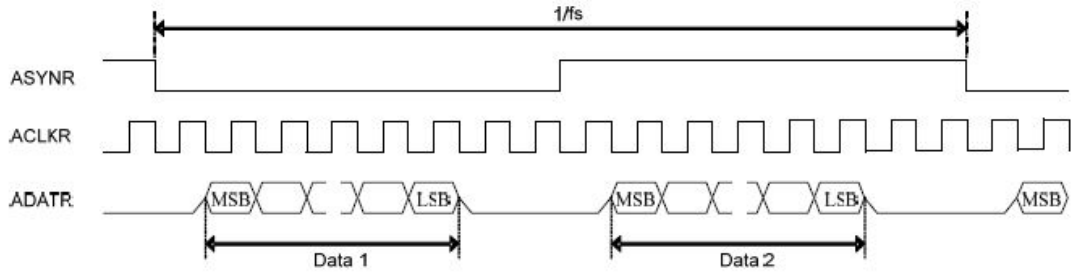


Fig 13-1 ACLKMASTER=0, RM_SYNC =0

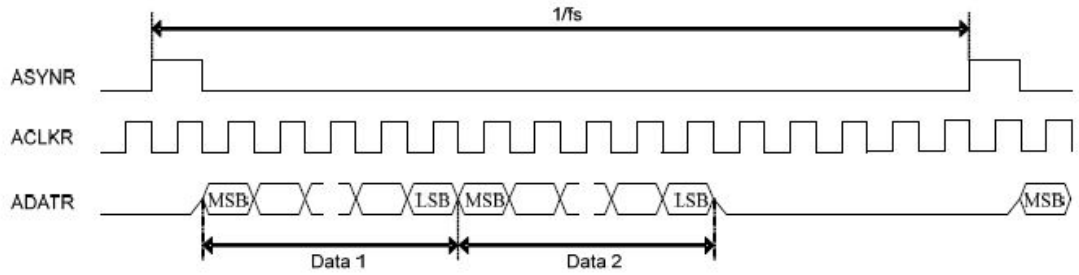


Fig 13-2 ACLKMASTER=0, RM_SYNC =1

ASYNR is ACLKR rising edge triggered input

If ASYNR is input and ASYNR input is ACLKR rising edge triggered input as ASYNR input signal is changing after ACLKR rising edge. EC6696 output ADATR by ACLKR falling edge triggered timing as shown on following figures. ASYNR signal is changing during ACLKR=1. EC6696 output ADATR data after next ACLKR falling edge triggered timing with less than half ACLKR clock delay.

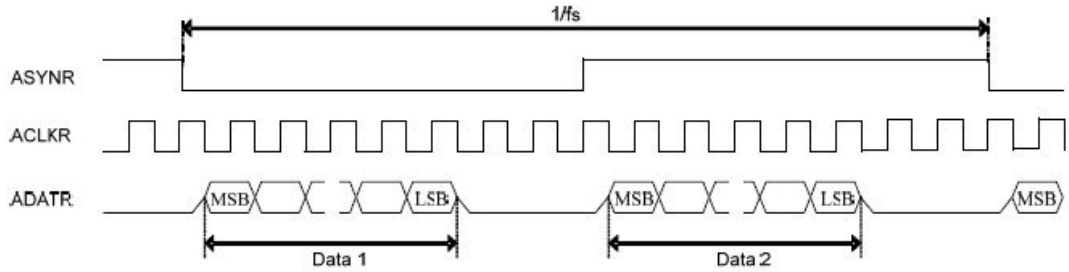


Fig 13-3 I2S_MASTER=0, RM_SYNC =0

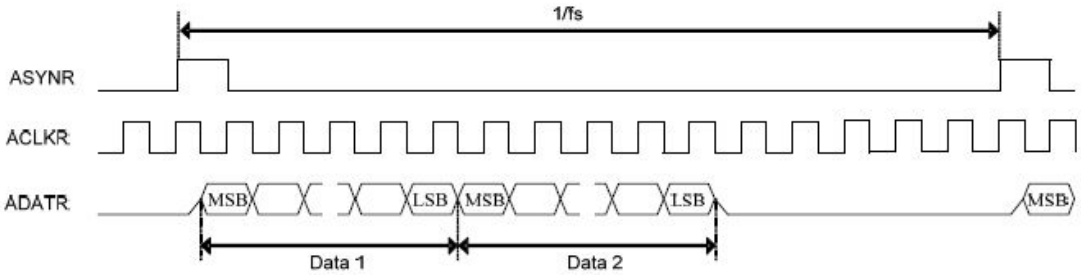


Fig 13-4 I2S_MASTER =0, RM_SYNC =1

2.12.5 ACLKP/ASYNP Slave Mode Data Input Timing

Following 8 data input timings are supported. ADATP_DLY register need to be set up according to the difference of ADATP data input timings. Data1 is only used as default.

ASYNP is ACLKP falling edge triggered input

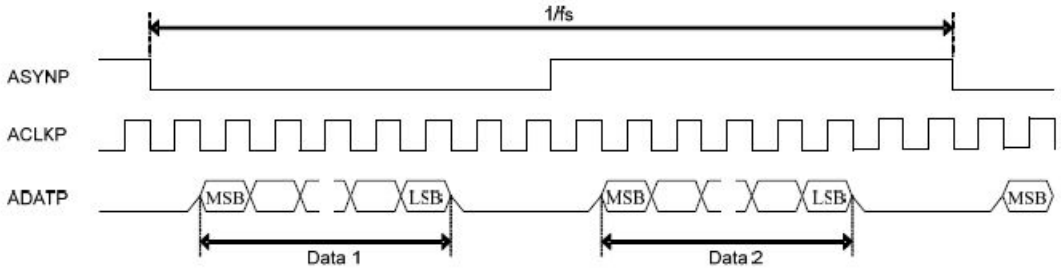


Fig 14-1 PB_SYNC =0, I2SP_MASTER=0, ADATP_DLY=0

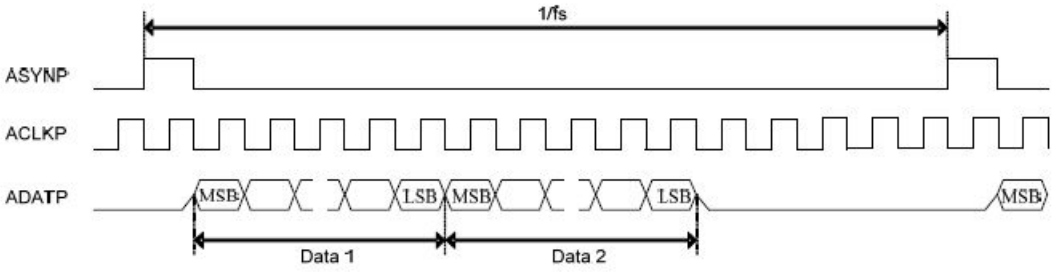


Fig 14-2 PB_SYNC =1, I2SP_MASTER =0, ADATP_DLY=0

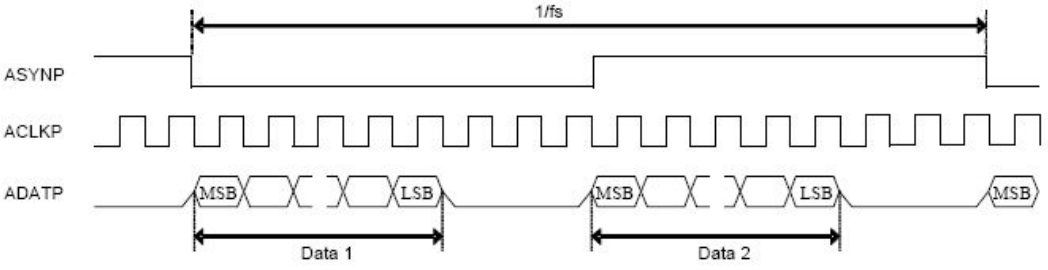


Fig 14-3 PB_SYNC =0, I2SP_MASTER =0, ADATP_DLY=1

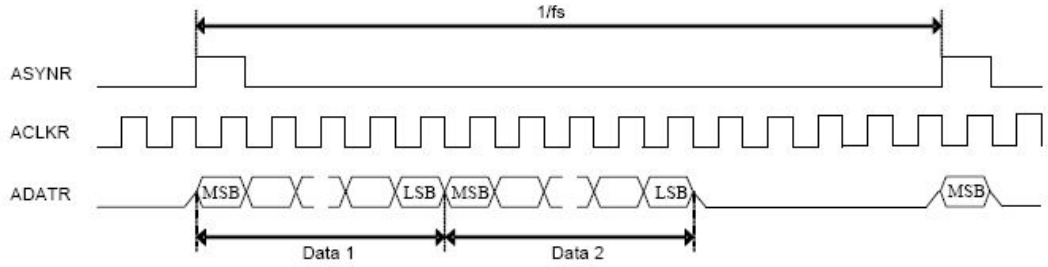


Fig 14-4 PB_SYNC =1, I2SP_MASTER =0, ADATP_DLY=1

ASYNP is ACLKP rising edge triggered input.

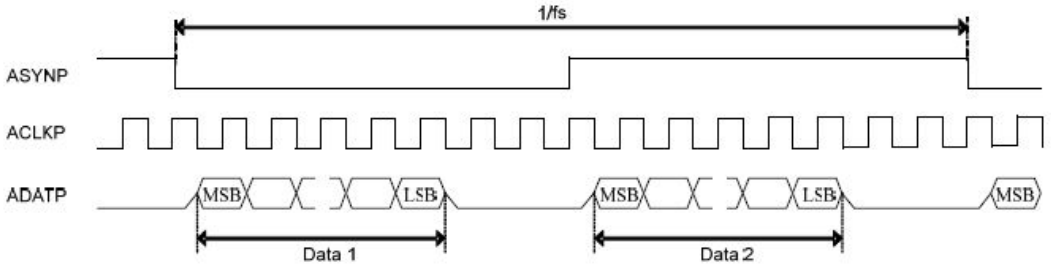


Fig 14-5 PB_SYNC =0, I2SP_MASTER =0, ADATP_DLY=1

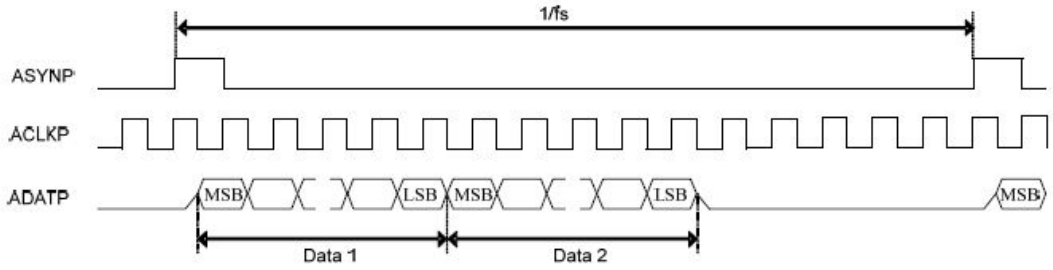


Fig 14-6 PB_SYNC =1, I2SP_MASTER =0, ADATP_DLY=1

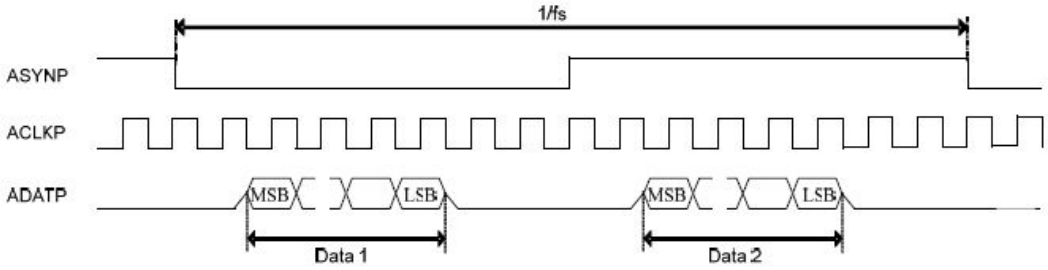


Fig 14-7 PB_SYNC =0, I2SP_MASTER =0, ADATP_DLY=0

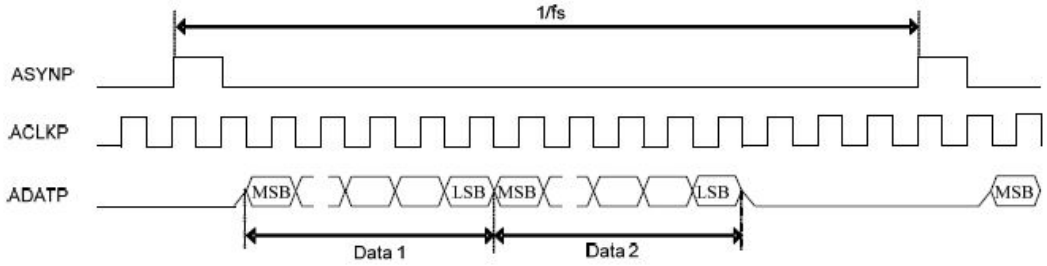


Fig 14-8 PB_SYNC =1, I2SP_MASTER =0, ADATP_DLY=0

2.13 Host Interface

2.13.1 Serial Interface

The two wire serial bus interface is used to allow an external micro-controller to write to or read from the data through the EC6696 register. The SCLK is the serial clock and SDAT is the data line. Both lines are pulled high by the resistors connected to VDD.

The slave address are composed by SADD[1:0] and sub-ADD[2:0], and details are shown on following page.

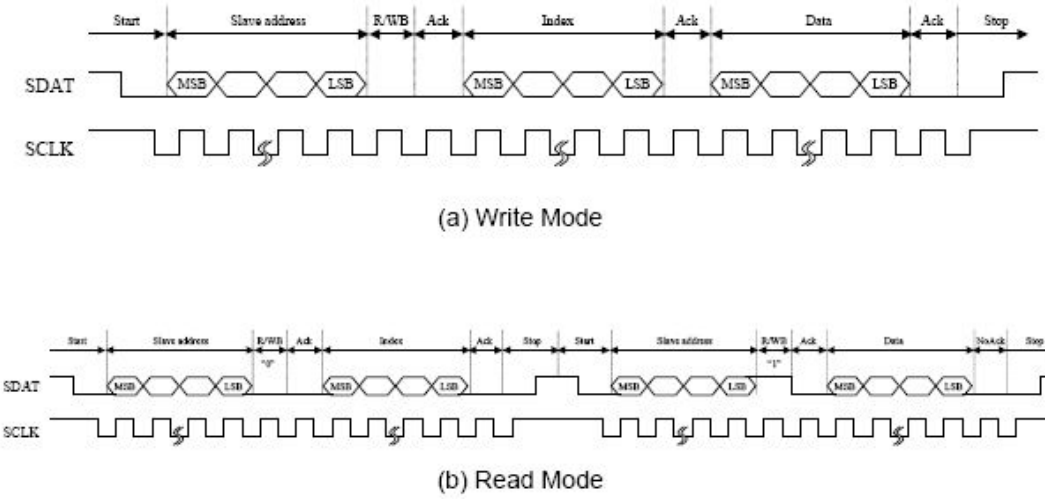


Fig 14 Timing Chart of Serial Interface

2.13.2 Clock PLL

The EC6696 has built-in 2x/4x clock PLL to generate 2xXTI clock and 4xXTI clock. Only 27MHz clock can be connected to XTI pin.

3. Control Register

EC6696 has six independent register spaces: four video channel spaces, one audio channel spaces and one format channel spaces. The register map of different video channel is the same as each other. The SADD[1:0] defines two MSB of the slave device address by tying the SADD pins either to VDD or GND.

Slave Address							R/W
SADD[1]	SADD[0]	1	1	Sub-ADD[2]	Sub-ADD[1]	Sub-ADD[0]	1=Read 0=Write

Sub-ADD[2:0] selects the different register spaces in EC6696

Register Space	Sub-ADD[2:0]
Video channel 1	3'b010
Video channel 2	3'b011
Video channel 3	3'b100
Video channel 4	3'b101
Audio channel	3'b110
Format channel	3'b111

For example, if sadd[1:0] = 2'b11, the slave address of video channel 1 is 0x7A, video channel 2 is 0x7B, video channel 3 is 0x7C, video channel 4 is 0x7D, audio channel is 0x7E, format channel is 0x7F.

The below are registers for one video channel.

3.1 Video Registers Description

0x01 – 960H Mode Control

Bit	Function	R/W	Description	Reset
1	960H_EN	R/W	Enable the 960H work mode. 1'b0 : 720H mode, clock is 27/54/108MHz. 1'b1 : 960H mode, clock is 36/72/144MHz.	1'b0

0x08 – Work Mode Control

Bit	Function	R/W	Description	Reset
2	FPS_TYPE	R/W	This bits controls video decode mode 0: decode CVBS type 525 lines / 60 fields. 1: decode CVBS type 625 lines / 50 fields.	1'h1
1-0	STD	R/W	Video decode standard in non-auto detect mode 2'h0: PAL. 2'h1: NTSC. Others reserved	2'h0

0x0a – Soft Reset Control I

Bit	Function	R/W	Description	Reset
6	RST_ADCS_N	R/W	ADCS module soft reset; If the register's value is 0, pull down the reset signal.	1'h1
5	RST_ATD_N	R/W	Standard Auto Detection module soft reset, If the register's value is 0, pull down the reset signal.	1'h1
4	RST_AGC_N	R/W	Auto Gain Control module soft reset, If the register's value is 0, pull down the reset signal.	1'h1
3	RST_SWTCH_N	R/W	Real Time Work Mode Control module soft reset, If the register's value is 0, pull down the reset signal.	1'h1
2	RST_ITP_N	R/W	Resample module soft reset, If the register's value is 0, pull down the reset signal.	1'h1
1	RST_SYNC_N	R/W	Synchronization module soft reset,	1'h1

			If the register's value is 0, pull down the reset signal.	
0	RST_LPF_N	R/W	Low Pass Filter module soft reset, If the register's value is 0, pull down the reset signal.	1'h1

0x0c – Soft Reset Control II

Bit	Function	R/W	Description	Reset
3	RST_PIS_N	R/W	Polar Inverse Scaler module soft reset, If the register's value is 0, pull down the reset signal.	1'h1
2	RST_AMD_N	R/W	Amplitude Demodulate module soft reset, If the register's value is 0, pull down the reset signal.	1'h1
1	RST_YUV_N	R/W	Y/C Decode module soft reset, If the register's value is 0, pull down the reset signal.	1'h1
0	RST_VDU_N	R/W	Video Display Unit module soft reset, If the register's value is 0, pull down the reset signal.	1'h1

0x0e – Switch Time Count III

Bit	Function	R/W	Description	Reset
7-0	SWTCH_CNT_L	R/W	Channel switch time counter in non-real time mode, low bits	8'hC0

0x13 – PGA Initial Gain

Bit	Function	R/W	Description	Reset
7-0	PGA_INIT_GAIN	R/W	Control the video ADC PGA gain initial value.	8'h9

0x14 – PGA Max Gain

Bit	Function	R/W	Description	Reset
7-0	PGA_MAX_GAIN	R/W	Control the video ADC PGA gain up range.	8'h18

0x15 – PGA Min Gain

Bit	Function	R/W	Description	Reset
7-0	PGA_MIN_GAIN	R/W	Control the video ADC PGA gain down range.	8'h0

0x17 – Max Sync Amplitude

Bit	Function	R/W	Description	Reset
7-0	MAX_SYNC_AMP	R/W	Up threshold of sync amplitude.	8'h16

0x18 – Min Sync Amplitude

Bit	Function	R/W	Description	Reset
7-0	MIN_SYNC_AMP	R/W	Down threshold of sync amplitude.	8'h12

0x19 – Video Sync Mode Control

Bit	Function	R/W	Description	Reset
7-6	CHS_TH	R/W	Channel search threshold 0: threshold = hsync_max_level * (1- 0). 1: threshold = hsync_max_level * (1- 1/2). 2: threshold = hsync_max_level * (1- 1/4). 3: threshold = hsync_max_level * (1- 1/8). The value of hsync_max_level is calculated by input signal.	2'h0
5-4	CHS_LENGTH	R/W	Channel search length 0: level of continuous 64 points lower than threshold. 1: level of continuous 128 points lower than threshold. 2: level of continuous 256 points lower than threshold. 3: level of continuous 512 points lower than threshold.	2'h3
3	VSYNC_PUL_NUM	R/W	This bit set the VSYNC pulse number in video decode: 0: 6 vsync_pulse. 1: 5 vsync_pulse.	1'h1
2	CS_EN	R/W	0: disable signal detect. 1: enable signal detect.	1'h1

1	VTRCK_EN	R/W	0: do not enable vertical tracking. 1: enable vertical tracking.	1'h1
0	HTRCK_EN	R/W	0: do not enable horizontal tracking. 1: enable horizontal tracking.	1'h1

0x1f – Channel Search Result

Bit	Function	R/W	Description	Reset
1-0	CS_RESULT	R	00: normal display mode, so no result. 01: channel search mode, and success. 10: channel search mode, but failed.	2'h0

0x3d – Line Number I

Bit	Function	R/W	Description	Reset
1-0	VLENGTH_H	R/W	Line number of one frame, high bits	2'h2

0x3e – Line Number II

Bit	Function	R/W	Description	Reset
7-0	VLENGTH_L	R/W	Line number of one frame, low bits	8'h71

0x40 – Standard Auto Detect Status

Bit	Function	R/W	Description	Reset
3	DET_STATUS	R	Auto detect status: 0: idle. 1: detection in progress.	X
2-0	STD_NOW	R	Current standard invoked: 0 = PAL(B,D,G,H,I). 1 = NTSC(M). 7 = Not Valid. Others reserved	X

0x41 – Standard Selection Mode

Bit	Function	R/W	Description	Reset
3	NT50_EN	R/W	1 = force decoding format to 50Hz NTSC. 0 = decoding format is set by register ATD_STD[2:0].	1'h0
2-0	ATD_STD	R/W	Standard selected: 0 = select PAL(B,D,G,H,I) mode. 1 = select NTSC(M) mode. 7 = select Auto detection mode. Others reserved	3'h0

0x42 –Standard Enable for Auto Detect

Bit	Function	R/W	Description	Reset
1	NTSCM_EN	R/W	1: enable recognition of NTSC(M). 0: disable recognition.	1'h1
0	PALD_EN	R/W	1: enable recognition of PAL(B, D, G, H, I). 0: disable recognition.	1'h1

0x43 – Auto Detect Start

Bit	Function	R/W	Description	Reset
0	ATD_ATSTART	W	Writing 1 to this bit will manually initiate the auto format detection.	1'h0

0x5a – CBP Type Control

Bit	Function	R/W	Description	Reset
3	CBP_TYPE	R/W	Chroma band pass filter type control: 0: NTSC BPF. 1: PAL BPF.	1'h1
2	FSC_STP_DIR	R/W	In NTSC and PAL, the fsc nco step adjust direction 0: nco_stp = +fsc_stp*imag_sign. 1: nco_stp = -fsc_stp*imag_sign.	1'h0
1	CB_FIX_EN	R/W	Cb_pha_fix enable, high valid.	1'h1

0	PN_ID_FIX	R/W	1: inverse the pn id line by lind. 0: fix the pn id.	1'h0

0x5b – FSC Frequency I

Bit	Function	R/W	Description	Reset
5-0	CB_FREQ_HH	R/W	Sub carrier frequency value, PAL-D default value is 44336/256. NTSC-M default value is 35795/256 As value = fsc * Sampl_Rate*2^BitNum_NCO So PAL = 4.43361875 / 13.5 * 2^30 = 26'd352634214 = 26'h1504c566	6'h15

0x5c – FSC Frequency II

Bit	Function	R/W	Description	Reset
7-0	CB_FREQ_H	R/W	High part of sub carrier frequency.	8'h04

0x5d – FSC Frequency III

Bit	Function	R/W	Description	Reset
7-0	CB_FREQ_M	R/W	Middle part of sub carrier frequency.	8'hc5

0x5e – FSC Frequency IV

Bit	Function	R/W	Description	Reset
7-0	CB_FREQ_L	R/W	Low part of sub carrier frequency.	8'h66

0x67 – Active Video and Color Burst position

Bit	Function	R/W	Description	Reset
7-6	SAV_LINE_H	R/W	High Bits of active video start position in one line	1'h0
5-4	EAV_LINE_H	R/W	High Bits of active video end position in one line	3'h3
3-2	SCB_LINE_H	R/W	High Bits of color burst start position in one line.	2'h0
1-0	ECB_LINE_H	R/W	High Bits of color burst end position in one line.	2'h0

0x68 – Active Video Start Position

Bit	Function	R/W	Description	Reset
7-0	SAV_LINE_L	R/W	Low bits of active video start position in one line PAL-D: 132 (0x84) (default) NTSC: 122 (0x7A)	8'h84

0x69 – Active Video End Position

Bit	Function	R/W	Description	Reset
7-0	EAV_LINE_L	R/W	Low bits of active video end position in one line PAL-D: 851 (0x353) (default) NTSC: 841 (0x349)	8'h53

0x6b – Color Burst Start Position

Bit	Function	R/W	Description	Reset
7-0	SCB_LINE_L	R/W	Low bits of color burst start position in one line. PAL-D: 76 (0x4c) (default)	8'h4C

0x6d – Color Burst End Position

Bit	Function	R/W	Description	Reset
7-0	ECB_LINE_L	R/W	Low bits of color burst end position in one line. PAL-D: 103 (0x67) (default)	8'h67

0x6f – Active Line Control

Bit	Function	R/W	Description	Reset
7-6	SAV_FLD_TOP_H	R/W	In top field, active video start line number, high bits	2'h0
5-4	EAV_FLD_TOP_H	R/W	In top field, active video end line number, high bits	2'h1
3-2	SAV_FLD_BOT_H	R/W	In bottom field, active video start line number, high bits	2'h1
1-0	EAV_FLD_BOT_H	R/W	In bottom field, active video end line number, high bits	2'h2

0x72 – Active Line in Top Field I

Bit	Function	R/W	Description	Reset
7-0	SAV_FLD_TOP_L	R/W	In top field, active video start line number, low bits. In PAL-D, 22(0x16) (default) In NTSC, 19 (0x13)	8'h16

0x73 – Active Line in Top Field II

Bit	Function	R/W	Description	Reset
7-0	EAV_FLD_TOP_L	R/W	In top field, active video end line number, low bits. In PAL-D, 309(0x135) (default) In NTSC, 257 (0x101)	8'h35

0x75 – Active Line in Bottom Field I

Bit	Function	R/W	Description	Reset
7-0	SAV_FLD_BOT_L	R/W	In bottom field, active video start line number, low bits. In PAL-D, 335(0x14f) (default) In NTSC, 257 (0x11b)	8'h4F

0x76 – Active Line in Bottom Field II

Bit	Function	R/W	Description	Reset
7-0	EAV_FLD_BOT_L	R/W	In bottom field, active video end line number, low bits. In PAL-D, 622(0x26e) (default) In NTSC, 521 (0x209)	8'h6E

0x77 – Color Burst Line Control

Bit	Function	R/W	Description	Reset
7-6	SCB_FLD_TOP_H	R/W	In top field, color burst start line number, high bits.	2'h0
5-4	ECB_FLD_TOP_H	R/W	In top field, color burst end line number, high bits.	2'h1
3-2	SCB_FLD_BOT_H	R/W	In bottom field, color burst start line number, high bits	2'h1
1-0	ECB_FLD_BOT_H	R/W	In bottom field, color burst end line number, high bits	2'h2

0x78 – Color Burst Line in Top Field I

Bit	Function	R/W	Description	Reset
7-0	SCB_FLD_TOP_L	R/W	In top field, color burst start line number, low bits. In PAL-D, 6 (default)	8'h7

0x79 – Color Burst Line in Top Field II

Bit	Function	R/W	Description	Reset
7-0	ECB_FLD_TOP_L	R/W	In top field, color burst end line number, low bits. In PAL-D, 307 (0x133) (default), after +1 = 0x134.	8'h34

0x7a – Color Burst Line in Bottom Field I

Bit	Function	R/W	Description	Reset
7-0	SCB_FLD_BOT_L	R/W	In bottom field, color burst start line number, low bits. In PAL-D, 319 (0x13f) (default), after +1 = 0x140.	8'h40

0x7b – Color Burst Line in Bottom Field II

Bit	Function	R/W	Description	Reset
7-0	ECB_FLD_BOT_L	R/W	In bottom field, color burst end line number, low bits. In PAL-D, 621 (0x26d) (default).	8'h6C

0x99 – video motion detect enable byte 23

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE23	R/W	Enable the motion detect.	8'hff

0x9a – video motion detect enable byte 22

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE22	R/W	Enable the motion detect.	8'hff

0x9b – video motion detect enable byte 21

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE21	R/W	Enable the motion detect.	8'hff

0x9c – video motion detect enable byte 20

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE20	R/W	Enable the motion detect.	8'hff

0x9d – video motion detect enable byte 19

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE19	R/W	Enable the motion detect.	8'hff

0x9e – video motion detect enable byte 18

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE18	R/W	Enable the motion detect.	8'hff

0x9f – video motion detect enable byte 17

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE17	R/W	Enable the motion detect.	8'hff

0xa0 – video motion detect enable byte 16

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE16	R/W	Enable the motion detect.	8'hff

0xa1 – video motion detect enable byte 15

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE15	R/W	Enable the motion detect.	8'hff

0xa2 – video motion detect enable byte 14

Bit	Function	R/W	Description	Reset

7-0	VMD_BYTE14	R/W	Enable the motion detect.	8'hff

0xa3 – video motion detect enable byte 13

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE13	R/W	Enable the motion detect.	8'hff

0xa4 – video motion detect enable byte 12

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE12	R/W	Enable the motion detect.	8'hff

0xa5 – video motion detect enable byte 11

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE11	R/W	Enable the motion detect.	8'hff

0xa6 – video motion detect enable byte 10

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE10	R/W	Enable the motion detect.	8'hff

0xa7 – video motion detect enable byte 9

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE9	R/W	Enable the motion detect.	8'hff

0xa8 – video motion detect enable byte 8

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE8	R/W	Enable the motion detect.	8'hff

0xa9 – video motion detect enable byte 7

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE7	R/W	Enable the motion detect.	8'hff

0xaa – video motion detect enable byte 6

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE6	R/W	Enable the motion detect.	8'hff

0xab – video motion detect enable byte 5

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE5	R/W	Enable the motion detect.	8'hff

0xac – video motion detect enable byte 4

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE4	R/W	Enable the motion detect.	8'hff

0xad – video motion detect enable byte 3

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE3	R/W	Enable the motion detect.	8'hff

0xae – video motion detect enable byte 2

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE2	R/W	Enable the motion detect.	8'hff

0xaf – video motion detect enable byte 1

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE23	R/W	Enable the motion detect.	8'hff

0xb0 – video motion detect enable byte 0

Bit	Function	R/W	Description	Reset
7-0	VMD_BYTE0	R/W	Enable the motion detect.	8'hff

0xc9 – video motion detect flag

Bit	Function	R/W	Description	Reset
0	VMD_FLAG	R	1: detected the motion object. 0: do not detect any motion object.	1'h0

0xec – CTI and Frame Rate Control

Bit	Function	R/W	Description	Reset
5	2D_BYPASS	R/W	Bypass 2d proc module.	1'h0
4	CTI_SUB_DIF	R/W	1: original signal minus diff value. 0: original signal add diff value.	1'h0
3	CTI_Y_BYPS	R/W	1: bypass y channel of CTI. 0: do y channel CTI.	1'h1
2	CTI_UV_BYPS	R/W	1: bypass uv channel of CTI. 0: do uv channel CTI..	1'h1
1	FRM_DROP_EN	R/W	1: drop one frame every two frame. 0: do not drop frame.	1'h0
0	FLD_DROP_EN	R/W	1: remove bottom field. 0: do not remove bottom field.	1'h0

0xee – U Scale Coefficient

Bit	Function	R/W	Description	Reset

7-0	U_SCALE_COEF	R/W	U scale coefficient, U_out = U_original * U_MUTE_COEF / 128	8'h40

0xf0 – V Scale Coefficient

Bit	Function	R/W	Description	Reset
7-0	V_SCALE_COEF	R/W	V scale coefficient V_out = V_original * V_MUTE_COEF / 128	8'h40

0xf2 – Y Scale Coefficient

Bit	Function	R/W	Description	Reset
7-0	Y_SCALE_COEF	R/W	Y scale coefficient Y_out = Y_original * Y_MUTE_COEF / 128	8'h40

0xf4 – horizontal crop control

Bit	Function	R/W	Description	Reset
7-6	HOR_CROP_REMAIN_H	R/W	Indicate the number of remain pixels (horizontal) high byte.	2'h2
5-0	HOR_CROP_LEFT	R/W	The number of cropping the left horizontal data.	6'h8

0xf6 – horizontal crop number remain low byte

Bit	Function	R/W	Description	Reset
7-0	HOR_CROP_REMAIN_L	R/W	Indicate the number of remain pixels (horizontal) low byte.	8'hc0

0xf8 – vertical crop control

Bit	Function	R/W	Description	Reset
7-6	VER_CROP_REMAIN_H	R/W	Indicate the number of remain pixels (vertical) high byte.	2'h1

5-0	VER_CROP_UP	R/W	The number of cropping the left vertical data.	6'h0

0xfa – vertical crop number remain low byte

Bit	Function	R/W	Description	Reset
7-0	VER_CROP_REMAIN_L	R/W	Indicate the number of remain pixels (vertical) low byte.	8'h20

0xfe – Display Control

Bit	Function	R/W	Description	Reset
2-1	DISPLAY_MODE	R/W	Control output image format. 0: YCbCr 4:2:2. 1: RGB 5:6:5.	2'h0
0	VIDEO_MODE	R/W	1: NTSC; 0: PAL;	1'h0

0xfe – Display Control

Bit	Function	R/W	Description	Reset
2-1	DISPLAY_MODE	R/W	Control output image format. 0: YCbCr 4:2:2. 1: RGB 5:6:5.	2'h0
0	VIDEO_MODE	R/W	1: NTSC; 0: PAL;	1'h0

3.2 Audio Registers

0x04(CH0)/0x44(CH1)/0x84(CH2)/0xC4(CH3) – Audio Mode Control

Bit	Function	R/W	Description	Reset
4	FPS_TYPE	R/W	Synchronization to video format 1: current video is 50 fields/s 0: current video is 59.94 fields/s	1'b1
3-2	Reserved			
1	AAMPMD	R/W	Audio auto detect working mode: 0: absolute amplitude auto detect mode. 1: differential amplitude auto detect mode	1'b0
0	AUDIO_MODE	R/W	Audio function mode. 0h: 8bit mono sample from internal ADC. 1h: 16bit mono sample from internal ADC.	1'b0

0x05(CH0)/0x45(CH1)/0x85(CH2)/0xC5(CH3) – Audio Mix Control

Bit	Function	R/W	Description	Reset
7	MIX_DERATIO	R/W	Disable the mixing ratio value for all audio. 0:Apply individual mixing ratio value for each audio 1:Apply nominal value for all audio commonly	1'b0
6	MRATIO_MD	R/W	Audio Mixing ratio value divider control 0: MIX_RATIO default value 1: MIX_RATIO / 64	1'b0
5-0	MIX_RATIO	R/W	If MRATIOMD=0(default) : Mix Ratio Value 0 0.25 (default) Recommended for most cases. 1 0.31 2 0.38 3 0.44 4 0.50 5 0.63	6'h0

			6 0.75 7 0.88 8 1.00 9 1.25 10 1.50 11 1.75 12 2.00 13 2.25 14 2.50 15 2.75 If MRATIOMD=1,Mixing ratio is MIX_RATIOn / 64.	

0x07(CH0)/0x47(CH1)/0x87(CH2)/0xC7(CH3)– Audio Mix Mute

Bit	Function	R/W	Description	Reset
0	MIX_MUTE	R/W	Enable the mute function for audio mixing. It effects only for mixing 0: normal. 1: muted.	1'b0

0x08(CH0, CH1, CH2, CH3) – Audio Output Law Mode

Bit	Function	R/W	Description	Reset
1-0	LAWMD	R/W	Select u-Law/A-Law/PCM/SB data output format on ADATR pin. 0: PCM output. 1: SB(Signed MSB bit in PCM data is inverted) output. 2: u-Law output. 3: A-Law output.	2'b1

0x09 – Audio Soft Reset

Bit	Function	R/W	Description	Reset
2	RST_ADC	R/W	ADC Sample module soft reset. 0: Pull down the reset signal in ADC module to reset all registers. 1: No change.	1'b1
1	RST_I2S	R/W	I2S record module soft reset. 0: Pull down the reset signal in I2S module to reset all registers. 1: No change.	1'b1
0	RST_I2SP	R/W	I2S playback module soft reset. 0: Pull down the reset signal in I2SP module to reset all registers. 1: No change.	1'b1

0x0A(CH0,CH1,CH2,CH3) – Clock and 960H Control

Bit	Function	R/W	Description	Reset
1	CLK_SEL	R/W	Select the clock, 27MHz or 36MHz.	1'b1
0	960H_EN	R/W	1: enable the 960H mode, one line is 2304 cycles and clock is 36MHz; 0: normal BT.656 mode, one line is 1728 cycles and clock is 27MHz;	1'b0

0x0B(CH0)/0x4B(CH1)/0x8B(CH2)/0xCB(CH3) – Audio ADC Digital Input Offset Control I

Bit	Function	R/W	Description	Reset
7-0	DC_OFFSET[7:0]	R/W	Set the Audio DC offset register's low 8 bit. Digital ADC input data offset control.Digital ADC input data is adjusted by ADJAADCn = AUDnADC + AADCnOFS. AUDnADC is 2's formatted Analog Audio ADC output. AADCnOFS is adjusted offset value by 2's format.	8'b0

0x0C(CH0)/0x4C(CH1)/0x8C(CH2)/0xCC(CH3) – Audio ADC Digital Input Offset Control II

Bit	Function	R/W	Description	Reset
1-0	DC_OFFSET[9:8]	R/W	Set the Audio DC offset register's high 2 bit.	2'b0

0x0D(CH0)/0x4D(CH1)/0x8D(CH2)/0xCD(CH3) – Audio Detection

Bit	Function	R/W	Description	Reset
7-5	ADET_FLT	R/W	Select the filter for audio detection. 0: wide LPF(default) . . . 7:Narrow LPF.	3'b0
4-0	ADET_TH	R/W	Define the threshold value for audio detection. 0: low value. . . 31: high value.	5'b0

0x0F(CH0, CH1, CH2, CH3) – Audio ADC Sample Rate

Bit	Function	R/W	Description	Reset
2-0	SAMPLE_RATE	R/W	Define audio ADC sample rate. 0: 48k sample rate. 1: 44.1k sample rate. 2: 32k sample rate. 3: 16k sample rate. 4: 8k sample rate.	3'b1

0x10(CH0)/0x50(CH1)/0x90(CH2)/0xD0(CH3) – Adjusted Analog Audio ADC Digital Input Value I

Bit	Function	R/W	Description	Reset
7-0	ADJAADC[7:0]	R	Bit7-0 of adjusted Audio ADC Digital Input Data Value.	X

0x11(CH0)/0x51(CH1)/0x91(CH2)/0xD1(CH3) –Adjusted Analog Audio ADC Digital Input Value II

Bit	Function	R/W	Description	Reset
1-0	ADJAADC[9:8]	R	Bit9-8 of adjusted Audio ADC Digital Input Data Value.	X

0x12(CH0)/0x52(CH1)/0x92(CH2)/0xD2(CH3) – Analog Audio ADC Digital Output Value I

Bit	Function	R/W	Description	Reset
7-0	AUDADC[7:0]	R	Bit7-0 of Analog Audio ADC Digital Output Data Value.	X

0x13(CH0)/0x53(CH1)/0x93(CH2)/0xD3(CH3) –Analog Audio ADC Digital Output Value II

Bit	Function	R/W	Description	Reset
1-0	AUDADC[9:8]	R	Bit9-8 of Analog Audio ADC Digital Output Data Value.	X

0x14(CH0)/0x54(CH1)/0x94(CH2)/0xD4(CH3) – Audio Detect Status

Bit	Function	R/W	Description	Reset
1	DETECT_AUDIO	R	1: Audio detected. 0: No audio detected.	X
0	LOST_AUDIO	R	1: Audio lost.	X

0x15 – Record Sample Rate

Bit	Function	R/W	Description	Reset

2-0	I2S_SAMPLE_RATE	R/W	Set I2S transfer data's sample rate. 0: 48k, 1: 44.1k, 2:32k, 3:16k, 4:8k.	3'b1

0x18 – Record ASYNR Sync Edge

Bit	Function	R/W	Description	Reset
0	FALL_EDGE	R/W	I2S ASYNR sync with ACLKR: 1: ASYNR sync with ACLKR fall edge. 0: ASYNR sync with ACLKR rise edge.	1'b1

0x1A – Record Master Mode

Bit	Function	R/W	Description	Reset
0	I2S_MASTER	R/W	Define the operation mode of the ACLKR and ASYNR pin for record. 0:All type I2S/DSP Slave mode(ACLKR and ASYNR is input) 1:EC6696 type I2S/DSP Master mode (ACLKR and ASYNR is output)	1'b1

0x1D – Record Multi Channel

Bit	Function	R/W	Description	Reset
1-0	R_MULTCH	R/W	Define the how many channels of audio for record on the ADATR pin. 0: 2 channels audio. 1: 4 channels audio. 2: 8 channels audio. 3: 16 channels audio. Number of output data is limited as shown on Sequence of Multi-channel Audio Record table. Also, each output position data are selected by R_SEQ_0/R_SEQ_1/…/R_SEQ_F registers.	2'b0

0x1E – Record Data Format

Bit	Function	R/W	Description	Reset
0	RM_8BIT	R/W	Define output data format per one word unit on ADATR pin. 0: 16bit one word unit output. 1: 8bit one word unit packed output.	1'b1

0x1F – Record Interface Mode

Bit	Function	R/W	Description	Reset
0	RM_SYNC	R/W	Define the digital serial audio data format for record and mixing audio on the ACLKR, ASYNR, ADATR pin. 0: i2s format. 1: dsp format.	1'b0

0x20 – Playback Data Sample Rate

Bit	Function	R/W	Description	Reset
2-0	I2SP_SAMPLE_RATE	R/W	0: 48k, 1: 44.1k, 2:32k, 3:16k, 4:8k.	3'b1

0x22 – Playback ACLKP Sync Edge

Bit	Function	R/W	Description	Reset
0	I2SP_FALL_EDGE	R/W	I2S ASYNP sync with ACLKP: 1: ASYNP sync with ACLKP fall edge. 0: ASYNP sync with ACLKP rise edge.	1'b1

0x23 – Playback Master Mode

Bit	Function	R/W	Description	Reset
0	I2SP_MASTER	R/W	Define the operation mode of the ACLKP and ASYNP pin for record. 0:All type I2S/DSP Slave mode(ACLKP and ASYNP is input) 1:EC6696 type I2S/DSP Master mode (ACLKP and ASYNP is output)	1'b1

0x24 – Playback Delay

Bit	Function	R/W	Description	Reset
0	ADATP_DLY	R/W	ADATP input data delay by one ACLKP clock. 0: No delay. This is for I2S type 1T delay input interface. 1: Add 1 ACLKP clock delay in ADATP input data. This is for left-justified type 0T delay input interface.	1'b0

0x25 – Playback Channel Select

Bit	Function	R/W	Description	Reset
1-0	I2SP_CHSEL	R/W	Left, right or both channel use for playback data. 00: Both left and right channel. 10: Left channel. 01: Right channel. Default: Left channel.	2'b10

0x26 – Playback Data Pack Format

Bit	Function	R/W	Description	Reset
0	PB_8BIT	R/W	Define playback data format per one word unit on ADATP pin. 0: 16bit one word unit output. 1: 8bit one word unit packed output.	1'b1

0x27 – Playback Data Mix Control

Bit	Function	R/W	Description	Reset
7	MIX_DERATIO	R/W	0: Apply individual mixing ratio value for each audio. 1: Apply nominal value for all audio commonly.	1'b0
6	MRATIO_MD	R/W	Audio mixing ratio value divider control. 0: Default value. 1: MIX_RATIO/64.	1'b0
5-0	MIX_RATIO	R/W	Audio input ratio value for audio mixing, ratio/64.	6'b0

0x28 – Playback Interface Mode

Bit	Function	R/W	Description	Reset
0	PB_SYNC	R/W	Define the digital serial audio data format for record and mixing audio on the ACLKP, ASYNP and ADATP pin. 0: i2s format. 1: dsp format.	1'b0

0x29 – Playback Data Mix Mute

Bit	Function	R/W	Description	Reset
0	PB_MIX_MUTE	R/W	Enable the mute function for playback mixing. 0: normal. 1: muted.	1'b0

0x2A – Playback Law Mode

Bit	Function	R/W	Description	Reset
1-0	INLAWMD	R/W	Choose the i2s input playback data's law mode. 0: PCM output. 1: SB(Signed MSB bit in PCM data is inverted) output. 2: u-Law output. 3: A-Law output.	2'b0

0x2B – Audio Interface Output Enable

Bit	Function	R/W	Description	Reset
2	I2S_DAT_OEN	R/W	1'b0: Enable the ADATR, ASYNR and ACLKR output. 1'b1: Disable output.	1'b1
1	reserve	R/W	reserve	1'b1
0	I2SP_DAT_OEN	R/W	1'b0: Enable the ADATP, ASYNP and ACLKP output. 1'b1: Disable output.	1'b1

0x30 – Output Data Sequence

Bit	Function	R/W	Description	Reset
7-4	R_SEQ1[3:0]	R/W	Define the sequence of record audio on the ADATR pin. The register's value represents position1's input source of audio channel. Refer to the Fig12 and Table 4 for the details	4'h2
3-0	R_SEQ0[3:0]	R/W	Define the sequence of record audio on the ADATR pin. The register's value represents position0's input source of audio channel.	4'h0

0x31 – Output Data Sequence

Bit	Function	R/W	Description	Reset
7-4	R_SEQ3[3:0]	R/W	Define the sequence of record audio on the ADATR pin. The register's value represents position3's input source of audio channel.	4'hf
3-0	R_SEQ2[3:0]	R/W	Define the sequence of record audio on the ADATR pin. The register's value represents position2's input source of audio channel.	4'h4

0x32 – Output Data Sequence

Bit	Function	R/W	Description	Reset
7-4	R_SEQ5[3:0]	R/W	Define the sequence of record audio on the ADATR pin. The register's value represents position5's input source of audio channel.	4'h5
3-0	R_SEQ4[3:0]	R/W	Define the sequence of record audio on the ADATR pin. The register's value represents position4's input source of audio channel.	4'h4

0x33 – Output Data Sequence

Bit	Function	R/W	Description	Reset
7-4	R_SEQ7[3:0]	R/W	Define the sequence of record audio on the ADATR pin. The register's value represents position7's input source of audio channel.	4'h7
3-0	R_SEQ6[3:0]	R/W	Define the sequence of record audio on the ADATR pin. The register's value represents position6's input source of audio channel.	4'h6

0x34 – Output Data Sequence

Bit	Function	R/W	Description	Reset
7-4	R_SEQ9[3:0]	R/W	Define the sequence of record audio on the ADATR pin. The register's value represents position9's input source of audio channel.	4'h3
3-0	R_SEQ8[3:0]	R/W	Define the sequence of record audio on the ADATR pin. The register's value represents position8's input source of audio channel.	4'h1

0x35 – Output Data Sequence

Bit	Function	R/W	Description	Reset
7-4	R_SEQb[3:0]	R/W	Define the sequence of record audio on the ADATR pin. The register's value represents positionB's input source of audio channel.	4'h0
3-0	R_SEQa[3:0]	R/W	Define the sequence of record audio on the ADATR pin. The register's value represents positionA's input source of audio channel.	4'he

0x36 – Output Data Sequence

Bit	Function	R/W	Description	Reset
7-4	R_SEQd[3:0]	R/W	Define the sequence of record audio on the ADATR pin. The register's value represents positionD's input source of audio channel.	4'hd
3-0	R_SEQc[3:0]	R/W	Define the sequence of record audio on the ADATR pin. The register's value represents positionC's input source of audio channel.	4'hc

0x37 – Output Data Sequence

Bit	Function	R/W	Description	Reset
7-4	R_SEQf[3:0]	R/W	Define the sequence of record audio on the ADATR pin. The register's value represents positionF's input source of audio channel.	4'hf
3-0	R_SEQe[3:0]	R/W	Define the sequence of record audio on the ADATR pin. The register's value represents positionE's input source of audio channel.	4'he

0x38 – Audio DAC Resource

Bit	Function	R/W	Description	Reset
3-0	R_DAC[3:0]	R/W	Define the audio resource for audio DAC: 4'h0: audio channel 0 4'h1: audio channel 1 4'h2: audio channel 2 4'h3: audio channel 3 4'h4: audio channel 4 4'he: playback data 4'hf: mix data Others reserved	4'he

0x3C – Audio DAC Amplifier Coefficient

Bit	Function	R/W	Description	Reset
5-0	AMP_COEF	R/W	DAC output amplifier coefficient. Data_out = data * amp_coef >> 4;	6'h10

0x3D – Audio DAC Output Bit Select

Bit	Function	R/W	Description	Reset
0	8BIT_EN	R/W	1'h0: DAC output mode is high 8bit. 1'h1: DAC output mode is low 8bit.	1'h1

0x3E – Audio ADC Control

Bit	Function	R/W	Description	Reset
2	ADC_PD	R/W	1: Set the ADC in power down mode. 0: ADC in normal mode.	1'h0
1	ADC_CLK_POL	R/W	Define the ADC clock's polarity. 0: Inverse the clock’s polarity. 1: No change.	1'h1
0	ADC_CLK_EN	R/W	1: Enable the ADC's clock. 0: Not enable.	1'h1

0x3F – Audio DAC Control

Bit	Function	R/W	Description	Reset
2	DAC_SL	R/W	1: Set DAC in sleep mode. 0: Not sleep.	1'h1
1	DAC_CLK_POL	R/W	Define the DAC clock's polarity. 0: Inverse the clock’s polarity. 1: No change.	1'h1
0	DAC_CLK_EN	R/W	1: Enable the DAC's clock; 0: Not enable;	1'h1

3.3 Format Registers

0x09 – Soft Reset

Bit	Function	R/W	Description	Reset
0	RST_SFT	R/W	Format module soft reset 0: pull down all the reset signal in audio, reset the registers; 1: no change;	1

0x0c – 960H Enable

Bit	Function	R/W	Description	Reset
0	960H_EN	R/W	0: 720H mode, clock is 27MHz; 1: 960H mode, clock is 36MHz;	1'b0

0x10 – 1st Channel Select

Bit	Function	R/W	Description	Reset
3-2	MAINCH_VD2	R/W	Select 1st video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD2 pin; 2'b11: the main channel data of VD2 are from ch3 2'b10: the main channel data of VD2 are from ch2 2'b1: the main channel data of VD2 are from ch1 2'b0: the main channel data of VD2 are from ch0	2'b1
1-0	MAINCH_VD1	R/W	Select 1st video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD1 pin; 2'b11: the main channel data of VD1 are from ch3 2'b10: the main channel data of VD1 are from ch2 2'b1: the main channel data of VD1 are from ch1 2'b0: the main channel data of VD1 are from ch0	2'b0

0x11 – 2nd Channel Control

Bit	Function	R/W	Description	Reset
3-2	SELCH_VD2	R/W	Select 2nd video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD2 pin: 2'b11: the select channel data of VD2 are from ch3. 2'b10: the select channel data of VD2 are from ch2. 2'b1: the select channel data of VD2 are from ch1. 2'b0: the select channel data of VD2 are from ch0. When MAINCH_VD2[1:0] = SELCH_VD2[1:0], the select channel data are from default ch0 (MAINCH_VD4 != 0) or ch1 (MAINCH_VD2 = 0).	2'b10
1-0	SELCH_VD1	R/W	Select 2nd video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD1 pin: 2'b11: the select channel data of VD1 are from ch3. 2'b10: the select channel data of VD1 are from ch2. 2'b1: the select channel data of VD1 are from ch1. 2'b0: the select channel data of VD1 are from ch0. When MAINCH_VD1[1:0] = SELCH_VD11:0], the select channel data are from default ch0 (MAINCH_VD1 != 0) or ch1 (MAINCH_VD1 = 0).	2'b01

0x12 – Channel Mode

Bit	Function	R/W	Description	Reset
3-2	CHMD2	R/W	Select video bus output mode on 8bit VD2[7:0] pin. 0: Single Channel ITU-R BT.656 format output. 1: Two Channel ITU-R BT.656 Time-multiplexed format output. 2: Four Channel ITU-R BT.656 Time-multiplexed format output.	2'd2
1-0	CHMD1	R/W	Select video bus output mode on 8bit VD1[7:0] pin. 0: Single Channel ITU-R BT.656 format output. 1: Two Channel ITU-R BT.656 Time-multiplexed format output. 2: Four Channel ITU-R BT.656 Time-multiplexed format output.	2'd2

0x19 – Channel Output Mux

Bit	Function	R/W	Description	Reset
3-0	1CH_SEL	R/W	In Single Channel ITU-R BT.656 format output mode, this register select the data source on VDn(n=1,2,3,4). 1ch_sel[1:0], VD1 output data select. 2'b00: the select channel data of VD1 are from ch0 2'b01: the select channel data of VD1 are from ch1 2'b10: the select channel data of VD1 are from ch2 2'b11: the select channel data of VD1 are from ch3 1ch_sel[3:2], VD2 output data select. 2'b00: the select channel data of VD2 are from ch0 2'b01: the select channel data of VD2 are from ch1 2'b10: the select channel data of VD2 are from ch2 2'b11: the select channel data of VD2 are from ch3	8'hE4

0x1a – BT656 Control

Bit	Function	R/W	Description	Reset
6	PAL_NTSC_MD	R/W	BT 656 Format: 1'b0: PAL mode. 1'b1: NTSC mode.	1'b0
5-4	CHID_MD	R/W	Set the channel ID. 2'd0: no channel ID. 2'd1: blank code with ID. 2'd2: sync code with ID. 2'd3: sync and blank code with ID.	1'd2
3	GEN_SIG_IN4	R/W	1: set the ch3 use data generated inside; 0: use data from stimulus module;	
2	GEN_SIG_IN3	R/W	1: set the ch3 use data generated inside; 0: use data from stimulus module;	
1	GEN_SIG_IN2	R/W	1: set the ch3 use data generated inside; 0: use data from stimulus module;	
0	GEN_SIG_IN1	R/W	1: set the ch3 use data generated inside; 0: use data from stimulus module;	

0x1d – VD Output Enable

Bit	Function	R/W	Description	Reset
5	CLKVD2_POL	R/W	1'b0: Not inverse. 1'b1: Polarity of vd2 clock inverse.	1'b1
4	CLKVD1_POL	R/W	1'b0: Not inverse. 1'b1: Polarity of vd1 clock inverse.	1'b1
3	VD2_OEN	R/W	1'b0: vd2 output is enable. 1'b1: vd2 output is tri-state.	1'b1
2	VD1_OEN	R/W	1'b0: vd1 output is enable. 1'b1: vd1 output is tri-state.	1'b1
1	CLKVD2_OEN	R/W	1'b0: vd2 clock output is enable. 1'b1: output is tri-state.	1'b1
0	CLKVD1_OEN	R/W	1'b0: vd1 clock output is enable. 1'b1: output is tri-state.	1'b1

4. Electrical Information

4.1 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	units
VDDV(measured to VSSV)	VDDV	3.0	3.3	3.6	V
VDDA(measured to VSSA)	VDDA	3.0	3.3	3.6	V
VDDI(measured to VSS)	VDDI	1.08	1.2	1.32	V
VDDO(measured to VSS)	VDDO	3.0	3.3	3.6	V
Analog Input Vpp(AC coupling required)	V_{AIN}	0	1.0	2.0	V
Ambient Operating Temperature	T_A	-20		70	°C

- Note: Power On/Off sequence should be keep the following rule.
  - Apply Power to VDDV, VDDA,VDDI and VDDO at the same time
  - If it is difficult to apply the power to these pins at the same time, apply to the power to VDDO first and to VDDV, VDDA, and VDDI later.
  - Cut the power of VDDV, VDDA, VDDI and VDDO at the same time
  - If it is difficult to cut the power of these pins at the same time, cut the power off to VDDV, VDDA,VDDI first and VDDO later

4.2 DC Electrical Parameters

Parameter	Symbol	Min	Typ	Max	units
Digital Inputs					
Input High Voltage	V_{IH}	2.0		3.6	V
Input Low Voltage	V_{IL}	-0.3		0.8	V
Input Leakage Current (@V_I=3.3V or 0V)	I_L			10	uA
Input Capacitance	C_{IN}		6		pF
Digital Outputs					
Output High Voltage	V_{OH}	2.4			V
Output Low Voltage	V_{OL}			0.4	V
High Level Output Current(@V_{OH}=2.4V)	I_{OH}	9.3	18.2	29.5	mA
Low Level Output Current (@V_{OL}=0.4V)	I_{OL}	7.4	11.8	16.5	mA
Tri-state Output Leakage Current (@Vo=3.3V or 0V)	I_{OZ}			±10	uA
Output Capacitance	C_O		6		pF
Analog Pin Input Capacitance	C_A		6		pF
Supply Current (4 video 960h, 4 audio, 144MHz 656 output)					
Analog Video ADC Supply Current (VDDV, 3.3V)	I_{DDV}		90		mA
Analog Audio Supply Current (VDDA, 3.3V)	I_{DDA}		5		mA
Digital Internal Supply Current (VDDI, 1.2V)	I_{DDI}		85		mA
Digital I/O Supply Current (VDDO, 3.3V)	I_{DDO}		35		mA
Total Power Dissipation	P		531		mW

4.3 Video Decoder Parameters 1

Parameter	Symbol	Min	Typ	Max	units
ADCs					
ADC resolution	ADCR	-	10	-	Bits
ADC integral Non-linearity	AINL	-	±1	-	LSB
ADC differential non-linearity	ADNL	-	±1	-	LSB
ADC clock rate	f_{ADC}	-	27	-	MHz
Horizontal PLL					
Line frequency(50Hz)	f_{LN}	-	15.625	-	KHz
Line frequency(60Hz)	f_{LN}	-	15.734	-	KHz
Static deviation	$\triangle f_H$	-	-	6.2	%
Subcarrier PLL					
subcarrier frequency(NTSC-M)	f_{SC}	-	3579545	-	Hz
subcarrier frequency(PAL-BDGHI)	f_{SC}	-	4433619	-	Hz
subcarrier frequency(PAL-M)	f_{SC}	-	3575612	-	Hz
subcarrier frequency(PAL-N)	f_{SC}	-	3582056	-	Hz
Lock in range	$\triangle f_H$	±450	-	-	Hz
Oscillator Input					
nominal frequency		-	27	-	MHz
deviation		-	-	±50	ppm
duty cycle		-	-	55	%

4.4 Video Decoder Parameters 2

Parameter	Symbol	Min	Typ	Max	units
Lock Specification					
Sync Amplitude Range		1	-	200	%
Color Burst Range		5	-	200	%
Horizontal Lock Range		-5	-	5	%
Vertical Lock Range		45	-	65	Hz
F_{SC} Lock Range		-	±450	-	Hz
Color Burst Position Range		-	±2.2	-	us
Color Burst Width Range		-		-	cycle
Video Bandwidth					
Bandwidth		-	6	-	MHz
Noise Specification					
SNR(Luma flat field)		-	57	-	dB
Nonlinear Specification					
Y Nonlinearity		-	0.5	0.7	%
Differential Phase		-	0.4	0.6	Degree
Differential Gain		-	0.6	0.8	%
Chroma Specification					
Hue Accuracy		-	1	-	Degree
Chroma ACC Range		-	-	400	%
Chroma Amplitude Error		-	1	-	%
Chroma Phase Error		-	0.3	-	%
Chroma Luma Intermodulation		-	0.2	-	%
K-Factor					
K_{2T}		-	0.5	-	%
$K_{pulse/bar}$		-	0.5	-	%

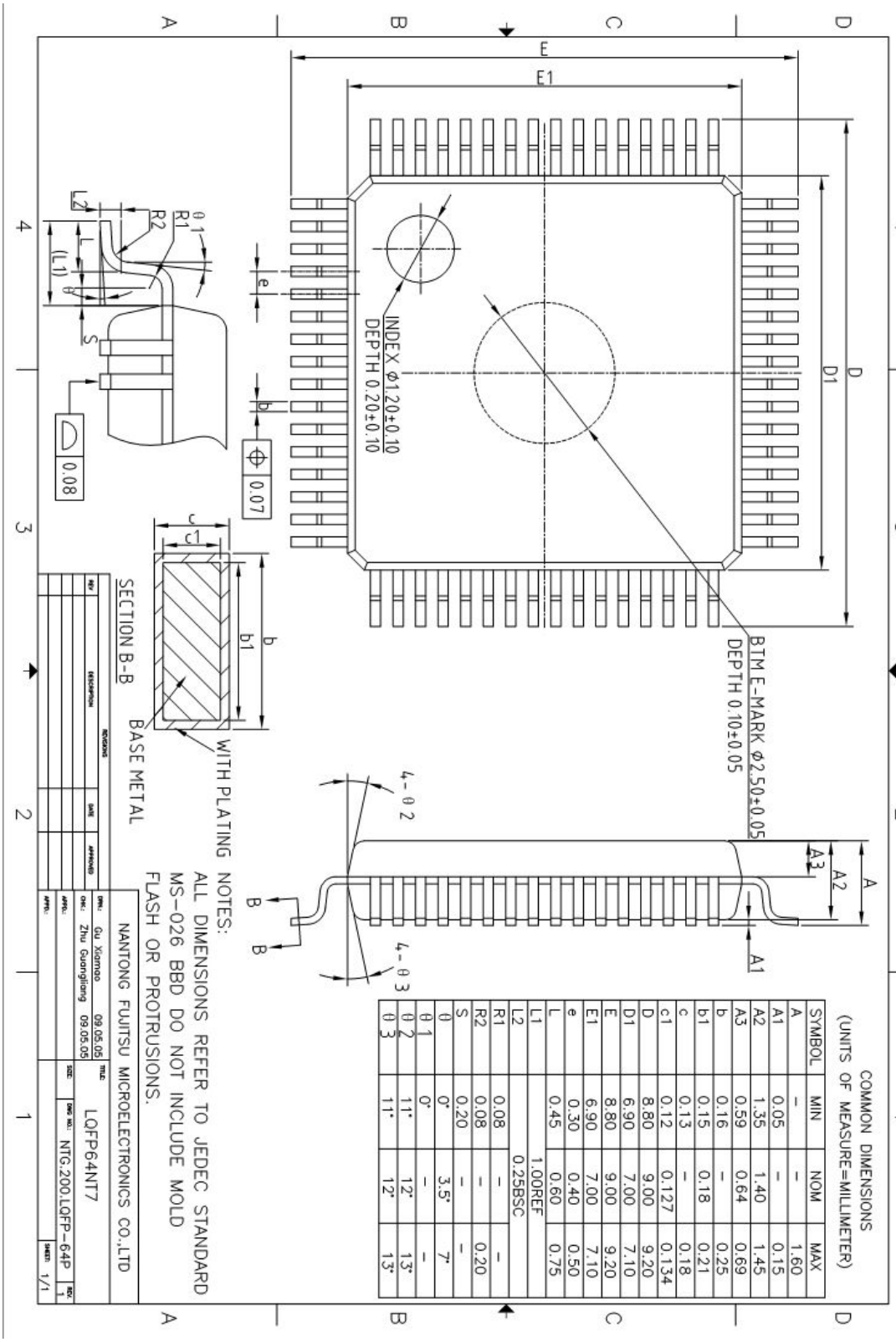
4.4 Analog Audio Parameters

Parameter	Symbol	Min	Typ	Max	units
Analog Audio Input Characteristics					
AIN-4 Input Impedance	RINX	10	-	-	Kohm
Inter-channel gain mismatch		-	0.2	-	dB
Input voltage range		-	-	2	Vpp
Full scale input voltage[1]	V_{iFULL}	-	3.3	-	Vpp
Inter-channel isolation[2]		-	90	-	dB
Analog Audio Output Characteristics					
AOUT Output Load Resistance	RLAO	2K	10K	-	Ohm
AOUT Load Capacitance	CLAO	-	20	1000	pF
AOUT Offset Voltage	VOSAO	-	-	100	mV
Full scale output voltage[3]	V_{oFULL}	-	1.2	-	Vpp

1. Tested at input gain of 0dB, Fin = 1KHZ.
2. Tested at input gain of 0dB, Fs=8KHz and 16KHz.
3. Tested at output gain of 0dB, Fout=1KHz.

4.5 Application Schematics

4.6 Package Dimension



SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.16	–	0.25
b1	0.15	0.18	0.21
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.30	0.40	0.50
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ 1	0°	–	–
θ 2	11°	12°	13°
θ 3	11°	12°	13°