ECN3297 is 16-channel High Voltage analog switching IC with bleed resistors on which latch-up free is realized by dielectric isolation technology.

High voltage and low ON-resistance MOS switches are used as output devices controlled by a 3.3V or 5V signal. The ECN3297 is most suited to Ultrasound Imaging applications.

### **Functions**

- \* High voltage and low on-resistance MOS switches integrated.
- \* 16bit shift resister integrated.
- \* Integrated bleed resistors on the outputs.
- \* Integrated clamping diodes for overvoltage protection positive overshoot.

#### **Features**

- \* Switch on-resistance: 19  $\Omega$  typ. (VPP=100V,VNN=-100V,ISIG=5mA, 25°C)
- \* Switch breakdown voltage: 220V
- \* Latch-up free CMOS and High-Voltage drive circuit.
- \* Power up/down sequence of power supply is free.
- \* 48-pin TQFP Package (RoHS compliant)

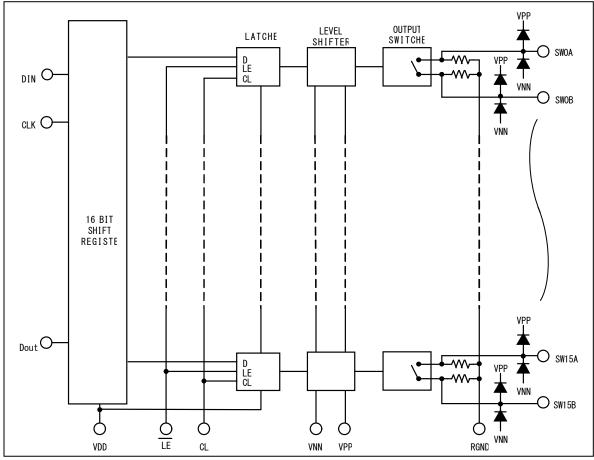


Fig.1 Block diagram

### 1. General

This Specification shall be applied to the following semiconductor integrated circuit.

1) Parts name: ECN3297TF

2) Application : Ultrasound imaging scanner and others

3) Structure : Monolithic IC4) Package : TQFP48

## 2. Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Terminal	Values	Unit	Note
1	Logic power supply voltage	VDD	VDD	-0.5 to +7.0	V	Ta=25°C
2	VPP-VNN supply voltage	-	VPP, VNN	220	V	Ta=25°C
3	VPP Positive high voltage supply	VPP	VPP	-0.5 to VNN+200	V	Ta=25°C
4	VNN negative high voltage supply	VNN	VNN	-200 to +0.5	V	Ta=25°C
5	Logic input voltages	VDD	DIN, CLK, CL, LE	-0.5 to VDD+0.3	٧	Ta=25°C
6	Analog signal range	-	SW0 to SW15	VNN to VPP	V	Ta=25°C
7	Operating junction temperature	Tjop	-	-20 to +125	°C	
8	Storage temperature	Tstg	-	-55 to +150	°C	
9	Power dissipation	Pw	-	1.0	W	TQFP48 Ta=70°C

## 3. Electrical Characteristics

## 3.1 DC Characteristics

Table 2 DC Characteristics	Ta=25°C	VDD=5V
----------------------------	---------	--------

		ible 2 D		ciensiics		1	1a-25 C VDD-5V		
No.	Items	Symbol		Spec	1	Unit	Test conditions		
. 10.	пошо	Cyllibol	Min	Тур	Max	Jill	100t conditions		
			-	24	38		ISIG=5mA VPP=40V,		
			_	17	27		ISIG=200mA VNN=-160V		
1	Small signal switch on	RONS	_	19	27	Ω	ISIG=5mA VPP=100V,		
•	resistance	110110	_	15	24	22	ISIG=200mA VNN=-100V		
			_	19	25		ISIG=5mA VPP=160V,		
			_	15	25		I SIG=200mA VNN=-40V		
2	Small signal switch on resistance matching	ΔRONS	_	5	20	%	VPP=100V, VNN=-100V ISW=5mA		
3	Large signal switch on resistance	RONL	_	16	_	Ω	VPP=100V   I SIG=1A VNN=-100V		
4	Value of output bleed resistance	RINT	20	35	50	kΩ	Output switch to RGND IRINT=0.5mA		
5	Switch off leakage per switch	ISOL	-	1.0	10	μА	VSIG=VPP-10V, or VNN+10V		
6	DC offset switch (off)	DCOFF	_	10	100	mV	No load		
7	DC offset switch (on)	DCON	_	10	100	mV	No load		
8	Positive HV supply current	IPPQ1	_	10	50	μΑ	All SWs off		
9	Negative HV supply current	INNQ1	_	-10	-50	μА	All SWs off		
10	Positive HV supply current	IPPQ2	-	10	50	μΑ	All SWs on, ISW=5mA		
11	Negative HV supply current	INNQ2	_	-10	-50	μА	All SWs on, ISW=5mA		
			-	_	7.0		VPP=40V VNN=-160V 50kHz output		
12	IPP Supply current	IPP	_	_	7.0	mA	VNN=-100V switching frequency		
			_	-	7.0		VNN=-40V without load		
			_	_	7.0		VPP=40V VNN=-160V 50kHz output		
13	INN Supply current	INN	_	_	7.0	mA	VNN=-100V switching frequency		
			_	_	7.0		VPP=160V VNN=-40V without load		
14	Logic supply average current	IDD	_	-	4.0	mA	fCLK=5MHz,VDD=5.0V		
15	Logic supply quiescent current	IDDQ	_	-	10	μΑ			
16	Data out source current	ISOR	0.45	0.70	_	mA	VOUT=VDD-0.7V		
17	Data out sink current	ISINK	0.45	0.70	_	mA	VOUT=0.7V		

## 3.2 AC Characteristics

Table 3 AC Characteristics

Ta=25°C VDD=5V

No.	Items	Symbol		Spec		Unit	Test conditions
INO.	items	Symbol	Min	Тур	Max	Offic	rest conditions
1	SW Turn on time	tON	_	_	5.0	μS	VSIG=VPP-10V, RL=10kΩ
2	SW Turn off time	tOFF	-	_	5.0	μS	VSIG=VPP-10V, RL=10kΩ
3	Clock fraguency	fCLK	_	_	30	MHz	50% duty cycle, fData=fCLK/2 VDD=5.0V
3	Clock frequency	ICLK	_	_	20	MHz	50% duty cycle, fData=fCLK/2 VDD=3.3V
4	Clock delay time to data out	tDO	16	_	55	ns	DOUT terminal,VDD=3.3V
			12	_	42	ns	DOUT terminal,VDD=5.0V
		+VSPK	_	_	150		VPP=40V, VNN=-160V,
		-VSPK	-	_	-150		RL= $50\Omega$
5	Output voltage spike	+VSPK	-	_	150	mV	VPP=100V, VNN=-100V,
	Output voltage spike	-VSPK	-	_	-150	IIIV	RL=50Ω
		+VSPK	-	ı	150		VPP=160V, VNN=-40V,
		-VSPK	_	_	-150		RL=50Ω

Table 4 AC Characteristics (for reference purpose only)

Ta=25°C VDD=5V

No.	Items	Symbol	Symbol Spec				Condition		
INO.	items	Symbol	Min	Тур	Max	Unit	Condition		
1	Off capacitance SW to GND	CSG (off)	-	6	-	pF	0V, 1MHz		
2	On Capacitance SW to GND	CSG (on)	1	15	-	pF	0V, 1MHz		
3	SW off isolation	KO	-30	-33		dB	f=5MHz, $1k\Omega$ //15pF load		
	SVV OII ISOIALIOII	RO	-54	-60	ı	dB	f=5MHz, $50\Omega$ load		
4	SW Crosstalk	KCR	-54	-60	_	dB	f=5MHz, $50\Omega$ load		

Note: These items are not tested when shipped.

## 4. Recommended Operating Conditions

Please operate in use within the limit of recommended operating conditions detailed in Table 5.

Table 5 Recommended Operating Conditions

No	Items	Symbol	Recommended Value
1	Logic power supply voltage	VDD	3.0V to 5.5V
2	Positive high voltage supply	VPP	40V to 160V
3	Negative high voltage supply	VNN	-160V to 0V
4	VPP-VNN supply voltage	ı	40V to 200V
5	High-level input voltage	VIH	0.9VDD to VDD
6	Low-level input voltage	VIL	0V to 0.1VDD
7	Analog signal voltage peak to peak	VSIG	VNN to VPP
8	Operating free air-temperature	Та	0°C to 70°C
9	Switching frequency	Fsw	50kHz max, Duty Cycle=50%
10	Set up time for LE	TSD	Min.60ns
11	Pulse width of LE	TWLE	Min.40ns
12	Time width of CL	TWCL	Min.40ns
13	Set up time DATA to Clock	TSU	Min.10ns
14	Hold time DATA from Clock	Th	Min.10ns
15	Maximum VSIG Slew Rate	dV/dt	Max.30V/ns

#### Attention;

- 1) Power up/down sequence of power supply is arbitrary except GND terminal of IC must be powered-up first and powered-down last.
- 2) It is indispensable to make there are not to exceed a maximum rated voltage by the occurrence of the excessive voltage in case of investing and cutting of the power supply.

## 5. Test Circuit

VPP

 $\vee NN$ 

 $\vee$ NN

Ko=20 log (VOUT/VIN)

d) Off Isolation

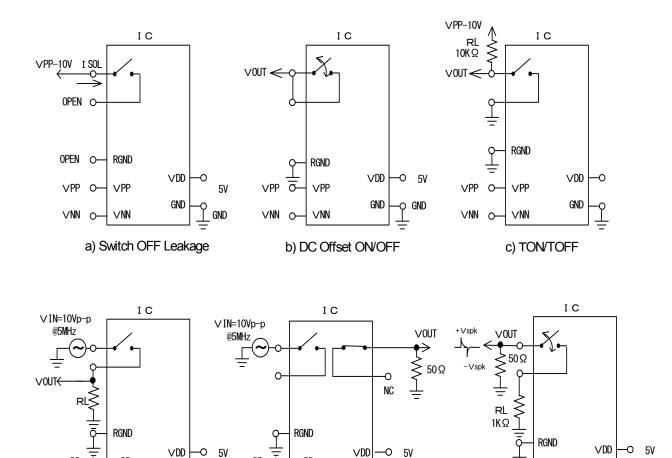


Fig. 2 Test Circuit

Kcr=20log(VOUT/VIN)

e) Crosstalk

 $\vee NN$ 

GND

→ GND

VPP

 $\vee NN$ 

GND

GND

VPP Ō

 $\vee NN$ 

VPP

 $\vee$ NN

f) Output Voltage Spike

GND

GND

## 6. Timing Waveforms

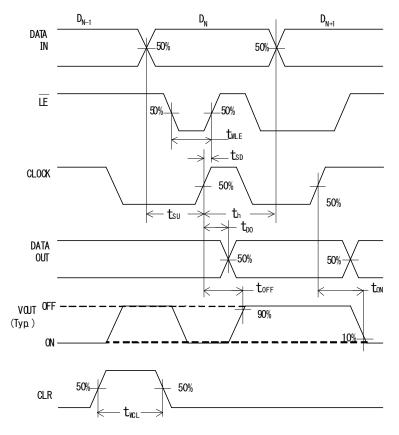


Fig. 3 Timing Waveforms

## <u>Note</u>

- 1. Serial data is clocked in on the rising edge of CLK.
- 2. The switches go to a state retaining their present condition on the rising edge of LE.

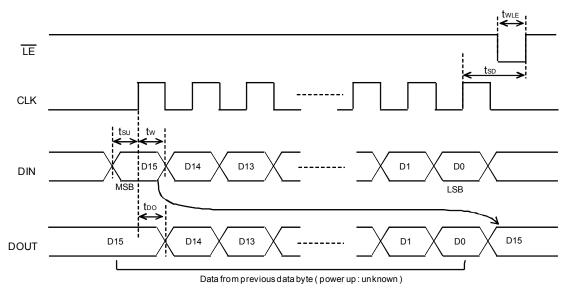


Fig. 4 LATCH ENABLE Timing waveform

## 7. Truth Table

Table 6 Truth table

D0	D1	D2	D3	D4	D5	D6	D7	LE	CL	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
Н								L	L	ON							
	L							L	L		OFF						
	Н							L	L		ON						
		L						L	L			OFF					
		Н						L	L			ON					
			L					L	L				OFF				
			Н					L	L				ON				
				L				L	L					OFF			
				Н				L	L					ON			
					L			L	L						OFF		
					Н			L	L						ON		
						L		L	L							OFF	
						Н		L	L							ON	
							L	L	L								OFF
							Н	L	L								ON
Χ	Χ	Χ	Χ	Χ	Χ	Χ	Χ	Н	L					IOUS S			
Х	Х	Х	Х	Х	Х	Χ	Х	Χ	Н	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
			,,					, ,		0	011	0	<b>U</b>	0.1	<u> </u>	•	
D8	D9	D10	D11	D12	D13	D14	D15	LE	CL	SW8						SW14	
D8	D9							LE L	CL	SW8	SW9						
D8 L	D9 L							LE L	CL L	SW8	SW9						
D8 L	D9							LE L	CL L	SW8	SW9	SW10					
D8 L	D9 L	D10						LE L L	CL L L	SW8	SW9	SW10					
D8 L	D9 L	D10						LE L L	CL L L L	SW8	SW9	SW10					
D8 L	D9 L	D10	D11					LE L L L L	CL L L L L L	SW8	SW9	SW10	SW11				
D8 L	D9 L	D10	D11					LE L L L L L L L L L L L L L L L L L L	CL L L L L L	SW8	SW9	SW10	SW11	SW12			
D8 L	D9 L	D10	D11	D12				LE L L L L L	CL L L L L L L L	SW8	SW9	SW10	SW11	SW12			
D8 L	D9 L	D10	D11	D12	D13			LE L L L L L L L L L L L L L L L L L L	CL L L L L L L	SW8	SW9	SW10	SW11	SW12	SW13		
D8 L	D9 L	D10	D11	D12	D13			LE L L L L L L L L L L L L L L L L L L	CL L L L L L L L L L L L L L L L L L L	SW8	SW9	SW10	SW11	SW12	SW13		
D8 L	D9 L	D10	D11	D12	D13	D14		LE L L L L L L L L L L L L L L L L L L	CL L L L L L L L L L L L L L L L L L L	SW8	SW9	SW10	SW11	SW12	SW13	SW14	
D8 L	D9 L	D10	D11	D12	D13	D14		LE	CL	SW8	SW9	SW10	SW11	SW12	SW13	SW14	
D8 L	D9 L	D10	D11	D12	D13	D14	D15	LE 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	CL L L L L L L L L L L	SW8	SW9	SW10	SW11	SW12	SW13	SW14	SW15
D8 L	D9 L	D10	D11	D12	D13	D14	D15	LE	CL L L L L L L L L L L L	SW8	SW9	SW10	SW11	SW12	SW13	SW14	SW15
D8 L H	L H	L H	L H	D12	L H	D14	D15	LE 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	CL	SW8	SW9	OFF ON	OFF ON	OFF ON	SW13	SW14	SW15
D8 L	D9 L	D10	D11	D12	D13	D14	D15	LE	CL L L L L L L L L L L L	SW8	SW9	OFF ON	OFF ON	SW12	SW13	SW14	SW15

X = Don't care

## Note

- 1. The 16 Switches operate independently.
- 2. When LE is low, the shift register data flows through the latch.
- 3. Shift register clocking has no effect on the switch states if LE is high.
- 4. When switch 15 is ON, DOUT is high.
- 5. The clear input overrides all other inputs.

## 8. Pin Configuration

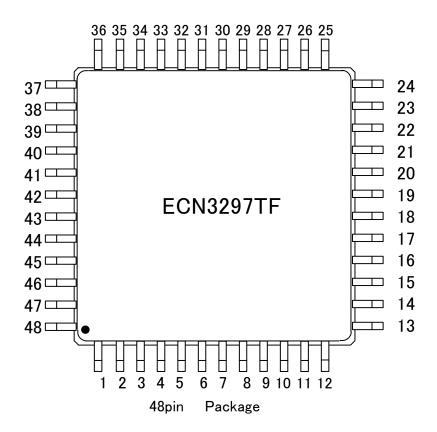
ECN3297TF TQFP48 (48Pin TQFP)

Table7. Pin Configuration

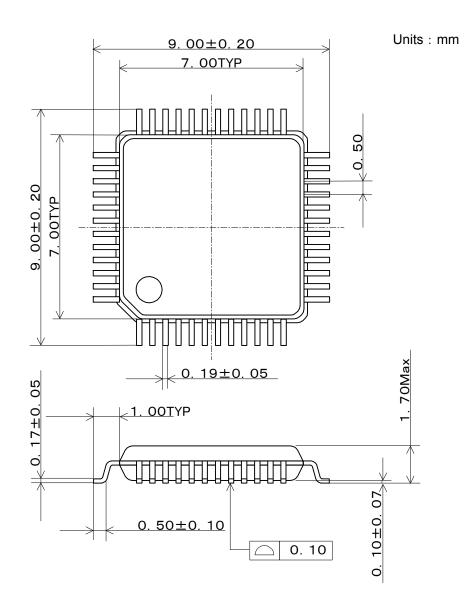
	Tab	ier. Pin Coniiguration	
Pin	Name	Functions	Note
1	N/C	No connection.	*1
2	N/C	No connection.	*1
3	SW4B	Analog Switch 4	
4	SW4A	Analog Switch 4	
5	SW3B	Analog Switch 3	
6	SW3A	Analog Switch 3	
7	SW2B	Analog Switch 2	
8	SW2A	Analog Switch 2	
9	SW1B	Analog Switch 1	
10	SW1A	Analog Switch 1	
11	SW0B	Analog Switch 0	
12	SW0A	Analog Switch 0	
13	VNN	Negative High Voltage Supply.	*2
14	N/C	No connection.	*1
15	VPP	Positive High Voltage Supply.	*2
16	N/C	No connection.	*1
17	GND	Ground	
18	VDD	Logic Supply Voltage	
19	DIN	Serial Data Input	
20	CLK	Serial Clock Input	
21	LE	Latch-Enable Input	
22	CLR	Latch-Clear Input	
23	DOUT	Serial Data Output	
24	RGND	Ground. Connect to Bleed Resister.	*3
25	SW15B	Analog Switch 15	
26	SW15A	Analog Switch 15	
27	SW14B	Analog Switch 14	
28	SW14A	Analog Switch 14	
29	SW13B	Analog Switch 13	
30	SW13A	Analog Switch 13	
31	SW12B	Analog Switch 12	
32	SW12A	Analog Switch 12	
33	SW11B	Analog Switch 11	
34	SW11A	Analog Switch 11	
35	N/C	No connection.	*1
36	N/C	No connection.	*1
37	SW10B	Analog Switch 10	
38	SW10A	Analog Switch 10	
39	SW9B	Analog Switch 9	
40	SW9A	Analog Switch 9	
41	SW8B	Analog Switch 8	
42	SW8A	Analog Switch 8	
43	SW7B	Analog Switch 7	
44	SW7A	Analog Switch 7	
45	SW6B	Analog Switch 6	
46	SW6A	Analog Switch 6	
47	SW5B	Analog Switch 5	
48	SW5A	Analog Switch 5	

Note 1. NOT connected on chip internal.

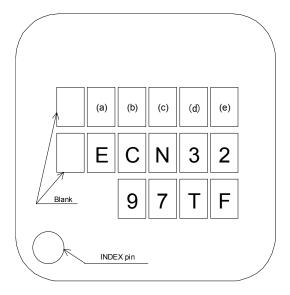
- 2. High voltage supply.
- 3. Connected all analog switches with bleed resistor on chip internal.



## 9. Package Outline



## 10. Marking spec



## Lot numbering rule

(a) :Year code (Least significant digit of Assembled year (A.D.))

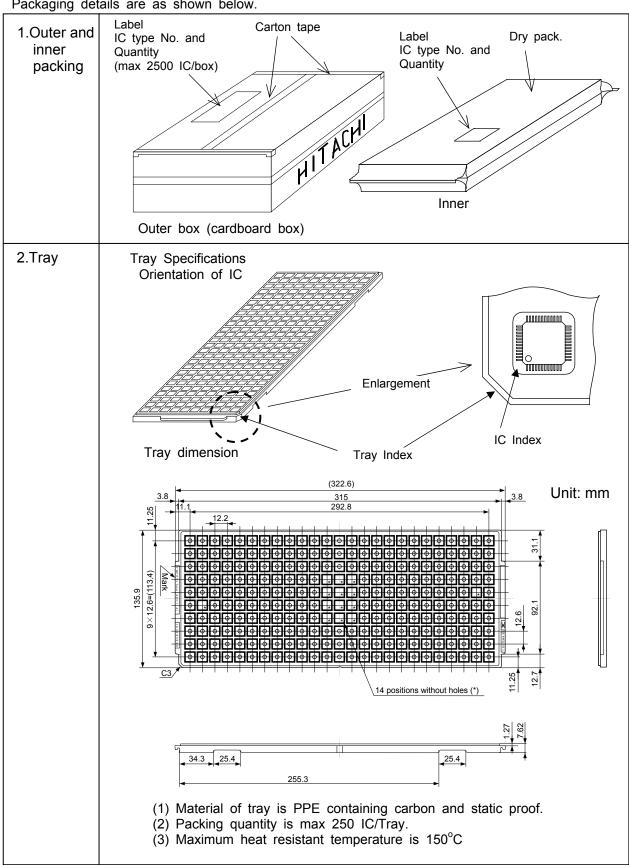
(b) :Month code (Refer to following table.)

- 4	,		,										
	Month	1	2	3	4	5	6	7	8	9	10	11	12
	Month code	Α	В	С	D	Е	К	L	М	N	Х	Υ	Z

(c),(d),(e) :Serial number within year/month code

### 11 Packing Form

Packaging details are as shown below.



### 12 Inspection

Hundred percent inspections shall be conducted on electric characteristics.

### 13. Important Notice

- 13.1 Hitachi warrants performance of its power semiconductor products (hereinafter called "products") to the specifications applicable at the time of sale in accordance with the Product Specification. Testing and other quality control techniques are utilized to the extent Hitachi needs to meet specifications described in the Product Specification. Specific testing of all parameters of each device is not necessarily performed, except those mandated by related laws and/or regulations.
- 13.2 Should any claim be made within one month of product delivery about products' failure to meet performance described in the Product Specification, all the products in relevant lot(s) shall be retested and re-delivered. Products delivered more than one month before of such claim shall not be counted for such response.
- 13.3 Hitachi assumes no obligation or any way of compensation should any fault about customer's goods using products be found in marketplace. Only in such a case fault of Hitachi is evident and products concerned do not meet the Product Specification, compensation shall be conducted if claimed within one year of product delivery up to in the way of product replacement or payment of equivalent amount.
- 13.4 Hitachi reserves the right to make changes in the Product Specification and to discontinue mass production of the relevant products without notice. Customers are advised before purchasing to confirm specification of the product of inquiry is the latest version and that the relevant product is on mass production status in such a case purchasing is suspended for one year or more.
- 13.5 In no event shall Hitachi be liable for any damage that may result from an accident or any other cause during operation of the user's units according to this Product Specification. Hitachi assumes no responsibility for any intellectual property claims or any other problems that may result from applications of information, products or circuits described in this Product Specification.
- 13.6 No license is granted by this Product Specification under any patents or other rights of any third party or Hitachi Power Semiconductor Device, Ltd.
- 13.7 This Product Specification may not be reproduced or duplicated, in any form, in whole or in part, without the expressed written permission of Hitachi Power Semiconductor Device, Ltd.
- 13.8 The products (technologies) described in this Product Specification are not to be provided to any party whose purpose in their application will hinder maintenance of international peace and safety nor are they to be applied to that purpose by their direct purchasers or any third party. When exporting these products (technologies), the necessary procedures are to be taken in accordance with related laws and regulations.

#### 13 Cautions

- 14.1 Customers are advised to follow the below cautions to protect semiconductor from electrical static discharge (ESD).
  - a) IC needs to be dealt with caution to protect from damage by ESD. Material of container or any device to carry semiconductor devices should be free from ESD which may be caused by vibration while transportation. To use electric-conductive container or aluminum sheet is recommended as an effective countermeasure.
  - b) Those what touch semiconductor devices such as work platform, machine and measuring and test equipment should be grounded.
  - c) Workers should be grounded connecting with high impedance around  $100k\Omega$  to  $1M\Omega$  while dealing with semiconductor to avoid damaging IC by electric static discharge.
  - d) Friction with other materials such as a high polymer should not be caused.
  - e) Attention is needed so that electric potential will be kept on the same level by short circuit terminals when PC board with mounted IC is carried and that vibration or friction might not occur.
  - f) Air conditioningis needed so that humidity should not drop.
- 14.2 Refer to the latest version of "Instructions for Use of Hitachi High-Voltage Monolithic ICs" for the other precautions and instructions on how to deal with products.
- 14.3 Regardless of changes in external conditions during use, "absolute maximum ratings" should never be exceeded in designing electronic circuits that employ products. In a case absolute maximum ratings are exceeded, products may be damaged or destroyed. In no event shall Hitachi be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.
- 14.4 Products may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure.
- 14.5 Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment).
  - Inclusion of products in such application shall be fully at the risk of customers. Hitachi Power Semiconductor Device, Ltd. assumes no liability for applications assistance, customer product design, or performance.
  - In such cases it is advised customers ensure circuit and/or product safety by using semiconductor devices that assures high reliability or by means of user's fail-safe precautions or other arrangement.
  - (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)
- 14.6 Lead-free solder is used for coating pins and the tab of this IC. Refer to the latest version of "Instructions for Use of Hitachi High-Voltage Monolithic ICs" for soldering conditions.

## ◆Appendix-Supplementary Data

Please read follows contents before using this product.

## **Function Discription**

#### 1. Bleed resistor

ECN3297TF feature integrated  $35k\Omega$  bleed resistor to discharge capacitive Loads such as piezoelectric transducers. Each analog switch terminal is coneccted RGND with a bleed resistor.

### 2. Overvoltage Protection

ECN3297TF feature clamping diodes to protect circuit against the overvoltage exceed VPP or VNN. ALL analog switches connect VPP and VNN terminals with clamping diode. Normaly, switch input voltage must not exceed VNN and VPP, and maximum current flows through the clamping diode should be less than 1A.

### 3. Power supply seaguence

ECN3297TF doesn't require special sequencing of the VPP, VNN, and VDD supply voltages. However, logic state is unsettled when power-up. After power-up, please refer to the truth table (Page. 8 Table. 7) and set the data of shift register.

## Precautions for Safe Use and Notices

If semiconductor devices are handled inappropriate manner, failures may result. For this reason, be sure to read the latest version of "Instructions for Use of Hitachi High-Voltage Monolithic ICs" before use.



This mark indicates an item about which caution is required.



### **CAUTION**

This mark indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury and damage to property.

## /!

## **CAUTION**

- (1) Regardless of changes in external conditions during use "absolute maximum ratings" should never be exceed in designing electronic circuits that employ semiconductors. In the case of pulse use, furthermore, "safe operating area (SOA)" precautions should be observed.
- (2) Semiconductor devices may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure.
- (3) In cases where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment), safety should be ensured by using semiconductor devices that feature assured safety or by means of user's fail-safe precautions or other arrangement. Or consult Hitachi's sales department staff.

(If a semiconductor devices fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst)

## NOTICES

- 1. This Data Sheet contains the specifications, characteristics (in figures and tables), dimensions and handling notes concerning power semiconductor products (hereinafter called "products") to aid in the selection of suitable products.
- 2. The specifications and dimensions, etc. stated in this Data Sheet are subject to change without prior notice to improve products characteristics. Before ordering, purchasers are advised to contact Hitachi's sales department for the latest version of this Data Sheet and specifications.
- 3. In no event shall Hitachi be liable for any damage that may result from an accident or any other cause during operation of the user's units according to this Data Sheet. Hitachi assumes to responsibility for any intellectual property claims or any other problems that may result from applications of information, products or circuits described in this Data Sheet.
- 4. In no event shall Hitachi be liable for any failure in a semiconductor device or any secondary damage resulting from use at a value exceeding the absolute maximum rating.
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Refer to the following website for the latest information. Consult Hitachi's sales department staff if you have any questions.

http://www.hitachi-power-semiconductor-device.co.jp/en/