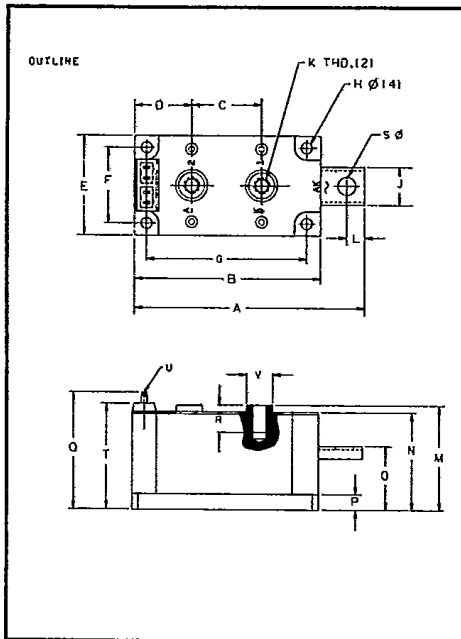


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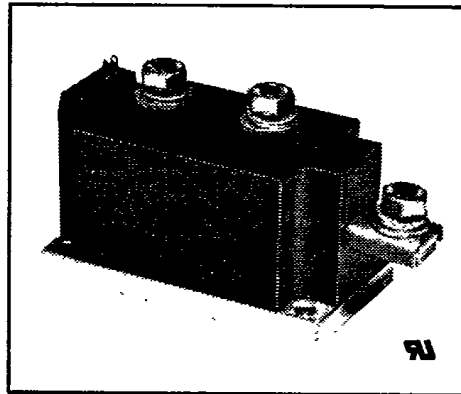
ED _____ 13
 ED _____ 16
 ED41 _____ 20

Dual SCR SCR/Diode Isolated Modules 130-160-200 Amperes 100-2400 Volts



**Dual SCR, SCR/Diode
 Isolated Modules
 Outline Drawing**

Dimension	Inches	Millimeters
A	4.52	115
B	3.66	93
C	1.38	35
D	1.12	28.5
E	1.97	50
F	1.50	38
G	3.15	80
H	.22	5.5
J	.74	18.5
K	—	M8
L	.35	9
M	2.05	52
N	1.93	49
O	1.26	32
P	.31	8
Q	2.16	55
R	.55	14
S	—	M8
T	2.09	53.1
U	.110 X .032	2.8 X 0.8
V	.52	13



**Dual SCR, SCR/Diode
 Isolated Modules
 130-160-200 Amperes/100-2400 Volts**

Ordering Information

Example: Select the complete eight digit rating module part number you desire from the table — i.e. ED430816 is an 800 Volt, 160 Ampere Dual SCR Phase Control Module.

Type	V _{DRM} Volts (x100)	Current Rating Amperes (x10)
ED41	01	13
ED42	02	16
ED43	04	20*
ED45**	06	
ED46**	08	
ED47	10	
ED48*	12	
ED72	14	
ED77	16	
	18	
	20	

Note: All voltages are not available in every type. Insert code in digits 5 and 6 of part number to specify voltage (example: ED430816 is a 600 Volt, 160 Ampere dual SCR module). Diode voltage is same as SCR except for ED72, ED77, where suffix OY or OZ is added to denote 1.7 times SCR or 2.0 times SCR (example: ED721213OZ provides 1200 Volts SCR, 2400 Volt Diode).

*200A rating available in ED41 type only.

**Consult factory for available rating.

Description

The POW-R-BLOK™ combines multiple power semiconductor devices in a single, electrically isolated module.


POW-R-BLOK™ can serve as the essential circuit element in many industrial applications, such as motor speed control, battery chargers, tap changers, transfer switches, and lighting controls. A variety of dual diode and SCR and diode combinations are available for use in 120, 240, 480 or 575 volt power line applications.

Semiconductor elements are secured by CBE (Compression Bonded Encapsulation) for excellent cycling performance.

POW-R-BLOK™ features a self-contained electrical isolation system. By using high thermal conductivity BeO ceramic isolators, excellent circuit-to-baseplate isolation (≥ 2500 volts RMS) has been achieved, while maintaining efficient cooling of the semiconductors. POW-R-BLOK™ has been tested and recognized by Underwriters Laboratories (QQQX2 Power Switching Semiconductors).

All ED Series SCR's use the "di/Namic" gate structure for ease of triggering and high di/dt capability.

Features:

- Compression Bonded Encapsulation
- Isolated Base Plate
- Insulated Package
- Low Thermal Impedance
- Metal Base Plate
- UL Recognized 

Benefits:

- No Additional Insulating Components Required
- Easy Installation
- Reduced Engineering Time
- Improved Heat Transfer
- Voltage Stability

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ED _____ 13, ED _____ 16, ED41 _____ 20
 Dual SCR, SCR/Diode Isolated Modules
 130-160-200 Amperes/100-2400 Volts

Absolute Maximum Ratings

Characteristics	Symbol	ED _____ 13	ED _____ 16	ED41 _____ 20	Units
Peak Forward Blocking Voltage	V_{DRM}	SCR to 1600			Volts
Peak Reverse Blocking Voltage	V_{RRM}	SCR to 1600, Diode to 2400			Volts
Transient Peak Reverse Blocking Voltage (Non-Repetitive) $t < 5$ ms	V_{RSM}	SCR to 1800, Diode to 2600			Volts
DC Reverse Blocking Voltage	$V_{R(DC)}$	SCR to 1280, Diode to 1920			Volts
RMS On-State Current	$I_{T(RMS)}, I_{F(RMS)}$	200	250	314	Amperes
Average On-State Current	$I_{T(AV)}, I_{F(AV)}$	130	160	200	Amperes
Peak One-Cycle Surge (Non-Repetitive) On-State Current (60Hz)	I_{TSM}, I_{FSM}	5000	5400	5800	Amperes
Peak Three-Cycle Surge (Non-Repetitive) On-State Current (60Hz)	I_{TSM}, I_{FSM}	3500	3800	4100	Amperes
Peak Ten-Cycle Surge (Non-Repetitive) On-State Current (60 Hz)	I_{TSM}, I_{FSM}	3100	3350	3600	Amperes
I^2t (for Fusing), 8.3 milliseconds	I^2t	103,750	121,000	139,600	A ² sec
Critical Rate-of-Rise of On-State Current $\text{\textcircled{1}}$ (Non-Repetitive)	di/dt	800	800	800	Amperes/ μ s
Peak Gate Power Dissipation	P_{GM}	16	16	16	Watts
Average Gate Power Dissipation	$P_{G(AV)}$	3.0	3.0	3.0	Watts
Peak Forward Gate Voltage	V_{GFM}	10	10	10	Volts
Peak Reverse Gate Voltage	V_{GRM}	5.0	5.0	5.0	Volts
Peak Forward Gate Current	I_{GFM}	4.0	4.0	4.0	Amperes
Storage Temperature	T_{STG}	-40 to 150	-40 to 150	-40 to 150	$^{\circ}$ C
Operating Temperature	T_J	-40 to 130	-40 to 130	-40 to 130	$^{\circ}$ C
Maximum Mounting Torque M6 Mounting Screw	—	50	50	50	in.-lb.
Maximum Terminal Torque M8 Terminal Screw	---	130	130	130	in.-lb.
V Isolation	V_{RMS}	2500	2500	2500	Volts

$\text{\textcircled{1}}$ Per JEDEC STD RS-397, 5.2.2.6.

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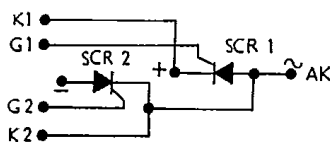
ED _____ 13, ED _____ 16, ED41 _____ 20
Dual SCR, SCR/Diode Isolated Modules
 130-160-200 Amperes/100-2400 Volts

Electrical and Thermal Characteristics $T_J=25^\circ\text{C}$ unless otherwise specified

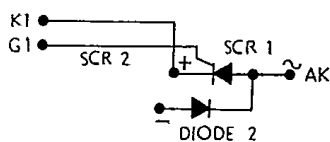
Characteristics	Symbol	Test Conditions	ED _____ 13	ED _____ 16	ED41 _____ 20	Units
Blocking State Maximums						
Forward Leakage Current, Peak	I_{DRM}	$T_J = 130^\circ\text{C}$, $V_{DRM} = \text{rated}$	50	50	50	mA
Reverse Leakage Current, Peak	I_{RRM}	$T_J = 130^\circ\text{C}$, $V_{RRM} = \text{rated}$	50	50	50	mA
Conducting State Maximums						
Peak On-State Voltage	V_{TM}	$I_{TM} = 625\text{A}$	1.55	1.45	—	Volts
Peak On-State Voltage	V_{FM}	$I_{FM} = 800\text{A}$	1.35	1.35	1.35	Volts
Switching Minimums						
Critical Rate of Rise of Off-State Voltage	dv/dt	$T_J = 130^\circ\text{C}$, $V_D = 2/3 V_{DRM}$	300	300	—	Volts/ μsec
Turn-Off Time (Typical)	t_q	$I_{TM} = 150\text{A}$, $T_J = 130^\circ\text{C}$ Reapplied dv/dt = 20V/ μsec linear to 0.8 V_{DRM}	100	100	—	μsec
Turn-On Time (Typical)	t_{on}	$I_{TM} = 100\text{A}$, $V_D = 100\text{V}$	5	5	—	μsec
Diode Reverse Recovery Time (Typical)	t_{rr}	$I_{FM} = 785\text{A}$, $T_p = 100\mu\text{sec}$ - $di/dt = 25 \text{ A}/\mu\text{s}$	10	10	10	μsec
Thermal Maximums						
Thermal Resistance, Junction to Case	$R_{\theta JC}$	Per Module	0.11	0.11	0.11	$^\circ\text{C}/\text{Watt}$
Thermal Resistance, Case to Sink Lubricated	$R_{\theta CS}$	Per Module	0.03	0.03	0.03	$^\circ\text{C}/\text{Watt}$
Gate Parameters Maximums						
Gate Current to Trigger	I_{GT}	$V_D = 12\text{V}$	150	150	—	mA
Gate Voltage to Trigger	V_{GT}	$V_D = 12\text{V}$	3	3	—	Volts
Non-Triggering Gate Voltage	V_{GDM}	$T_J = 130^\circ\text{C}$, $V_D = 1/2 V_{DRM}$	0.15	0.15	—	Volts

Connection Diagrams

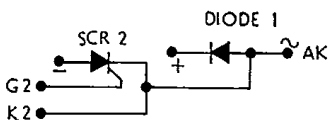
- ED43 Dual SCR Phase Control
- ED46 Dual SCR Fast Switch*



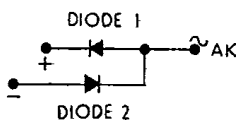
- ED42 SCR/Diode Phase Control
- ED45 SCR/Diode Fast Switch*
- ED72 SCR/Diode Current Source**



- ED47 Diode/SCR Phase Control
- ED48 Diode/SCR Fast Switch*
- ED77 Diode/SCR Current Source**



- ED41 Diode/Diode Standard Recovery
- ED44 Diode/Diode Fast Recovery*

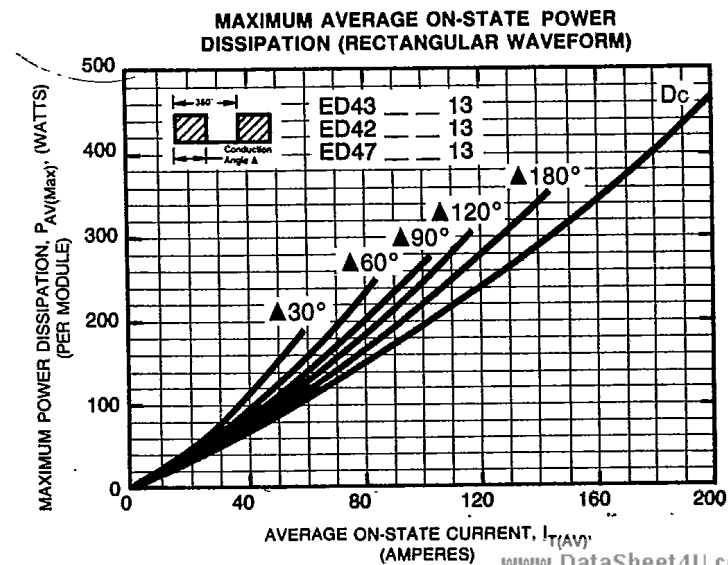
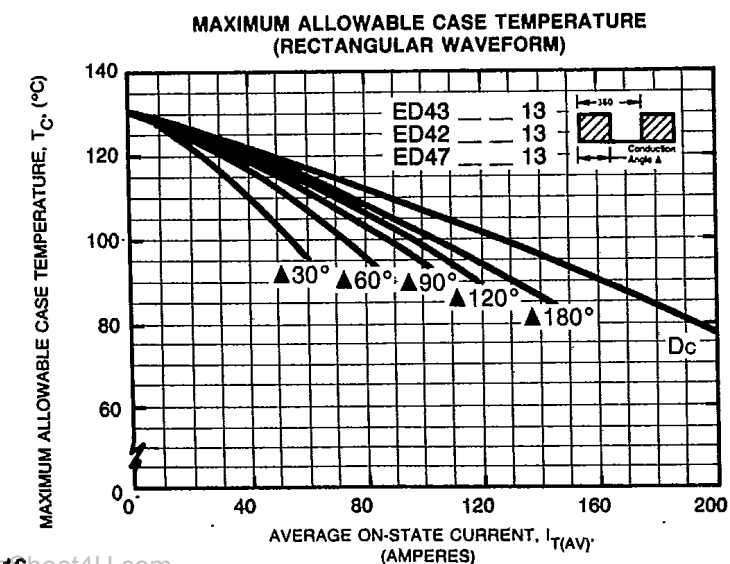
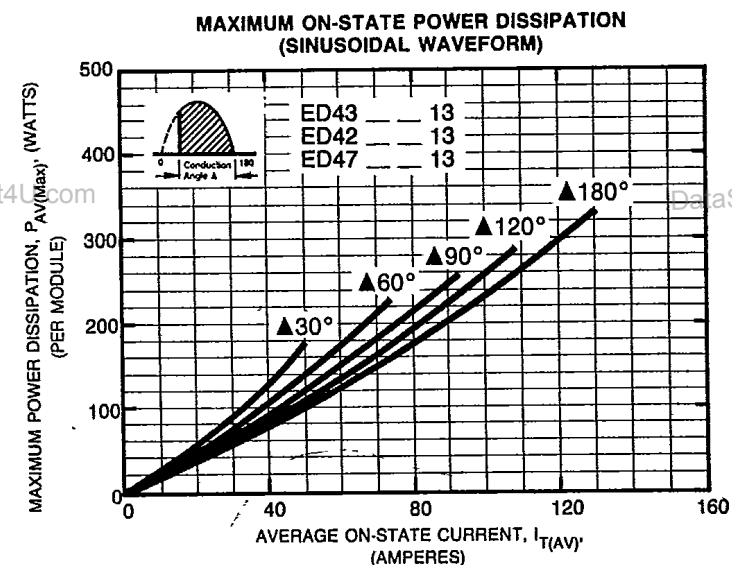
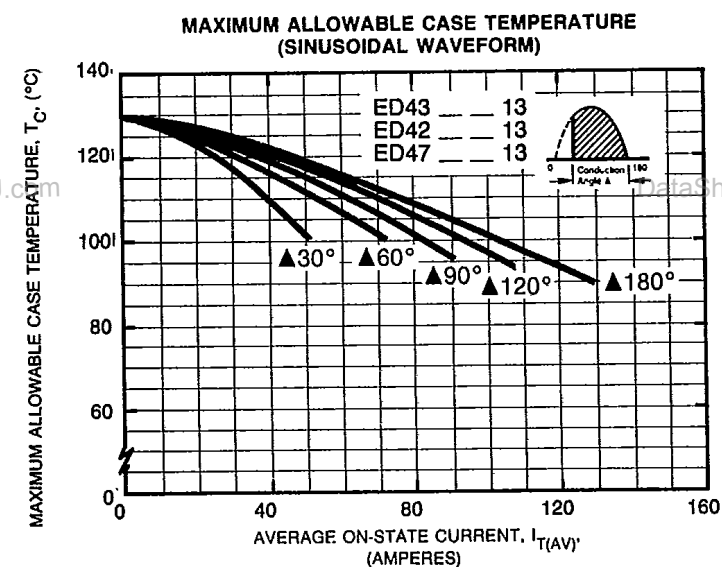
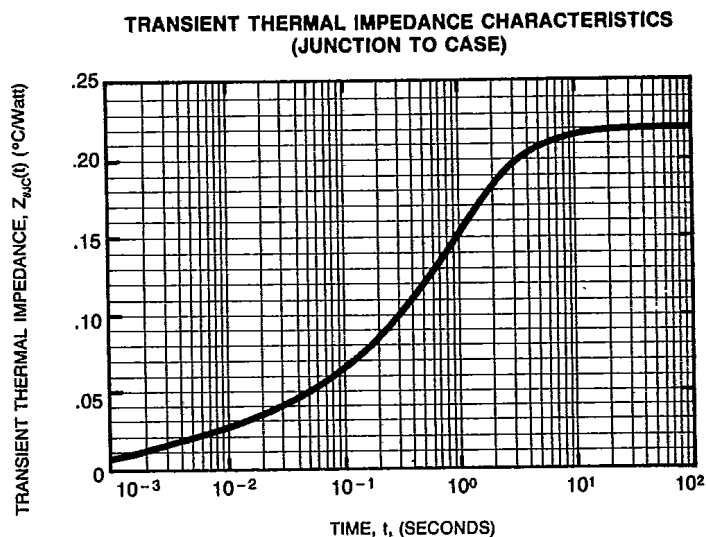
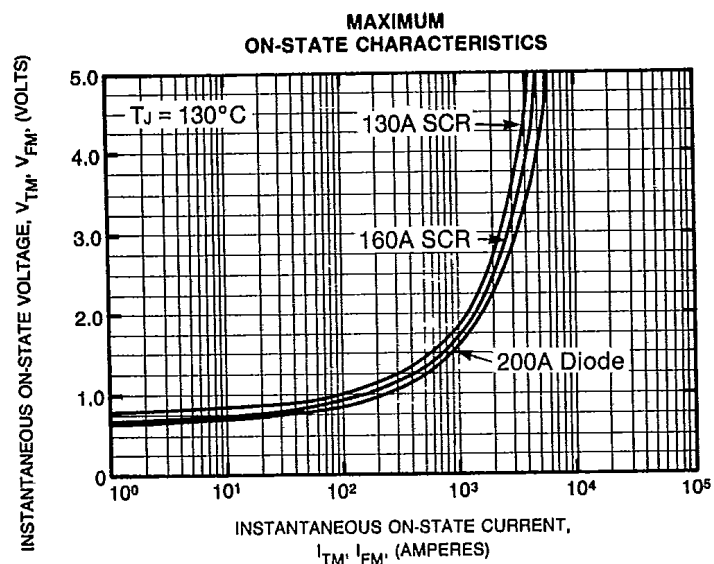


WARNING:
 Internal insulation used is Beryllium Oxide. User should avoid grinding, crushing or abrading these portions. Care must be exercised in properly disposing of unwanted modules.

*Consult factory for available ratings
 **Ratings identical to ED42/ED47

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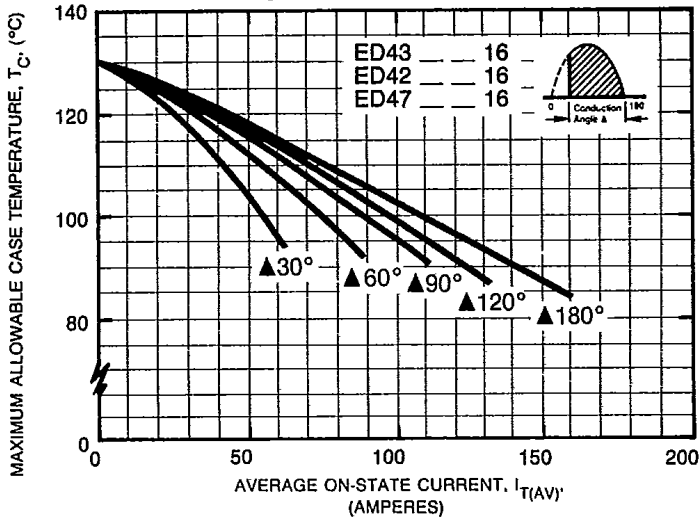
ED 13, ED 16, ED41 20
Dual SCR, SCR/Diode Isolated Modules
 130-160-200 Amperes/100-2400 Volts



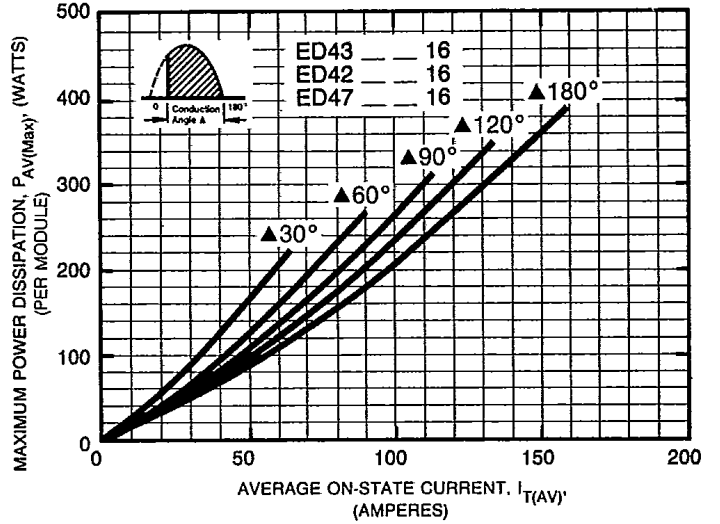
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ED _____ 13, ED _____ 16, ED41 _____ 20
 Dual SCR, SCR/Diode Isolated Modules
 130-160-200 Amperes/100-2400 Volts

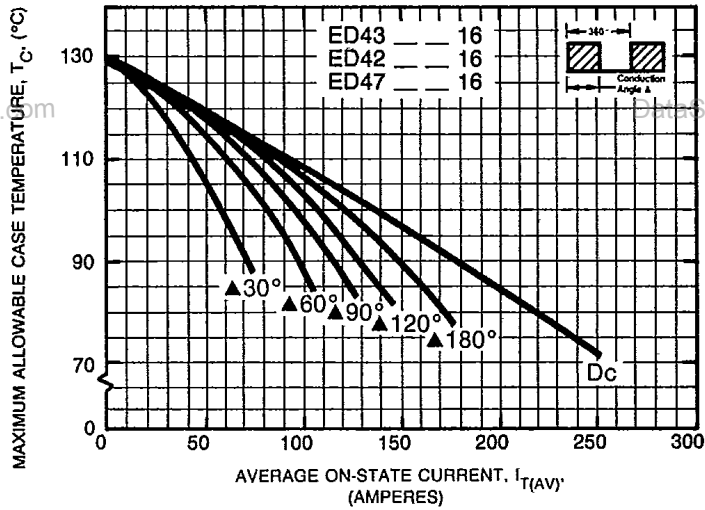
MAXIMUM ALLOWABLE CASE TEMPERATURE (SINUSOIDAL WAVEFORM)



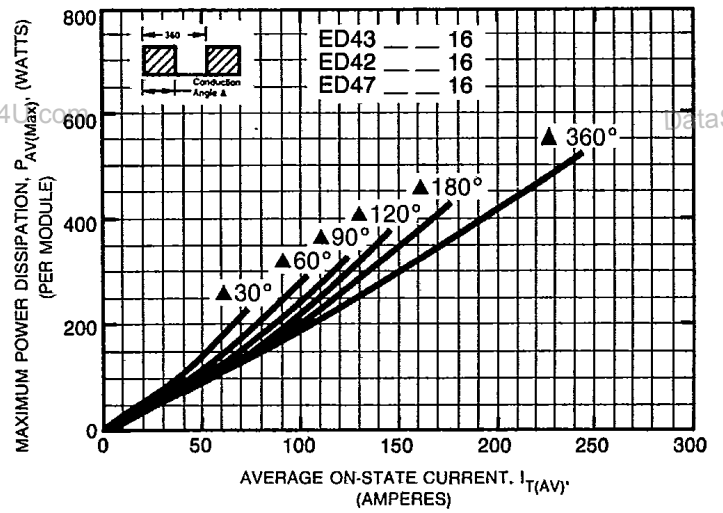
MAXIMUM ON-STATE POWER DISSIPATION (SINUSOIDAL WAVEFORM)



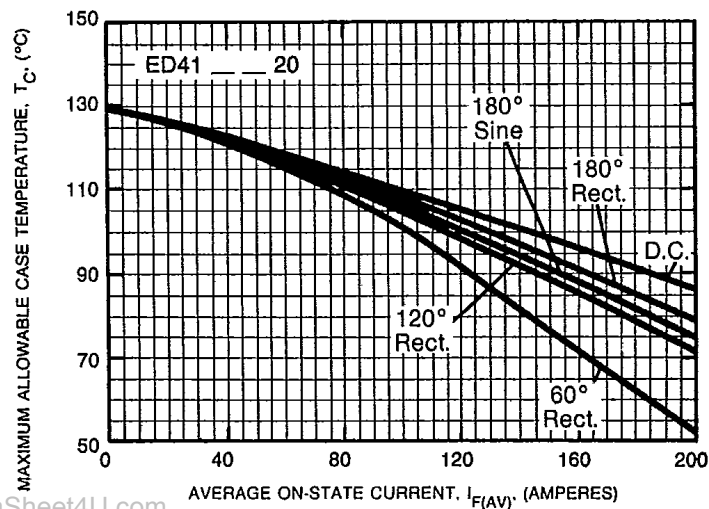
MAXIMUM ALLOWABLE CASE TEMPERATURE (RECTANGULAR WAVEFORM)



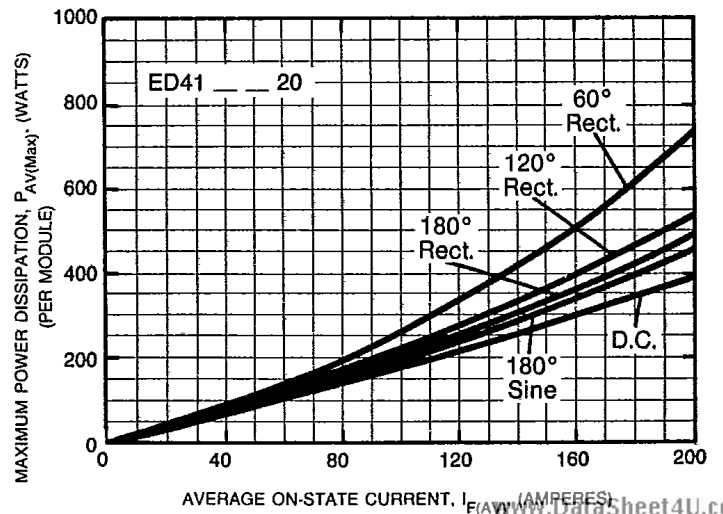
MAXIMUM AVERAGE ON-STATE POWER DISSIPATION (RECTANGULAR WAVEFORM)



MAXIMUM ALLOWABLE CASE TEMPERATURE



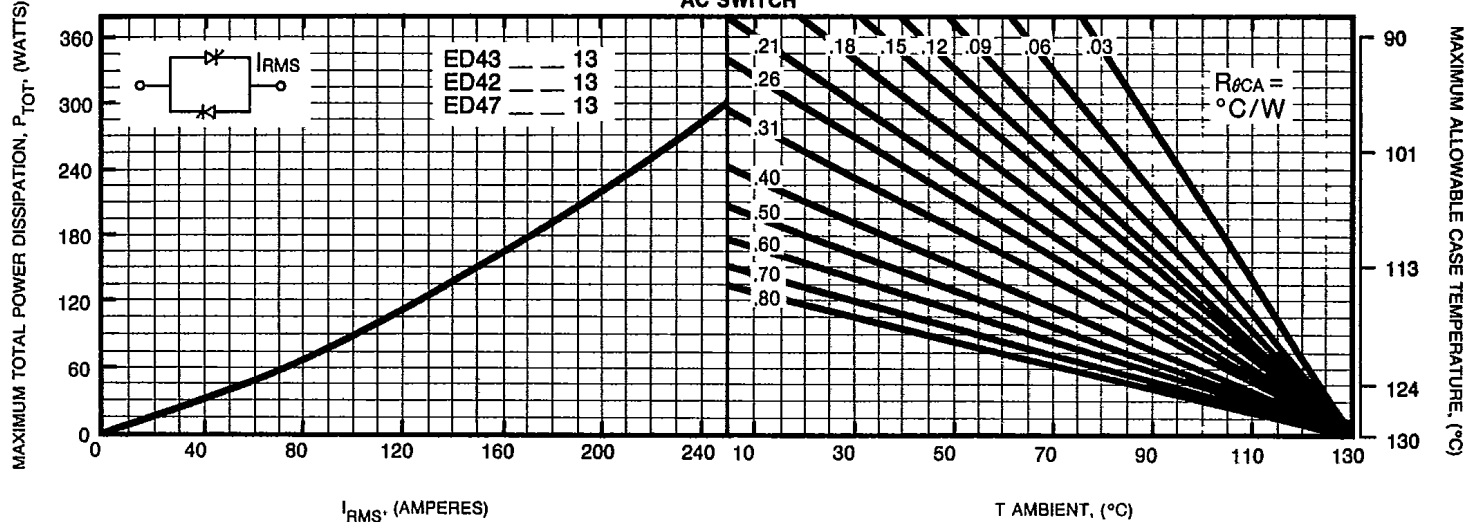
MAXIMUM ON-STATE POWER DISSIPATION



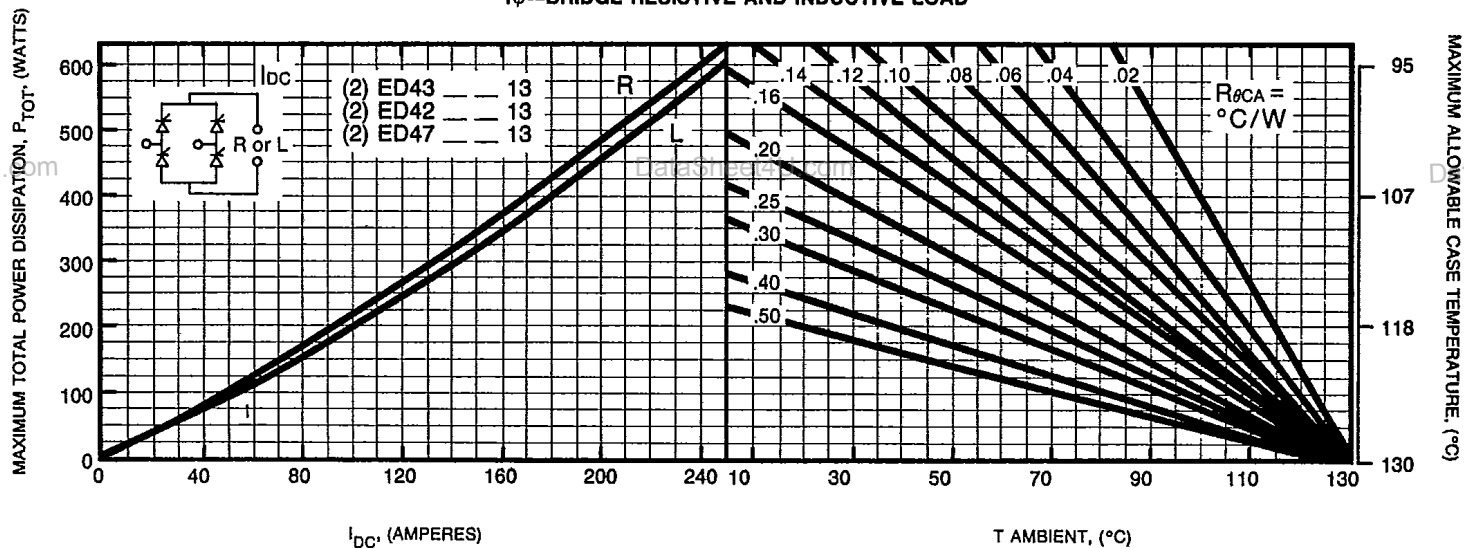
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ED _____ 13, ED _____ 16, ED41 _____ 20
Dual SCR, SCR/Diode Isolated Modules
130-160-200 Amperes/100-2400 Volts

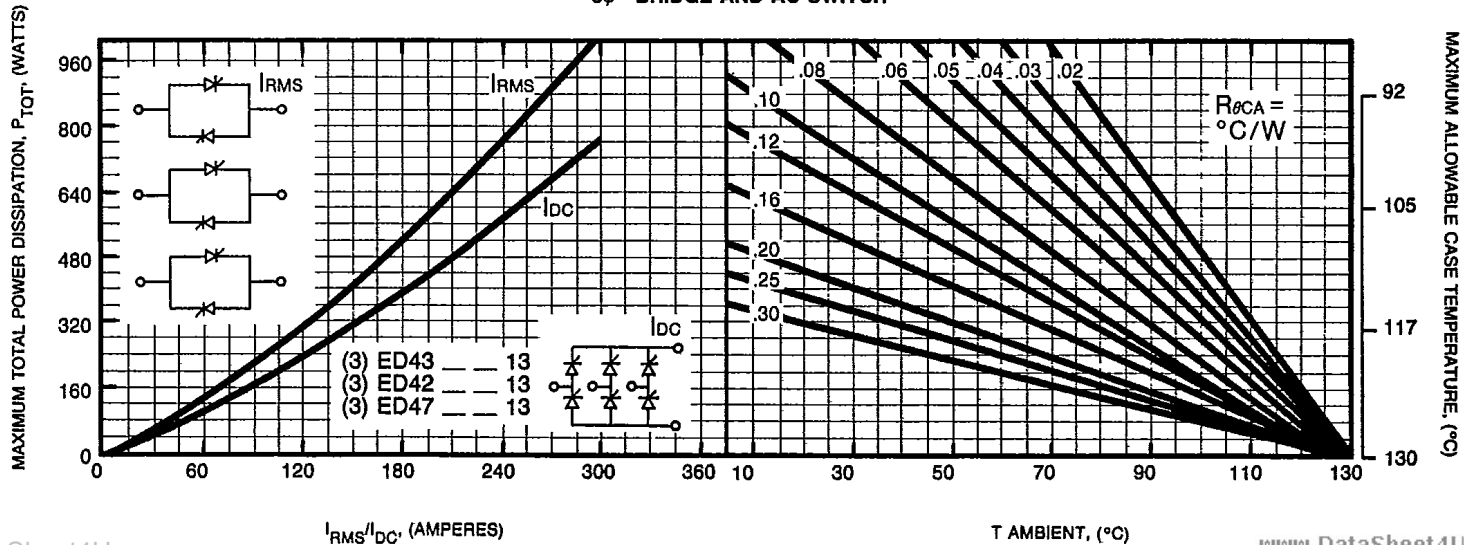
MAXIMUM TOTAL POWER DISSIPATION AND MAXIMUM AMBIENT TEMPERATURES
AC SWITCH



1 ϕ -BRIDGE RESISTIVE AND INDUCTIVE LOAD



3 ϕ -BRIDGE AND AC SWITCH

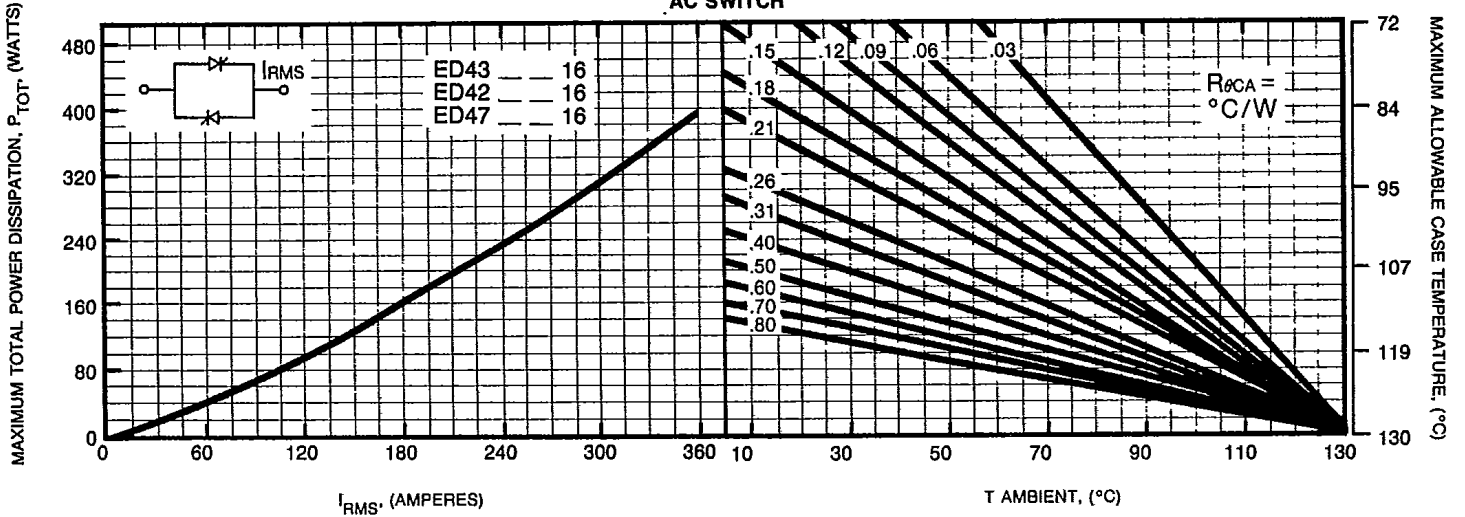


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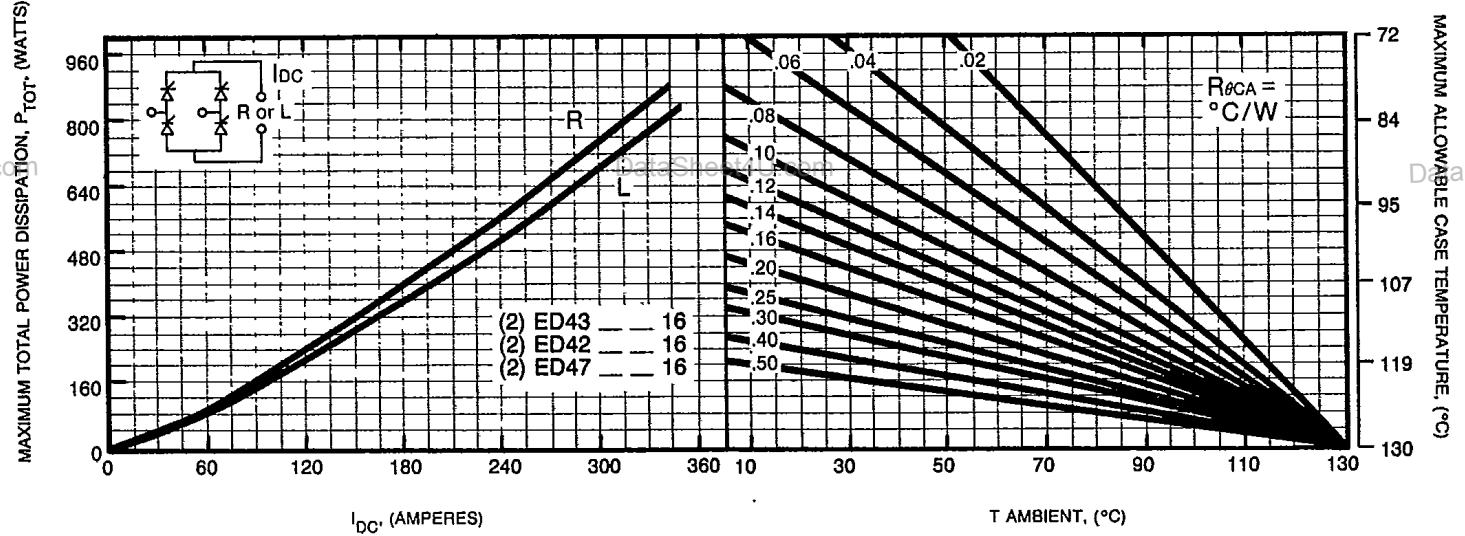
ED _____ 13, ED _____ 16, ED41 _____ 20
 Dual SCR, SCR/Diode Isolated Modules
 130-160-200 Amperes/100-2400 Volts

MAXIMUM TOTAL POWER DISSIPATION AND MAXIMUM AMBIENT TEMPERATURES

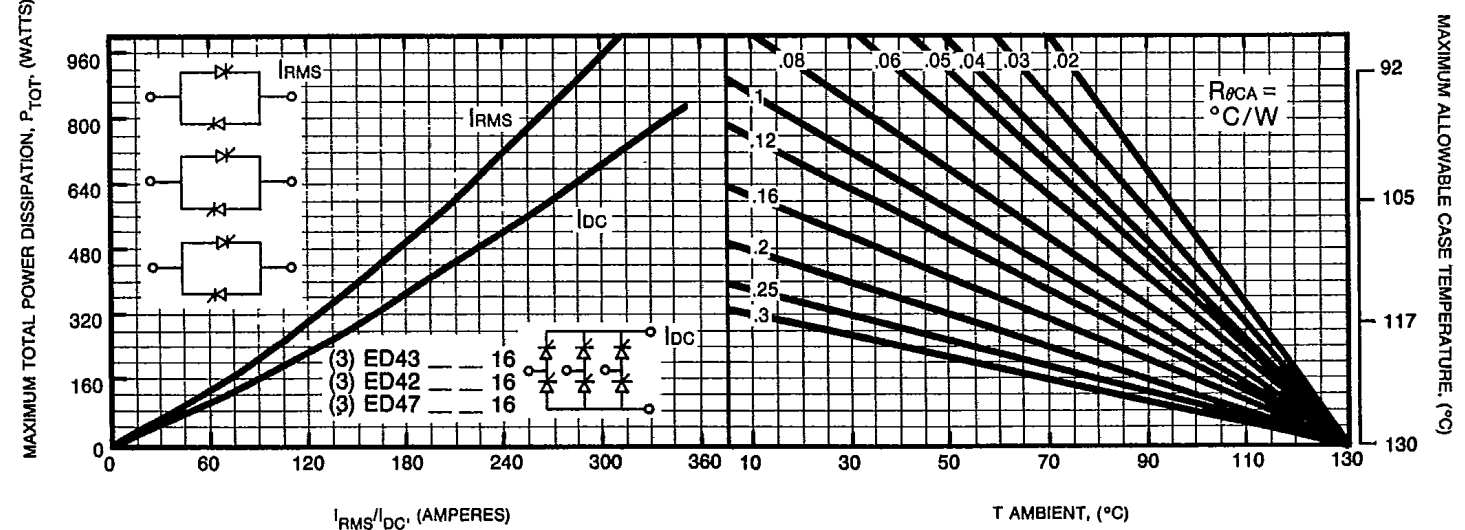
AC SWITCH



1 ϕ —BRIDGE RESISTIVE AND INDUCTIVE LOAD



3 ϕ —BRIDGE AND AC SWITCH

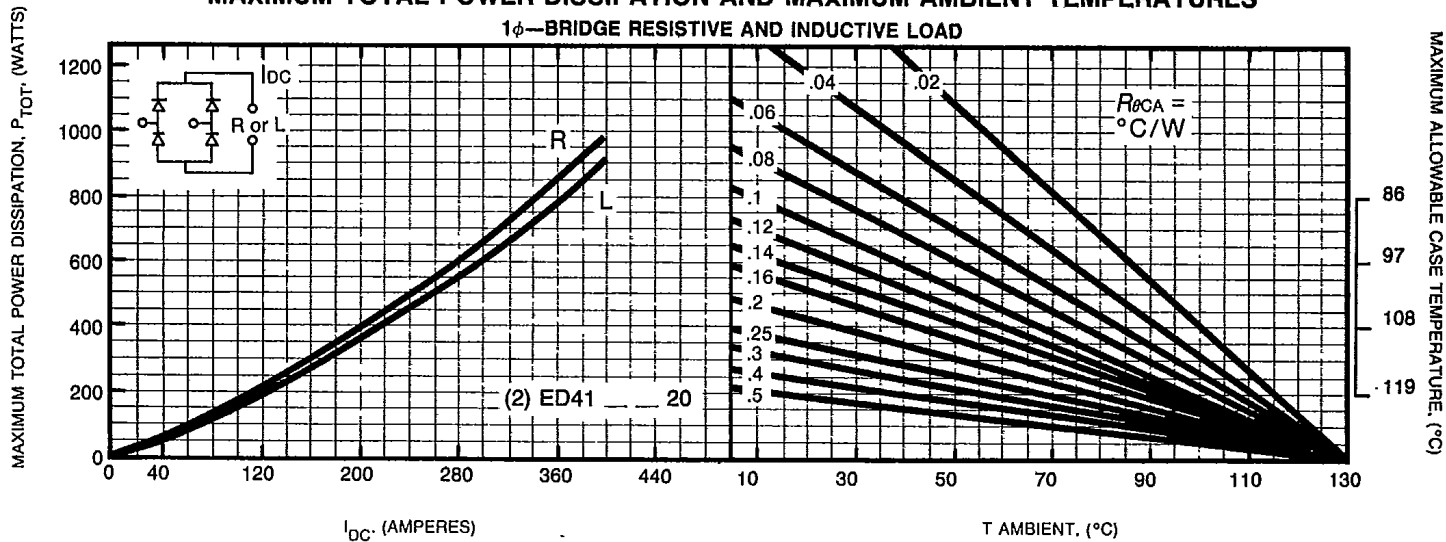


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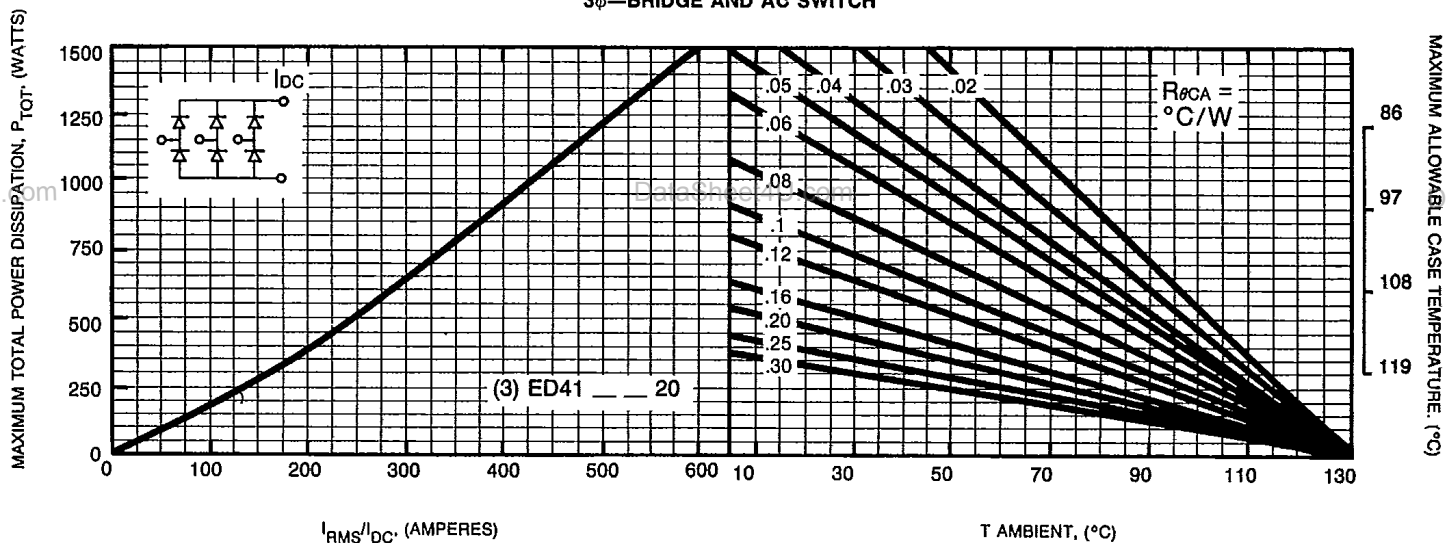
ED _____ 13, ED _____ 16, ED41 _____ 20
 Dual SCR, SCR/Diode Isolated Modules
 130-160-200 Amperes/100-2400 Volts

MAXIMUM TOTAL POWER DISSIPATION AND MAXIMUM AMBIENT TEMPERATURES

1 ϕ —BRIDGE RESISTIVE AND INDUCTIVE LOAD



3 ϕ —BRIDGE AND AC SWITCH

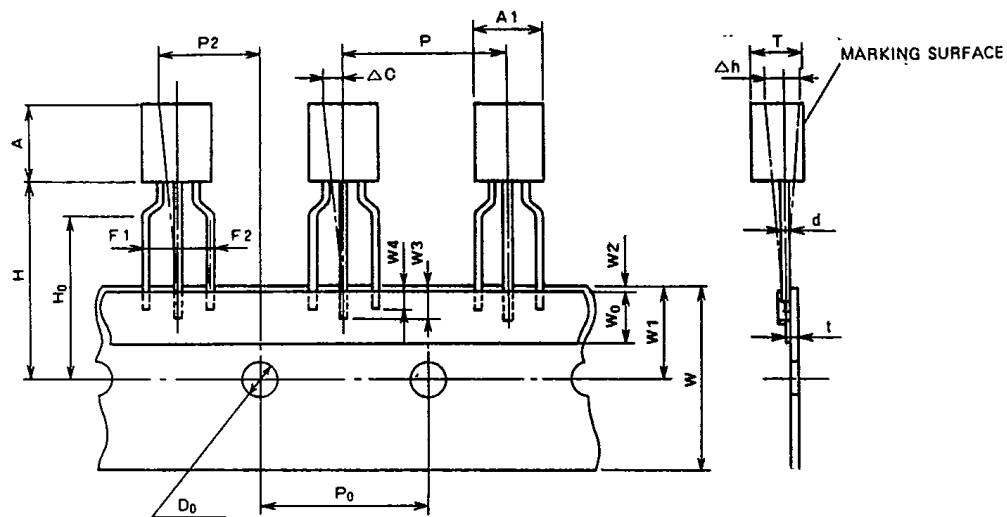


Taping

STANDARD SPECIFICATIONS FOR TAPING OF MOLDED PACKAGE THYRISTORS AND TRIACS

TO-92 Package

Thyristor
CR02AM, CR03AM, CR04AM
Triac
BCR1AM

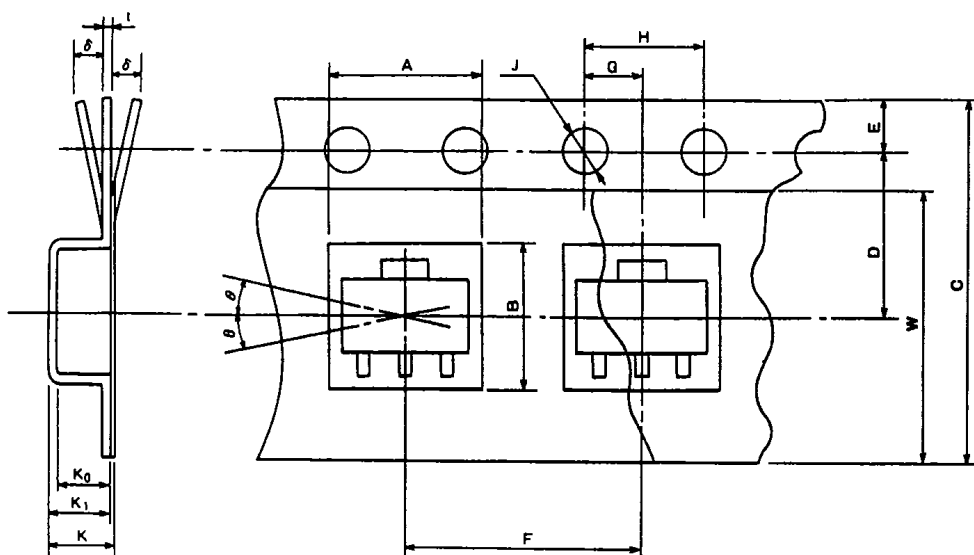


Taping dimensions

Description of symbol	Symbol	Dimensions (Unit:mm)	Remark
Product width	A1	5.0 MAX	
Product height	A	5.0 MAX	
Product thickness	T	3.7 MAX	
Lead wire diameter	d	0.6 MAX	
Sticker lead wire length (1)	W3	2.5 MIN	
Sticker lead wire length (2)	W4	2.0 MIN	
Pitch between products	P	12.7 ± 1.0	
Feed hole pitch	P ₀	12.7 ± 0.3	The cumulative pitch error is ± 1mm per 20 pitches.
Feed hole deviation (1)	P2	6.35 ± 1.3	
Distance between lead wires	F1, F2	2.5 ± 0.4	
Defective product (1)	Δh	0 ± 2.0	
Tape width	W	18.0 ± $\begin{smallmatrix} 1.0 \\ 0.5 \end{smallmatrix}$	
Sticker tape width	W ₀	6.0 ± 0.5	
Feed hole deviation (2)	W1	9.0 ± 0.5	
Sticker tape deviation	W2	0.5 MAX	
Position of product bottom surface	H	17.5 MIN	
Lynch height of lead wire	H ₀	16.0 ± 0.5	
Feed hole diameter	D ₀	4.0 ± 0.2	
Tape thickness	t	0.7 ± 0.2	
Defective product (2)	ΔC	0 ± 1.0	

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Powerex Semiconductor Data Book
 Taping



SOT-89 Package

Thyristor
 CR08AS

Taping dimensions

Description of symbol		Symbol	Dimensions/angles Unit:mm	Remark
Parts insertion	Height	A	5.0 ± 0.1	Cross-section of the surface 0.5mm above the inner bottom
	Width	B	4.6 ± 0.1	Cross-section of the surface 0.5mm above the inner bottom
Concave square hole	Depth	K_0	1.8 ± 0.1	Inner space
	Pitch	F	8.0 ± 0.1	Cumulative error +0.1/-0.3 MAX/10 pitches
Round feed hole	Diameter	J	$\phi 1.5 \pm 0.05$	
	Pitch	H	4.0 ± 0.1	Cumulative error +0.1/-0.3 MAX/10 pitches
	Position	E	1.5 ± 0.1	Distance between the tape edge and the hole center
Distance between center lines	Vertical	G	2.0 ± 0.5	Center line of concave square hole and round feed hole
	Horizontal	D	5.65 ± 0.05	Center line of concave square hole and round feed hole
Cover tape	Width	W	$9.5 + 0.3/-0$	Thickness: 0.1 MAX
Carrier tape	Width	C	12 ± 0.2	Warp $\phi 0.3$ MAX
	Thickness	t	0.3 ± 0.05	
	Package hole depth	K_1	2.1 ± 0.1	
Device	Package dimensions	—	—	As shown in (e)
	Inclination	θ	30° MAX.	
Total Thickness		K	2.3 ± 0.1	Total thickness including cover and carrier tapes