



# Data Sheet Addendum: LPDDR2 SDRAM

## EDB8132B4PB-8D-F-R, EDB8132B4PB-8D-F-D

### Features

This addendum documents features of the Micron® 4Gb Mobile Low-Power DDR2 SDRAM (LPDDR2) device.

This addendum does not provide detailed device information. The standard density-specific device data sheet provides a complete description of device functionality, operating modes, and specifications unless specified herein.

Information provided here is in addition to or supersedes information in the device data sheet.

- Ultra-low-voltage core and I/O power supplies
- Frequency range
  - 400 MHz (data rate: 800 Mb/s/pin)
- 4n prefetch DDR architecture
- 8 internal banks for concurrent operation
- Multiplexed, double data rate, command/address inputs; commands entered on each CK\_t/CK\_c edge
- Bidirectional/differential data strobe per byte of data (DQS\_t/DQS\_c)
- Programmable READ and WRITE latencies (RL/WL)
- Burst length: 4, 8, and 16
- Per-bank refresh for concurrent operation
- Auto temperature-compensated self refresh (ATCSR) by built-in temperature sensor
- Partial-array self refresh (PASR)
- Deep power-down mode (DPD)
- Selectable output drive strength (DS)
- Clock-stop capability
- Lead-free (RoHS-compliant) and halogen-free packaging

### Options

- $V_{DD1}/V_{DD2}/V_{DDQ}$ : 1.8V/1.2V/1.2V
- Array configuration
  - 256 Meg x 32 (DDP)
- Packaging
  - 12mm x 12mm, 168-ball PoP FBGA package
- Operating temperature range
  - From -30°C to +85°C

**Table 1: Configuration Addressing – Single-Channel Package**

Architecture	256 Meg x 32
Density per package	8Gb
Die per package	2
Ranks per channel	1
Die per rank	2
Configuration	32 Meg x 16 x 8 banks x 2



## 168-Ball LPDDR2 SDRAM Addendum Features

**Table 1: Configuration Addressing – Single-Channel Package (Continued)**

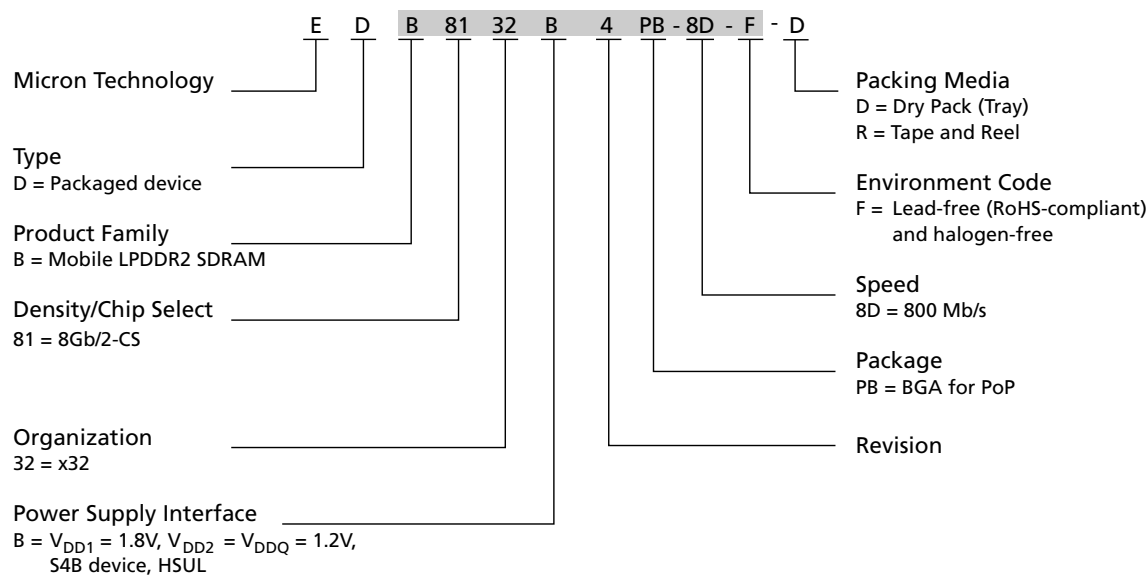
Architecture	256 Meg x 32
Row addressing	16K A[13:0]
Column addressing	2K A[10:0]

**Table 2: Key Timing Parameters**

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	WRITE Latency	READ Latency
8D	400	800	3	6

**Table 3: Part Number Description**

Part Number	Total Density	Configuration	Ranks	Channels	Package Size	Ball Pitch
EDB8132B4PB-8D-F-R, EDB8132B4PB-8D-F-D	8Gb	256 Meg x 32	1	1	12mm x 12mm (0.80mm MAX height)	0.50mm

**Figure 1: Marketing Part Number Chart**


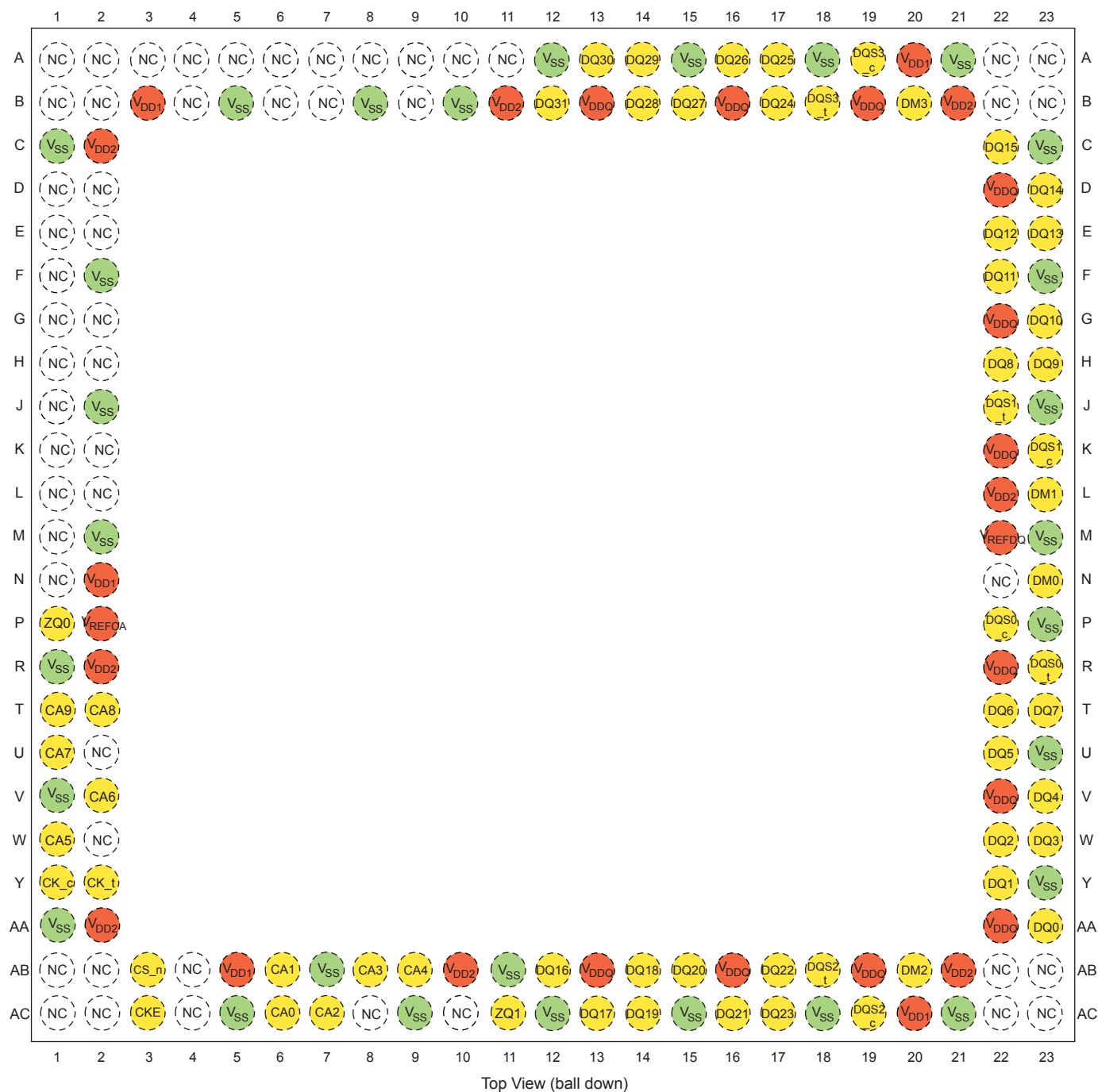
Note: 1. The characters highlighted in gray indicate the physical part marking found on the device.



# 168-Ball LPDDR2 SDRAM Addendum Ball Assignments

## Ball Assignments

Figure 2: 168-Ball PoP Single-Channel FBGA – 2 x 4Gb Die, 12mm x 12mm





## Ball Descriptions

The ball/pad description table below is a comprehensive list of signals for the device family. All signals listed may not be supported on this device. See Ball Assignments for information specific to this device.

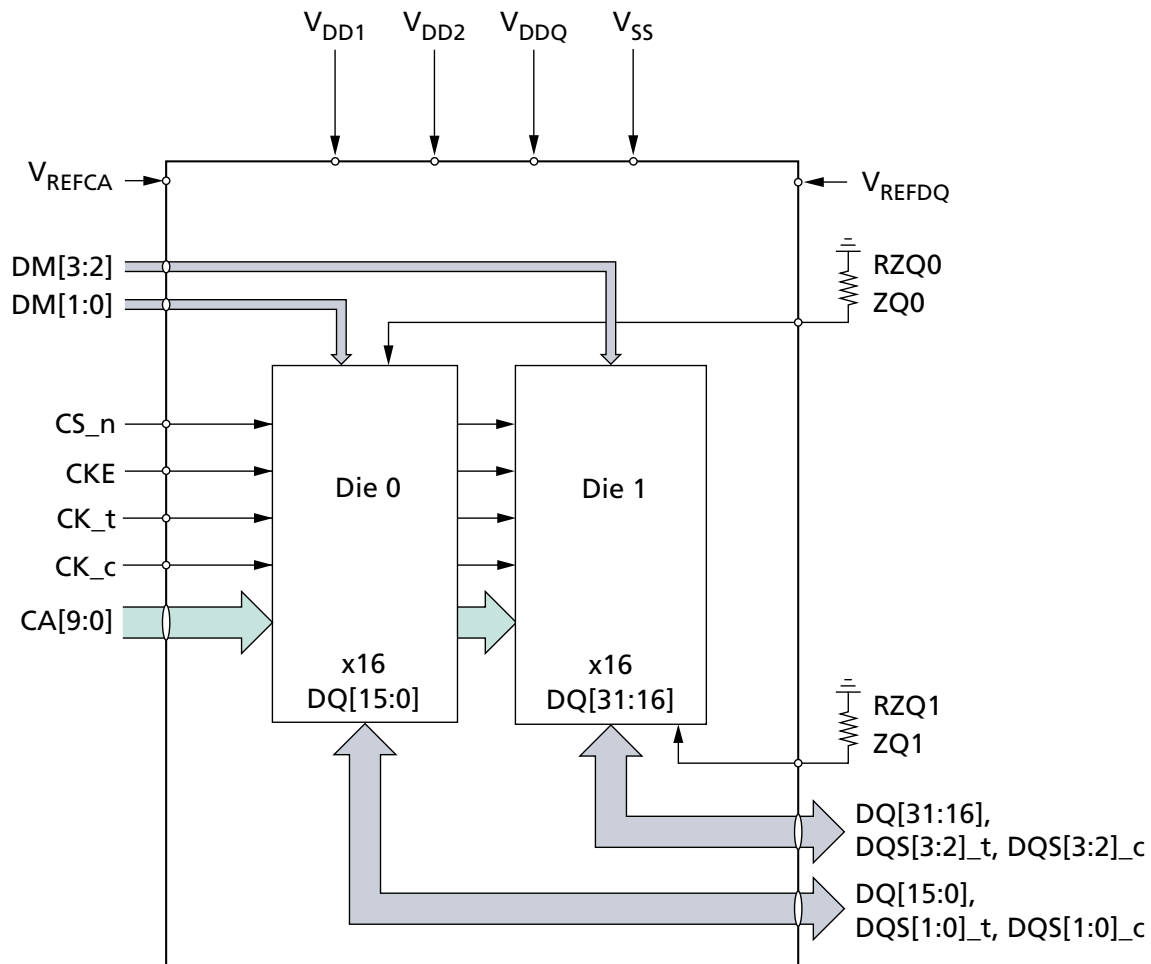
**Table 4: Ball/Pad Descriptions**

Symbol	Type	Description
CA[9:0]	Input	<b>Command/address inputs:</b> Provide the command and address inputs according to the command truth table.
CK_t, CK_c	Input	<b>Clock:</b> Differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock.
CKE	Input	<b>Clock enable:</b> CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled on the rising edge of CK.
CS_n	Input	<b>Chip select:</b> Considered part of the command code and is sampled on the rising edge of CK.
DM[3:0]	Input	<b>Input data mask:</b> Input mask signal for write data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[3:0] is DM for each of the four data bytes, respectively.
DQ[31:0]	I/O	<b>Data input/output:</b> Bidirectional data bus.
DQS[3:0]_t, DQS[3:0]_c	I/O	<b>Data strobe:</b> Bidirectional (used for read and write data) and complementary (DQS_t and DQS_c). It is edge-aligned output with read data and centered input with write data. DQS[3:0]_t/DQS[3:0]_c is DQS for each of the four data bytes, respectively.
V <sub>DDQ</sub>	Supply	<b>DQ power supply:</b> Isolated on the die for improved noise immunity.
V <sub>SSQ</sub>	Supply	<b>DQ ground:</b> Isolated on the die for improved noise immunity.
V <sub>DD1</sub>	Supply	<b>Core power:</b> Supply 1.
V <sub>DD2</sub>	Supply	<b>Core power:</b> Supply 2.
V <sub>SS</sub>	Supply	<b>Common ground.</b>
V <sub>REFCA</sub> , V <sub>REFDQ</sub>	Supply	<b>Reference voltage:</b> V <sub>REFCA</sub> is reference for command/address input buffers, V <sub>REFDQ</sub> is reference for DQ input buffers.
ZQ[1:0]	Reference	<b>External reference ball for output drive calibration:</b> This ball is tied to an external 240Ω resistor (RZQ), which is tied to V <sub>SSQ</sub> .
NU	–	<b>Not usable:</b> Do not connect.
NC	–	<b>No connect:</b> Not internally connected.
(NC)	–	<b>No connect:</b> Balls indicated as (NC) are no connects; however, they could be connected together internally.



## Package Block Diagrams

Figure 3: Single-Rank, Dual-Die, Single-Channel Package Block Diagram

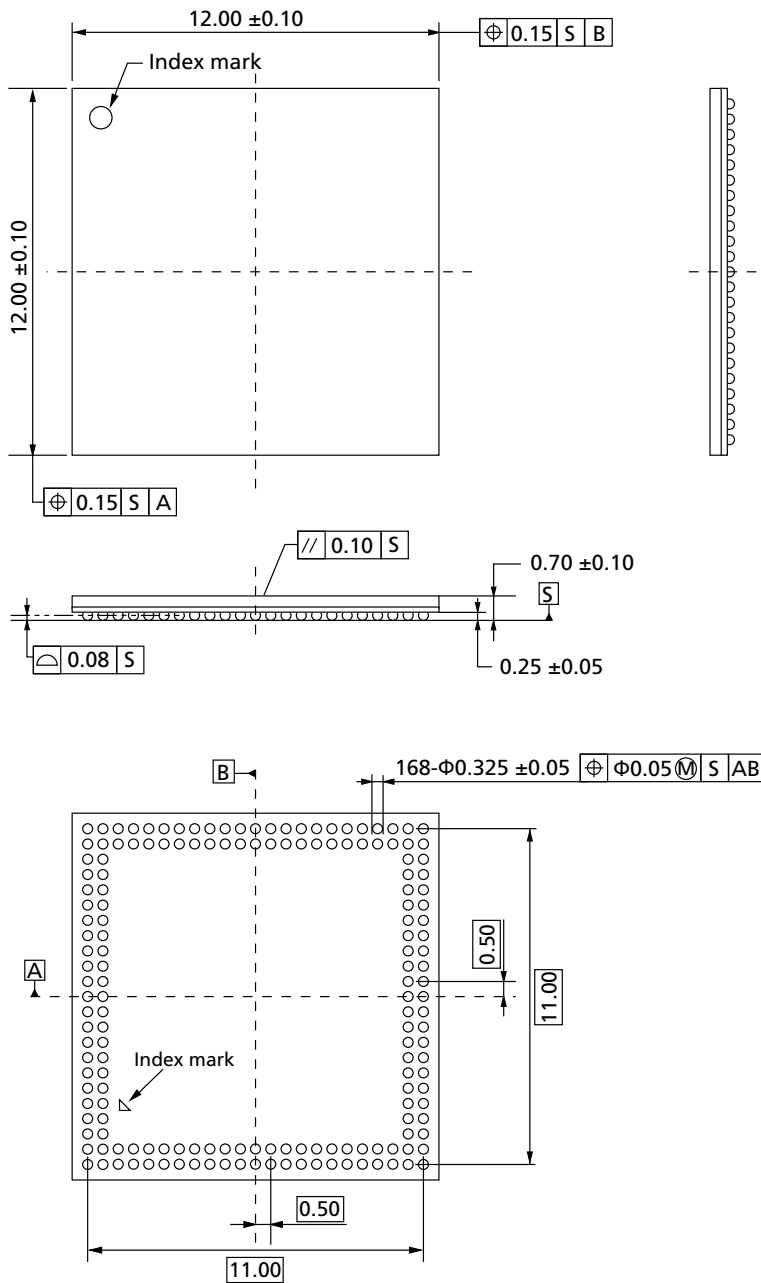




# 168-Ball LPDDR2 SDRAM Addendum Package Dimensions

## Package Dimensions

Figure 4: 168-Ball PoP FBGA (12mm x 12mm) – EDB8132B4PB-8D-F-D/R



- Notes: 1. Package drawing: ECA-TS2-0515-02.  
 2. All dimensions are in millimeters.



## Revision History

### Rev. B – 7/14

- Updated resistors in Package Block Diagram

### Rev. A – 4/14

- Initial release

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900  
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This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.