64Kx16 Static RAM CMOS, Module

The EDI8F1664C is a high speed 64Kx16 CMOS Static RAM Module. The module consists of four (4) 32Kx8 CMOS Static RAMs in plastic small outline packages, surface mounted onto an epoxy laminate (FR-4) substrate. The 32Kx8 RAMs are organized as two banks of 32Kx16 bits each. Functional equivalence to proposed monolithic megabit Static RAMs is achieved with an on-board decoder that interprets the higher order address (A15) to select one of the two banks as the x16 output, and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for Lower Byte (DQØ-DQ7) and Upper Byte (DQ8-DQ15) control, respectively.

EDI uses surface mount technology to produce high density modules which provide a cost effective solution for systems with minimal board spacing.

The EDI8F1664C is available with access times as fast as 100ns. All outputs and inputs are TTL-compatible and operate from a +5V supply. Fully asynchronous circuitry requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

Features

64Kx16 bit CMOS Static
Random Access Memory Module
- Access Times 100, 120, and 150ns
- Fully Static, No Clocks
- Inputs and Outputs Directly TTL Compatible

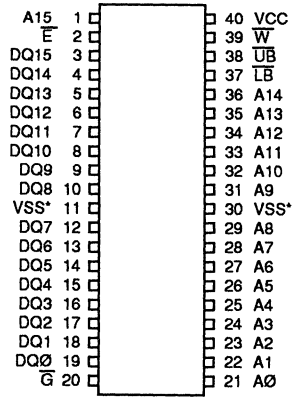
Jedec Approved Pinout
- 40 Pin Dual-in-line Package

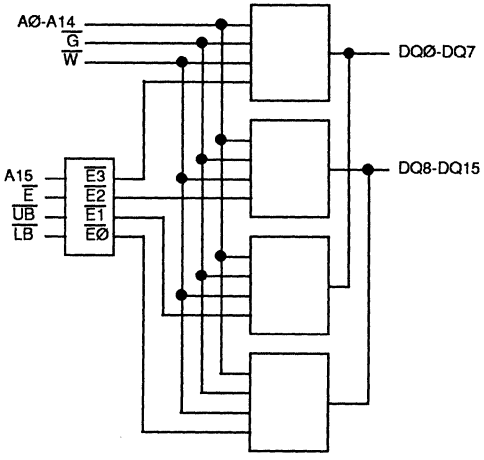
Single +5V (±10%) Supply Operation

Pin Names

AØ-A15	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ15	Data Input/Output
$\overline{UB}$	Upper Byte Control
$\overline{LB}$	Lower Byte Control
VCC	Power (+5V±10%)
VSS	Ground

Pin Configuration and Block Diagram





*Note: Both ground pins (VSS) need to be grounded for proper operations.

Absolute Maximum Ratings*

Voltage on any pin relative to VSS .....-0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial..... 0°C to +70°C.
Storage Temperature (Ambient/Ceramic).-65°C to +150°C
Power Dissipation.....4 Watts
Output Current..... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels..... VSS to 3.0V
Input Rise and Fall Times..... 5ns
Input and Output Timing Levels..... 1.5V
Output Load.: 1TTL, CL = 100pF
(Note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

(TA = 0°C to +70°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current, x16 mode	ICC1	$\overline{W}$, $\overline{E}$, $\overline{LB}$, $\overline{UB}$ = VIL, II/O = 0mA, Min Cycle	--	170	195	mA
Operating Power Supply Current, x8 mode	ICC1	$\overline{W}$, $\overline{E}$ = VIL; $\overline{LB}$ or $\overline{UB}$ =VIL; II/O = 0mA, Min Cycle	--	115	120	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH or $\overline{LB}$ & $\overline{UB}$ ≥ VIH	--	50	75	mA
Full Standby (CMOS) Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V or $\overline{LB}$ & $\overline{UB}$ ≥ VCC-0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V	--	1	3	mA
Input Leakage Current	IIL	VIN = 0V to VCC	--	--	10	µA
Output Leakage Current	IOL	V I/O = 0V to VCC	--	--	10	µA
Output High Voltage	VOH	IOH = -1.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL = 2.1mA	--	--	0.4	V

*Typical = TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{UB}$	$\overline{LB}$	$\overline{W}$	$\overline{G}$	Mode	Output	Power
H	X	H	X	X	Standby	HIGH Z	ICC2, ICC3
L	H	H	X	X	Standby	HIGH Z	ICC2, ICC3
L	X	X	H	H	Read, Output Deselect	HIGH Z	ICC1
L	L	H	L	X	UB Write	DIN(8-15)	ICC1
L	H	L	L	X	LB Write	DIN(0-7)	ICC1
L	L	L	L	X	Standby	DIN(0-15)	ICC1
L	L	H	H	L	Standby	DOUT(8-15)	ICC1
L	H	L	H	L	Standby	DOUT(0-7)	ICC1
L	L	L	H	L	Standby	DOUT(0-15)	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Pins	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	G,A	CI	50	pF
Capacitance Control (DQ Pins)	CD/Q	CD/Q	30	pF
Input Capacitance Control Lines	$\overline{E}$, $\overline{UB}$, $\overline{LB}$	CC	30	pF
Input Capacitance $\overline{W}$ Line	$\overline{W}$	CW	50	pF

These parameters are sampled, not 100% tested.

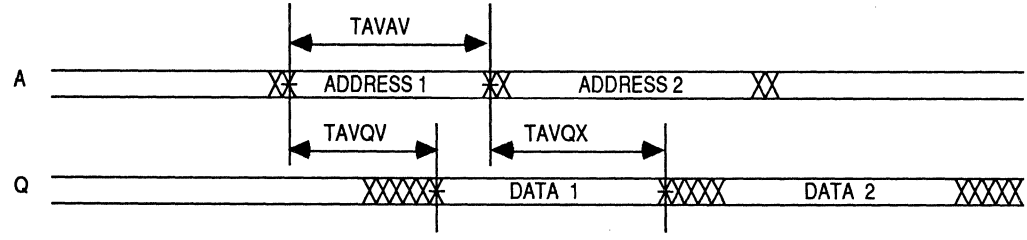
AC Characteristics
Read Cycle

(TA = 0°C to +70°C; VCC = 5.0V ±10%)

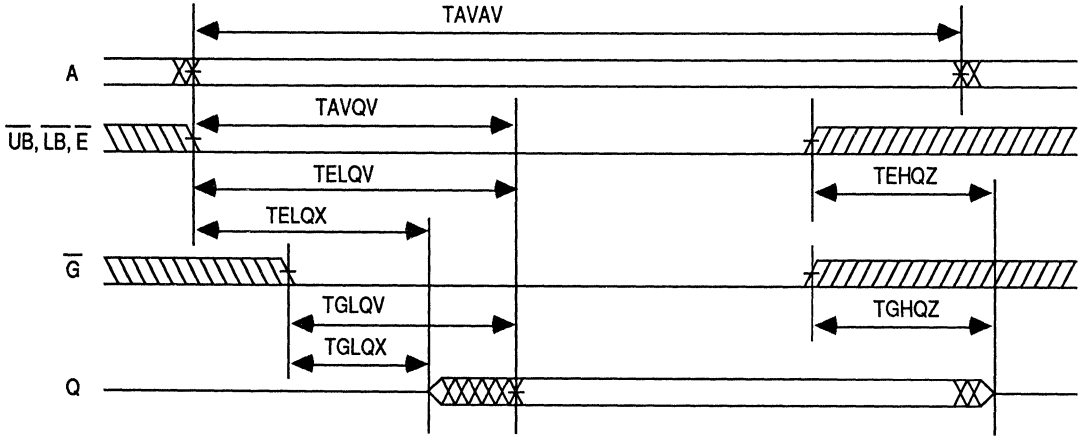
Parameter	Symbol		100ns		120ns		150ns		Units
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV		100		120		150		ns
Address Access Time	TAVQV			100		120		150	ns
Chip EnableAccess Time	TELQV	$\overline{E}$		100		120		150	ns
Chip Enable to Output in Low Z (1)	TELQX	$\overline{E}$	30		30		30		ns
Output Enable to Output Valid	TGLQV			50		60		70	ns
Output Enable to Output in Low Z (1)	TGLQX		10		10		10		ns
Chip Enable to Output in High Z (1)	TEHQZ	$\overline{E}$		30		40		50	ns
Output Enable to Output in High Z (1)	TGHQZ			30		40		50	ns
Output Hold from Address Change	TAVQX		10		10		10		ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
$\overline{W}$ High; $\overline{G}$, $\overline{E}$ Low



Read Cycle 2
$\overline{W}$ High

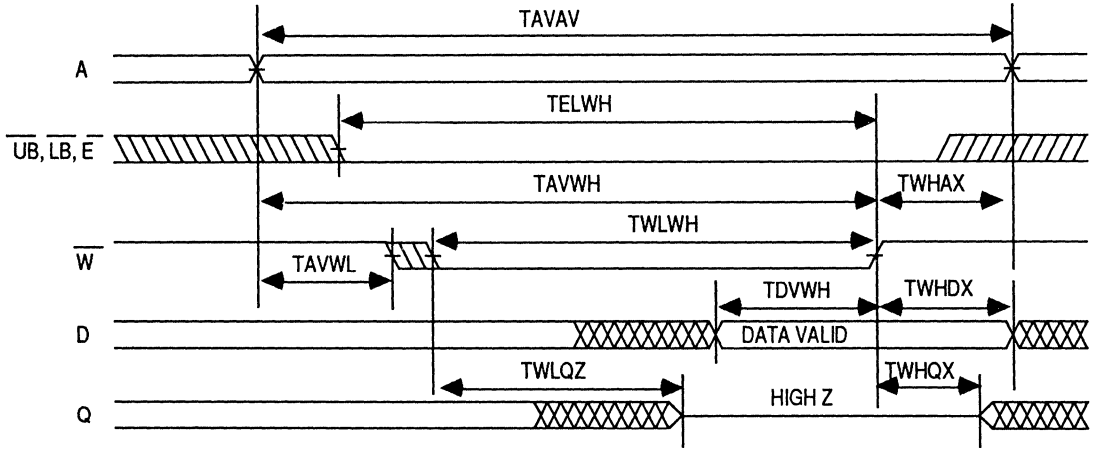


AC Characteristics
Write Cycle
(TA = 0°C to +70°C; VCC = 5.0V ±10%)

Parameter	Symbol			100ns		120ns		150ns		Units
				Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV			100		120		150		ns
Chip Enable to	TWLWH	$\overline{W}$		80		90		110		ns
End of Write	TWLEH	$\overline{E}$		80		90		110		ns
Address Setup Time	TAVWL	$\overline{W}$		20		20		20		ns
	TAVEL	$\overline{E}$		0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$		80		90		110		ns
End of Write	TAVEH	$\overline{E}$		80		90		110		ns
Write Pulse Width	TWLWH	$\overline{W}$		60		70		80		ns
	TELEH	$\overline{E}$		60		70		80		ns
Write Recovery Time	TWHAX	$\overline{W}$		0		0		0		ns
	TEHAX	$\overline{E}$		20		20		20		ns
Data Hold Time	TWHDX	$\overline{W}$		0		0		0		ns
	TEHDX	$\overline{E}$		20		20		20		ns
Write to Output in High Z (1)	TWLQZ			0	35	0	35		45	ns
Data to Write Time	TDVWH	$\overline{W}$		35		40		50		ns
	TDVEH	$\overline{E}$		35		40		50		ns
Output Active from End of Write (1)	TWHQX			0		0		0		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled