2 Megabyte Sync/Sync Burst, Small Outline DIMM

FEATURES

- 2x128Kx72 Synchronous, Synchronous Burst
- Flow-Through Architecture
- Sequential Burst MODE
- Clock Controlled Registered Bank Enables (E1#, E2#)
- Clock Controlled Byte Write Mode Enable (BWE#)
- Clock Controlled Byte Write Enables (BW1# - BW8#)
- Clock Controlled Registered Address
- Clock Controlled Registered Global Write (GW#)
- Aysnchronous Output Enable (G#)
- Internally self-timed Write
- Gold Lead Finish
- 3.3V ± 10% Operation
- Access Speed(s): TKHQV=8.5, 9, 10, 12ns
- Common Data I/O
- High Capacitance (30pf) drive, at rated Access Speed
- Single total array Clock
- Multiple Vcc and Gnd

DESCRIPTION

The EDI2AG272129VxxD1 is a Synchronous/ Synchronous Burst SRAM, 72 position SO DIMM (144 contacts) Module, organized as 2x128Kx72. The Module contains four (4) Synchronous Burst Ram Devices, packaged in the industry standard JEDEC 14mmx20mm TQFP placed on a Multilayer FR4 Substrate. The module architecture is defined as a Sync/Sycn Burst, Flow-Through, with support for sequential burst. This module provides High Performance, 2-1-1-1 accesses when used in Burst Mode, and used as a Synchronous Only Mode, provides a high performance cost advantage over BiCMOS aysnchronous device architectures.

Synchronous Only operations are performed via strapping ADSC# Low, and ADSP# / ADV# High, which provides for Ultra Fast Accesses in Read Mode while providing for internally self-timed Early Writes.

Synchronous/Synchronous Burst operations are in relation to an externally supplied clock, Registered Address, Registered Global Write, Registered Enables as well as an Asynchronous Output enable. This Module has been defined with full flexibility, which allows individual control of each of the eight bytes, as well as Quad Words in both Read and Write Operations.

*This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

PIN CONFIGURATION

PIN SYMBOLS

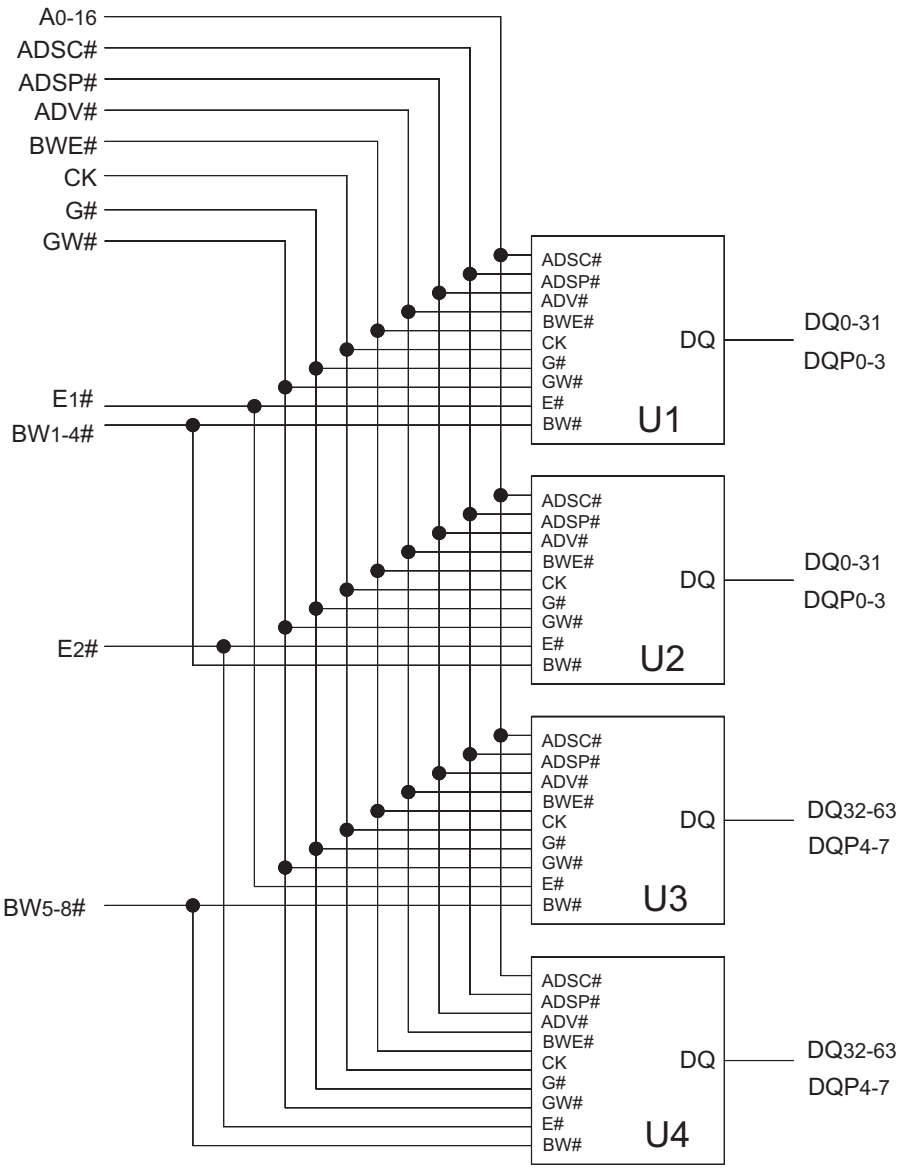
PIN	FUNCTION	PIN	FUNCTION
1	V_{SS}	37	DQ0
2	V_{SS}	38	DQ7
3	A0	39	DQ1
4	RFU	40	DQ6
5	A16	41	DQ2
6	A1	42	DQ5
7	A2	43	DQ3
8	A15	44	DQ4
9	A14	45	V_{SS}
10	A3	46	V_{SS}
11	A4	47	BW_2#
12	A13	48	DQP_1
13	A12	49	V_{CC}
14	A5	50	V_{CC}
15	A6	51	DQ8
16	A11	52	DQ15
17	A10	53	DQ9
18	A7	54	DQ14
19	A8	55	DQ10
20	A9	56	DQ13
21	V_{CC}	57	DQ11
22	V_{CC}	58	DQ12
23	G#	59	V_{SS}
24	RFU	60	V_{SS}
25	GW#	61	BW_3#
26	ADV#	62	DQP_2
27	ADSP#	63	V_{CC}
28	ADSC#	64	V_{CC}
29	E_1#	65	DQ16
30	CK	66	DQ23
31	E_2#	67	DQ17
32	BWE#	68	DQ22
33	BW_1#	69	DQ18
34	DQP0	70	DQ21
35	V_{CC}	71	DQ19
36	V_{CC}	72	DQ20

PIN	FUNCTION	PIN	FUNCTION
73	V_{SS}	109	DQ41
74	V_{SS}	110	DQ46
75	BW_4#	111	DQ42
76	DQP_3	112	DQ45
77	V_{CC}	113	DQ43
78	V_{CC}	114	DQ44
79	DQ24	115	V_{SS}
80	DQ31	116	V_{SS}
81	DQ25	117	BW_7#
82	DQ30	118	DQP_6
83	DQ26	119	V_{CC}
84	DQ29	120	V_{CC}
85	DQ27	121	DQ48
86	DQ28	122	DQ55
87	V_{SS}	123	DQ49
88	V_{SS}	124	DQ54
89	BW_5#	125	DQ50
90	DQP_4	126	DQ53
91	V_{CC}	127	DQ51
92	V_{CC}	128	DQ52
93	DQ32	129	V_{SS}
94	DQ39	130	V_{SS}
95	DQ33	131	BW_8#
96	DQ38	132	DQP_7
97	DQ34	133	V_{CC}
98	DQ37	134	V_{CC}
99	DQ35	135	DQ56
100	DQ36	136	DQ63
101	V_{SS}	137	DQ57
102	V_{SS}	138	DQ62
103	BW_6#	139	DQ58
104	DQP_5	140	DQ61
105	V_{CC}	141	DQ59
106	V_{CC}	142	DQ60
107	DQ40	143	V_{SS}
108	DQ47	144	V_{SS}

PIN NAMES

DQ0-DQ63	Input/Output Bus
DQP0-DQP7	Parity Bits
A0-A16	Address Bus
E1#, E2#	Synchronous Bank Enables
BWE#	Byte Write Mode Enable
BW1#-BW8#	Byte Write Enables
CK	Array Clock
GW#	Synchronous Global write Enable
G#	Asynchronous Output Enable
Vcc	3.3V Power Supply
Vss	Gnd

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

DIMM Pins	Symbol	Type	Description
3, 6, 7, 10, 11, 14 15, 18, 19, 20, 17 16, 13, 12, 9, 8, 5	A0-A16	Input Synchronous	Addresses: These inputs are registered and must meet the setup and hold times around the rising edge of CK. The burst counter generates internal addresses associated with A0 and A1, during burst and wait cycle.
33, 47, 61, 75, 89, 103, 117, 131	BW1#, BW2#, BW3#, BW4#, BW5#, BW6#, BW7#, BW8#	Input Synchronous	Byte Write: A byte write is LOW for a WRITE cycle and HIGH for a READ cycle. BW0# controls DQ0-7 and DQP0, BW1# controls DQ8-15 and DQP1. BW2# controls DQ16-23 and DQP2. BW3# controls DQ24-31 and DQP3. BW4# controls DQ32-39 and DQP4. BW5# controls DQ40-47 and DQP5. BW6#controls DQ48-55 and DQP6. BW7# controls DQ56-64 and DQP7.
32	BWE#	Input Synchronous	Write Enable: This active LOW input gates byte write operations and must meet the setup and hold times around the rising edge of CK.
25	GW#	Input Synchronous	Global Write: This active LOW input allows a full 72-bit WRITE to occur independent of the BWE# and BWx# lines and must meet the setup and hold times around the rising edge of CK.
30	CK	Input Synchronous	Clock: This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
29, 31	E1#, E2#	Input Synchronous	Bank Enables: These active LOW inputs are used to enable each individual bank and to gate ADSP#.
23	G#	Input	Output Enable: This active LOW asynchronous input enables the data output drivers.
26	ADV#	Input Synchronous	Address Status Processor: This active LOW input is used to control the internal burst counter. A HIGH on this pin generates wait cycle (no address advance)
27	ADSP#	Input Synchronous	Address Status Processor: This active LOW input, along with EL# and EH# being LOW, causes a new external address to be registered and a READ cycle is initiated using the new address.
28	ADSC#	Input Synchronous	Address Status Controller: This active LOW input causes device to be de-selected or selected along with new external address to be registered. A READ or WRITE cycle is initiated depending upon write control inputs.
Various	DQ0-63	Input/Output	Data Inputs/Outputs: First byte is DQ0-7, second byte is DQ8-15, third byte is DQ16-23, fourth byte is DQ24-31, fifth byte is DQ32-39, sixth byte is DQ40-47, seventh byte is DQ48-55 and the eight byte is DQ56-64.
38, 48, 62, 76, 90, 104, 118, 132	DQP0-7	Input/Output	Parity Inputs/Outputs: DQP0 is parity bit for DQ0-7. DQP1 is parity bit for DQ8-15. DQP2 is parity bit for DQ16-23. DQP3 is parity bit for DQ24-31. DQP4# is parity bit for DQ32-39. DQP5 is parity bit for DQ40-47. DQP6# is parity bit for DQ48-55. DQP7 is parity bit for DQ56-64 and DQP7. In order to use the device configured as a 128K x 64, the parity bits need to be tied to Vss through a 10K ohm resistor.
Various	Vcc	Supply	Core power supply: +3.3V -5%/ + 10%
Various	Vss	Ground	Ground

SYNCHRONOUS BURST - TRUTH TABLE

Operation	E1#	E2#	ADSP#	ADSC#	ADV#	GW#	G#	CK	DQ	Addr. Used
Deselected Cycle, Power Down; Bank 1	H	X	X	L	X	X	X	L-H	High-Z	None
Deselected Cycle, Power Down; Bank 2	X	H	X	L	X	X	X	L-H	High-Z	None
Read Cycle, Begin Burst; Bank 1	L	H	L	X	X	X	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 1	L	H	L	X	X	X	H	L-H	High-Z	External
Read Cycle, Begin Burst; Bank 2	H	L	L	X	X	X	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 2	H	L	L	X	X	X	H	L-H	High-Z	External
Write Cycle, Begin Burst; Bank 1	L	H	H	L	X	L	X	L-H	D	External
Write Cycle, Begin Burst; Bank 2	H	L	H	L	X	L	X	L-H	D	External
Read Cycle, Begin Burst; Bank 1	L	H	H	L	X	H	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 1	L	H	H	L	X	H	H	L-H	High-Z	External
Read Cycle, Begin Burst; Bank 2	H	L	H	L	X	H	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 2	H	L	H	L	X	H	H	L-H	High-Z	External
Read Cycle, Continue Burst; Bank 1	X	H	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 1	X	H	X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 2	H	X	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 2	H	X	X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 1	H	H	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 1	H	H	X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 2	H	H	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 2	H	H	X	H	L	H	H	L-H	High-Z	Next
Write Cycle, Continue Burst; Bank 1	X	H	H	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 1	H	H	X	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 2	H	X	H	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 2	H	H	X	H	L	L	X	L-H	D	Next
Read Cycle, Suspend Burst; Bank 1	X	H	H	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 1	X	H	H	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 2	H	X	H	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 2	H	X	H	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 1	H	H	X	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 1	H	H	X	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 2	H	H	X	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 2	H	H	X	H	H	H	H	L-H	High-Z	Current
Write Cycle, Suspend Burst; Bank 1	X	H	H	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 1	H	H	X	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 2	H	X	H	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 2	H	H	X	H	H	L	X	L-H	D	Current

SYNCHRONOUS ONLY - TRUTH TABLE

Operation	E1#	E2#	GW#	G#	ZZ	CK	DQ
Synchronous Write-Bank 1	L	H	L	H	L	↑	High-Z
Synchronous Read-Bank 1	L	H	H	L	L	↑	
Synchronous Write-Bank 2	H	L	L	H	L	↑	High-Z
Synchronous Read-Bank 2	H	L	H	L	L	↑	

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Relative to V_{SS}	-0.5V to +4.6V
V_{IN}	-0.5V to V_{CC} +0.5V
Storage Temperature	-55°C to +125°C
Operating Temperature (Commercial)	0°C to +70°C
Operating Temperature (Industrial)	-40°C to +85°C
Short Circuit Output Current	10 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V_{CC}	3.14	3.3	3.6	V
Supply Voltage	V_{SS}	0.0	0.0	0.0	V
Input High	V_{IH}	1.1	3.0	V_{CC}+0.3	V
Input Low	V_{IL}	-0.3	0.0	0.3	V
Input Leakage	I_{LI}	-2	1	2	µA
Output Leakage	I_{LO}	-2	1	2	µA

DC ELECTRICAL CHARACTERISTICS - READ CYCLE

Description	SYM	Typ	Max				Units
			8.5	9	10	12	
Power Supply Current	Icc1	1.6	2.2	2.1	2.1	2.0	A
Power Supply Current Device Selected, No Operation	Icc	750	1.5	1.5	1.0	1.0	A
CMOS Standby	Icc3	250	300	300	300	300	mA
Clock Running-Deselect	IccK	600	1000	1000	750	750	mA

AC TEST CONDITIONS

Input Pulse Levels	V_{SS} to 3.0V
Input and Output Timing Ref.	1.25V
Output Test equivalencies	

AC TEST LOAD

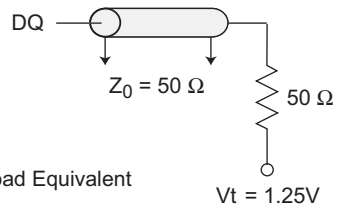


Fig. 1
Output Load Equivalent

BURST ADDRESS TABLE (MODE=NC/VCC)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A-A00	A-A01	A-A10	A-A11
A-A01	A-A00	A-A11	A-A10
A-A10	A-A11	A-A00	A-A01
A-A11	A-A10	A-A01	A-A00

BURST ADDRESS TABLE (MODE=GND)

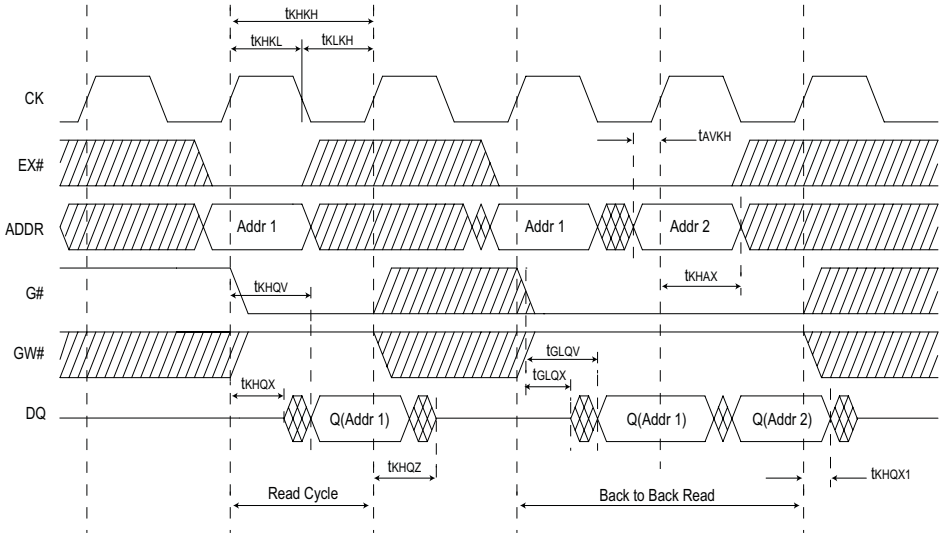
First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A-A00	A-A01	A-A10	A-A11
A-A01	A-A10	A-A11	A-A00
A-A10	A-A11	A-A00	A-A01
A-A11	A-A00	A-A01	A-A10

READ CYCLE TIMING PARAMETERS

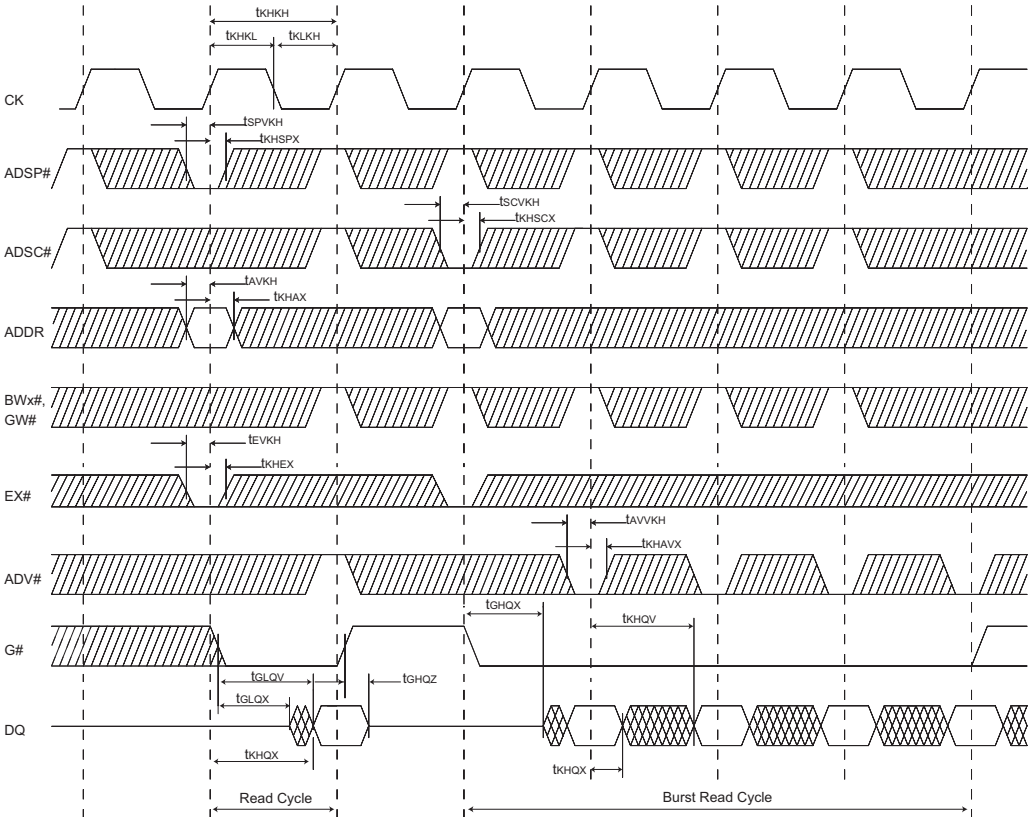
		8.5ns		9ns		10ns		12ns		
Description	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Clock Cycle Time	t_{KHKH}	*	*	10		12		15		ns
Clock High Time	t_{KHKL}	*	*	4		5		5		ns
Clock Low Time	t_{KLKH}	*	*	4		5		5		ns
Clock to Output Valid	t_{KHQV}	*	*		9		10		12	ns
Clock to Output Invalid	t_{KHQX1}	*	*	3		3		3		ns
Clock to Output Low-Z	t_{KHQX}	*	*	2		2		2		ns
Output Enable to Output Valid	t_{GLQV}	*	*		4		4		5	ns
Output Enable to Output Low-Z	t_{GLQX}	*	*	0		0		0		ns
Output Enable to Output High-Z	t_{GHQZ}	*	*		4		4		5	ns
Address Setup	t_{AVKH}	*	*	2.5		2.5		2.5		ns
Bank Enable Setup	t_{EVKH}	*	*	2.5		2.5		2.5		ns
Address Hold	t_{KHAX}	*	*	1.0		1.0		1.0		ns
Bank Enable Hold	t_{KHEX}	*	*	1.0		1.0		1.0		ns

**TBD*

SYNCHRONOUS ONLY READ CYCLE



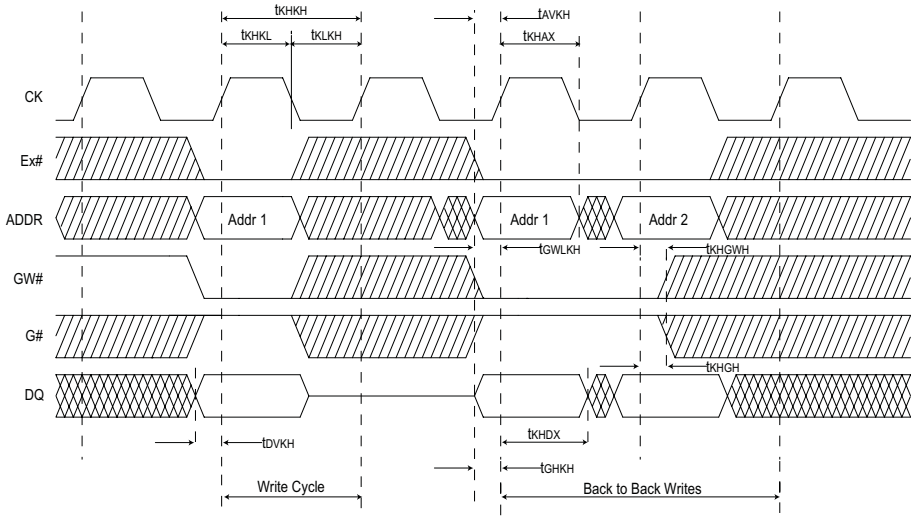
SYNC-BURST READ CYCLE



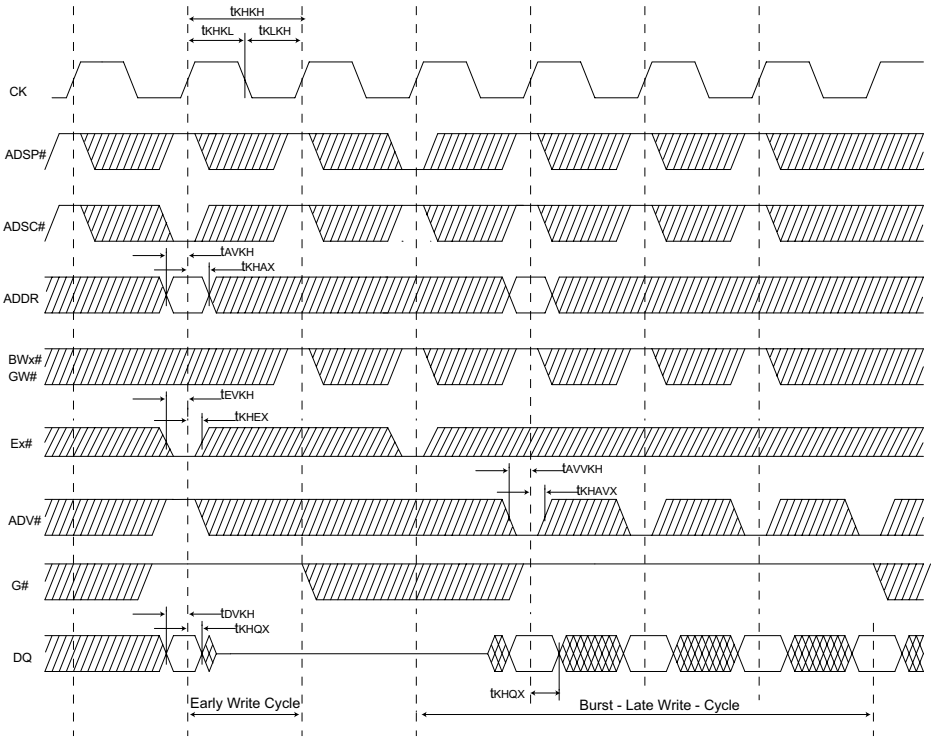
WRITE CYCLE TIMING PARAMETERS

Description	Sym	8.5ns Min	8.5ns Max	9ns Min	9ns Max	10ns Min	10ns Max	12ns Min	12ns Max	Units
Clock Cycle Time	t_{KHKH}			10		12		15		ns
Clock High Time	t_{KHKL}			4		5		5		ns
Clock Low Time	t_{KLKH}			4		5		5		ns
Address Setup	t_{AVKH}			2.5		2.5		2.5		ns
Address Hold	t_{KHAX}			1.0		1.0		1.0		ns
Bank Enable Setup	t_{EVKH}			2.5		2.5		2.5		ns
Bank Enable Hold	t_{KHEX}			1.0		1.0		1.0		ns
Global Write Enable Setup	t_{WVKH}			2.5		2.5		2.5		ns
Global Write Enable Hold	t_{KHWX}			1.0		1.0		1.0		ns
Data Setup	t_{DVKH}			2.5		2.5		2.5		ns
Data Hold	t_{KHDX}			1.0		1.0		1.0		ns

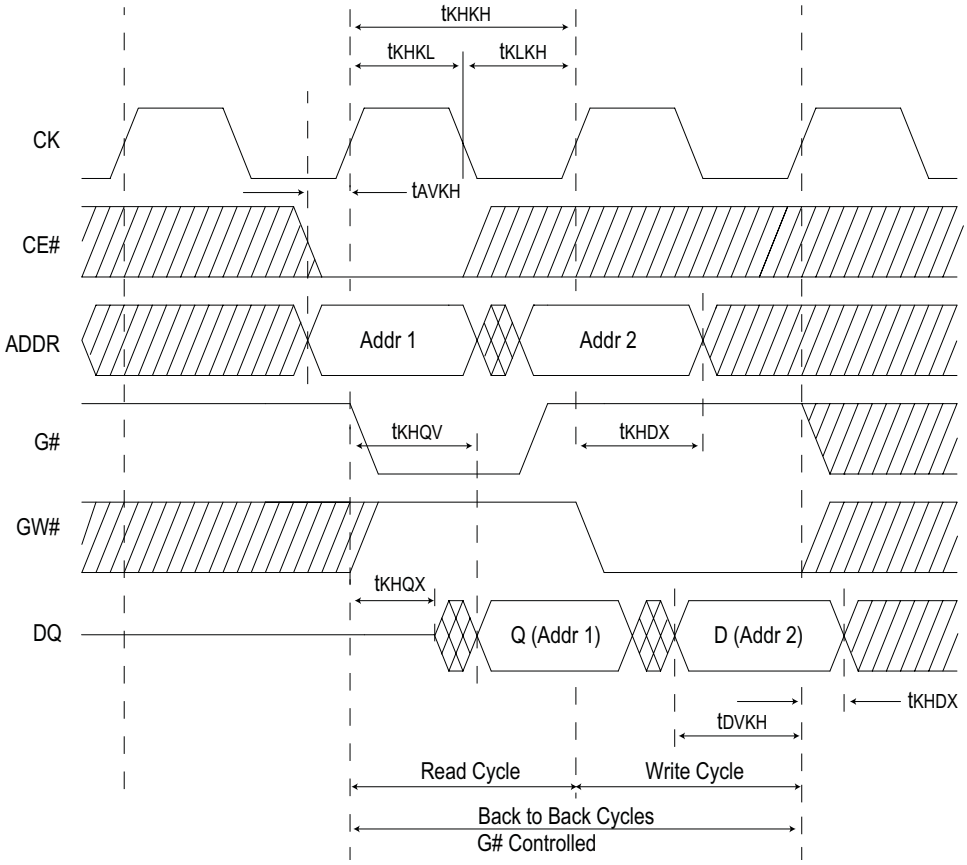
SYNC (NON-BURST) WRITE CYCLE



SYNCBURST WRITE CYCLE



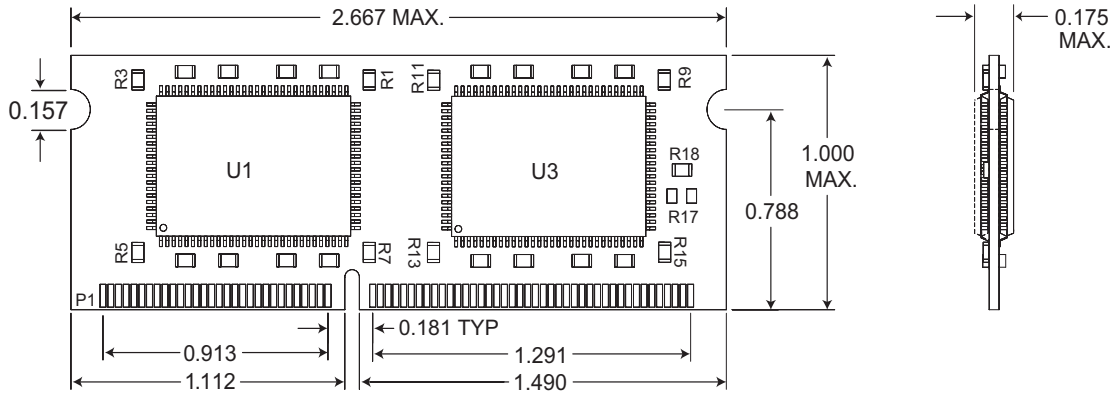
SYNC (NON-BURST) READ/WRITE CYCLE



PACKAGE DESCRIPTION

Package No. 409

144 Lead
SO DIMM



ORDERING INFORMATION

Part Number	Organization	Voltage	Speed (ns)	Package
EDI2AG272129V85D1*	2x128Kx72	3.3	8.5	144 SO-DIMM
EDI2AG272129V9D1*	2x128Kx72	3.3	9	144 SO-DIMM
EDI2AG272129V10D1	2x128Kx72	3.3	10	144 SO-DIMM
EDI2AG272129V12D1	2x128Kx72	3.3	12	144 SO-DIMM

**Consult Factory for Availability*