256Kx1 Static RAM CMOS, High Speed Monolithic

The EDI81256C/P is a 262,144 bit high performance, low power CMOS Static RAM organized as 256Kx1. It is available in Standard (C) and Low Power (P) versions.

Fully asynchronous, the EDI81256C/P requires no clocks or refreshing for operation.

All inputs and outputs are TTL compatible and operate from a single 5 volt supply.

Military product is available 100% screened to MIL-STD-883C, Class B.

Features

256Kx1 bit CMOS Static Random Access Memory

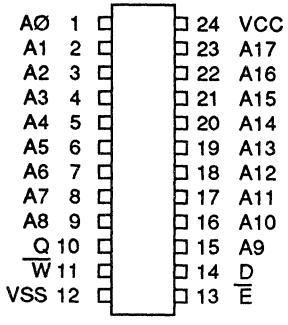
- Access Times 35, 45, and 55ns
- Fully Static, No Clocks
- Inputs and Outputs Directly TTL Compatible
- Data Retention Function on EDI81256P

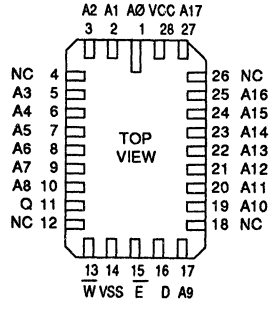
Jedec Approved Pinouts

- 24 Pin Ceramic DIP (Q)
- 28 Pin Ceramic LCC (L)

Single +5V (±10%) Supply Operation

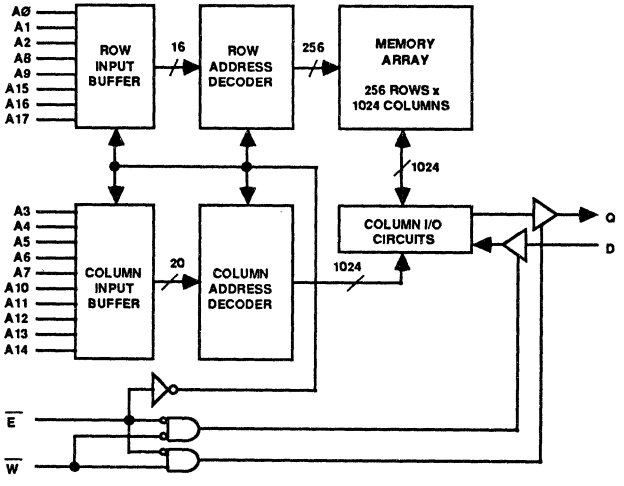
Pin Configuration and Block Diagram





Pin Names

AØ-A17	Address Inputs
E	Chip Enable
W	Write Enable
D	Data Input
Q	Data Output
VCC	Power (+5V±10%)
VSS	Ground



Absolute Maximum Ratings*

Voltage on any pin relative to VSS .....-0.5V to 7.0V
Operating Temperature TA (Ambient)
Industrial.....-40°C to +85°C
Military..... -55°C to +125°C
Storage Temperature (Ambient/Ceramic). -65°C to +150°C
Power Dissipation..... 1 Watt
Output Current..... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels..... VSS to 3.0V
Input Rise and Fall Times..... 5ns
Input and Output Timing Levels..... 1.5V
Output Load.....1TTL, CL = 30pF
(note: For TEHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions		Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	C	--	80	120	mA
			P	--	80	100	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$≥ VIH, VIN ≤ VIL or VIN ≥ VIH		--	2	25	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$≥ VCC-0.2V	C	--	1	10	mA
		VIN ≥VCC-0.2V or VIN≤0.2V	P	--	0.5	3	mA
Input Leakage Current	IIL	VIN = 0V to VCC		--	--	±5	µA
Output Leakage Current	IOL	V I/O = 0V to VCC		--	--	±5	µA
Output High Voltage	VOH	IOH= -4.0mA		2.4	--	--	V
Output Low Voltage	VOL	IOL= 8.0mA		--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

E	W	Mode	Output	Power
$\overline{H}$	$\overline{X}$	Standby	HIGH Z	ICC2, ICC3
L	H	Read	DOUT	ICC1
L	L	Write	HIGH Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max		Unit
		LCC	DIP	
Input Capacitance (Except DQ Pins)	CI	6	10	pF
Capacitance Control (DQ Pins)	CD/Q	8	12	pF

These parameters are sampled, not 100% tested.

AC Characteristics

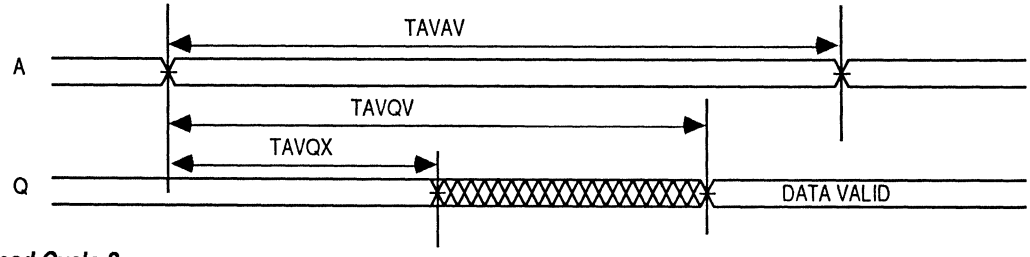
Read Cycle

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

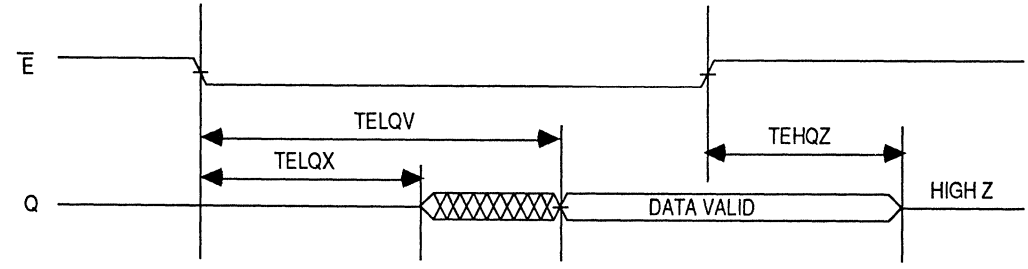
Parameter	Symbol	35ns		45ns		55ns		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	35		45		55		ns
Address Access Time	TAVQV		35		45		55	ns
Chip Enable Access Time	TELQV		35		45		55	ns
Chip Enable to Output in Low Z (1)	TELQX	5		5		5		ns
Chip Enable to Output in High Z (1)	TEHQZ	0	20	0	20	0	20	ns
Output Hold from Address Change	TAVQX	5		5		5		ns
Chip Enable to Power Up (1)	TPU	0		0		0		ns
Chip Disable to Power Down (1)	TPD		35		45		55	ns

Note 1: Parameter guaranteed, but not tested.

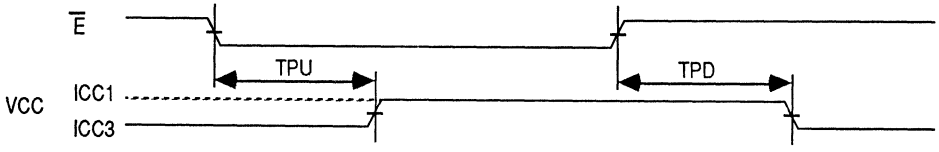
Read Cycle 1
$\overline{W}$ High (continuously selected, $\overline{E}$ Low)



Read Cycle 2
$\overline{E}$ Low, $\overline{W}$ High



$\overline{E}$ Power Down Function



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AC Characteristics

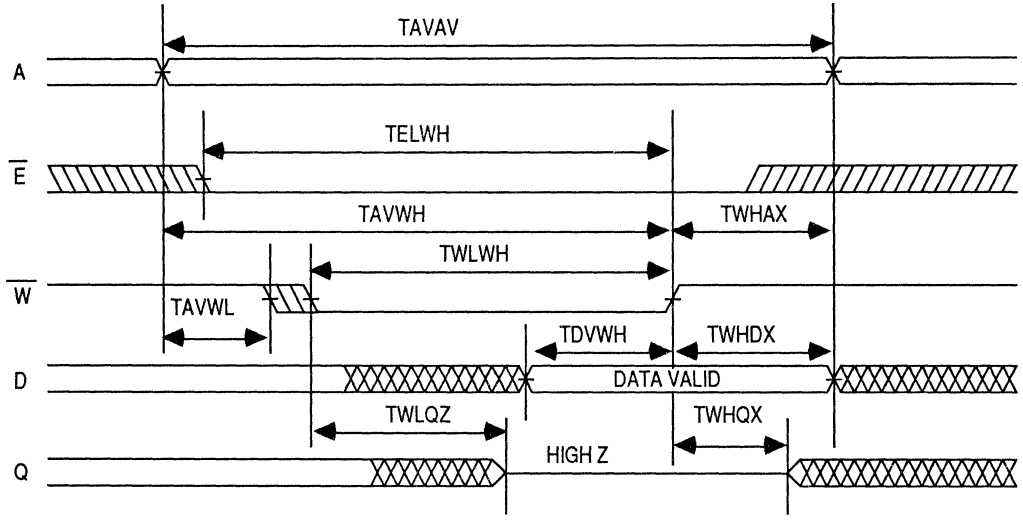
Write Cycle

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

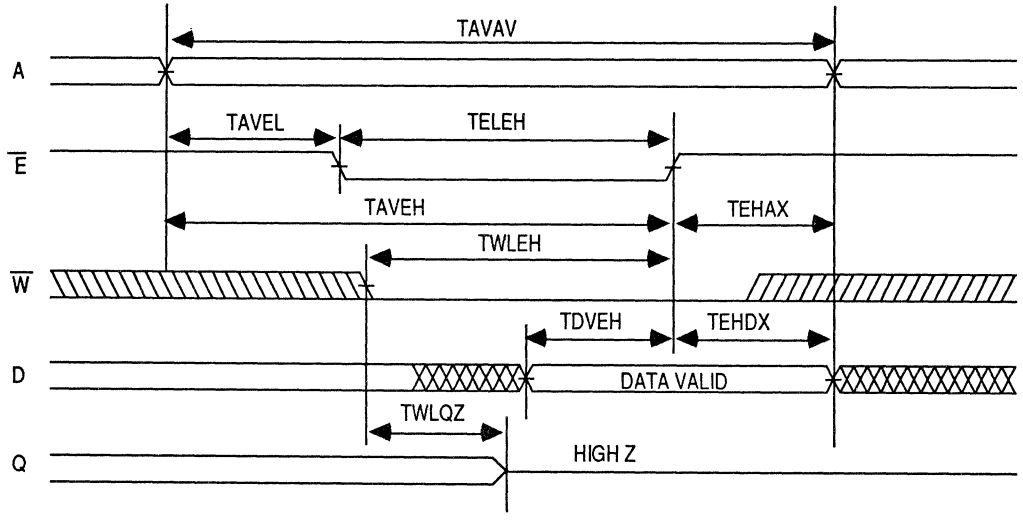
Parameter	Symbol		35ns		45ns		55ns		Units
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		35		45		55		ns
Chip Enable to	TELWH	$\overline{W}$	30		35		40		ns
End of Write	TWLEH	$\overline{E}$	30		35		40		ns
Address Setup Time	TAVWL	$\overline{W}$	0		0		0		ns
	TAVEL	$\overline{E}$	0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$	30		35		40		ns
End of Write	TAVEH	$\overline{E}$	30		35		40		ns
Write Pulse Width	TWLWH	$\overline{W}$	25		25		30		ns
	TELEH	$\overline{E}$	25		25		30		ns
Write Recovery Time	TWHAX	$\overline{W}$	5		5		5		ns
	TEHAX	$\overline{E}$	5		5		5		ns
Data Hold Time	TWHDX	$\overline{W}$	0		0		0		ns
	TEHDX	$\overline{E}$	0		0		0		ns
Write to Output in High Z (1)	TWLQZ		0	15	0	15	0	20	ns
Data to Write Time	TDVWH	$\overline{W}$	20		25		25		ns
	TDVEH	$\overline{E}$	20		25		25		ns
Output Active from End of Write (1)	TWHQX		0		0		0		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled



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Data Retention Characteristics — *Low Power (EDI81256P Version Only)*

(TA =-55°C to +125°C)

Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E}$≥ VDD -0.2V	--	50	500	µA
Chip Disable to Data Retention Time	TCDR	VIN ≥VDD -0.2V	0	--	--	ns
Operation Recovery Time	TR	or VIN ≤0.2V	TAVAV*	--	--	ns

*Read Cycle Time

Data Retention
$\overline{E}$ Controlled