



256Kx16 MONOLITHIC SRAM, SMD 5962-96795

FEATURES

- 256Kx16 bit CMOS Static
- Random Access Memory
 - Access Times of 17, 20, 25, 35ns
 - Data Retention Function (LPA version)
 - TTL Compatible Inputs and Outputs
 - Fully Static, No Clocks
- 44 lead JEDEC Approved Revolutionary Pinout
 - Ceramic SOJ (Package 322)
 - Ceramic Flatpack (Package 323)
- Single +5V ($\pm 10\%$) Supply Operation

The EDI816256CA is a 4 megabit Monolithic CMOS Static RAM.

The EDI816256CA uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device allows upper and lower byte access by use of the data byte control pins (LB#, UB#).

The devices are available in a fully hermetic 44 lead ceramic SOJ and a 44 lead Ceramic Flatpack. The Ceramic SOJ is pin for pin compatible with the commercially available plastic SOJ. This allows the user the luxury of designing a board that can be used for both the commercial and military market.

A Low Power version with Data Retention (EDI816256LPA) is also available for battery backed applications. Military product is available compliant to Appendix A of MIL-PRF-38535.

PIN CONFIGURATION TOP VIEW

A0	1	44	A17
A1	2	43	A16
A2	3	42	A15
A3	4	41	OE#
A4	5	40	UB#
CS#	6	39	LB#
I/O1	7	38	I/O16
I/O2	8	37	I/O15
I/O3	9	36	I/O14
I/O4	10	35	I/O13
Vcc	11	34	Vss
Vss	12	33	Vcc
I/O5	13	32	I/O12
I/O6	14	31	I/O11
I/O7	15	30	I/O10
I/O8	16	29	I/O9
WE#	17	28	NC
A5	18	27	A14
A6	19	26	A13
A7	20	25	A12
A8	21	24	A11
A9	22	23	A10

PIN DESCRIPTION

A0-17	Address Inputs
LB# (I/O1-8)	Lower-Byte Control (I/O1-8)
UB# (I/O9-16)	Upper-Byte Control (I/O9-16)
I/O1-16	Data Input/Output
CS#	Chip Select
OE#	Output Enable
WE#	Write Enable
Vcc	+5.0V Power
Vss	Ground
NC	No Connection



ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on any pin relative to Vss	-0.5 to 7.0	V
Operating Temperature T _A (Ambient)		
Commercial	0 to +70	°C
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Plastic	-65 to +125	°C
Power Dissipation	1.5	W
Output Current	20	mA
Junction Temperature, T _J	175	°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Condition	Max	Unit
Address Lines	CI	V _{IN} = V _{CC} or V _{SS} , f = 1.0MHz	12	pF
Data Lines	CD/Q	V _{IN} = V _{CC} or V _{SS} , f = 1.0MHz	14	pF

These parameters are sampled, not 100% tested.

TRUTH TABLE

CS#	WE#	OE#	LB#	UB#	Mode	Data I/O		Supply Current
						I/O ₁₋₈	I/O ₉₋₁₆	
H	X	X	X	X	Not Select	High Z	High Z	I _{CC2} , I _{CC3}
L	H	H	X	X	Output Disable			
L	X	X	H	H				
L	H	L	L	H	Read	Data Out	High Z	I _{CC1}
			H	L		High Z	Data Out	
			L	L		Data Out	Data Out	
L	L	X	L	H	Write	Data In	High Z	I _{CC1}
			H	L		High Z	Data In	
			L	L		Data In	Data In	

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Supply Voltage	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.2	—	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

DC CHARACTERISTICS

V_{CC} = 5V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions		Min	Max	Units
Input Leakage Current	I _{LI}	V _{IN} = 0V to V _{CC}			10	μA
Output Leakage Current	I _{LO}	V _{I/O} = 0V to V _{CC}			10	μA
Operating Power Supply Current	I _{CC1}	WE#, CS# = V _{IL} , I _{I/O} = 0mA, Min Cycle			300	mA
Standby (TTL) Power Supply Current	I _{CC2}	CS# ≥ V _{IH} , V _{IN} ≤ V _{IL} , V _{IN} ≥ V _{IH}			60	mA
Full Standby Power Supply Current	I _{CC3}	CS# ≥ V _{CC} -0.2V	CA	—	25	mA
		V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V	LPA	—	16	mA
Output Low Voltage	V _{OL}	I _{OL} = 6.0mA			0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA		2.4		V

NOTE: DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

AC TEST CONDITIONS

Figure 1

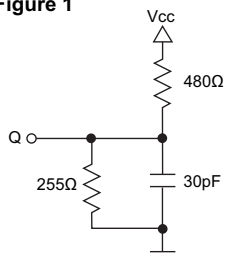
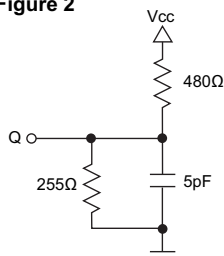


Figure 2



Input Pulse Levels	V _{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For t_{EHQZ}, t_{GHQZ} and t_{WLQZ}, C_L = 5pF (Figure 2)



AC CHARACTERISTICS – READ CYCLE

$V_{CC} = 5V$, $V_{SS} = 0V$, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol		17ns		20ns		25ns		35ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	17		20		25		35		ns
Address Access Time	t_{AVQV}	t_{AA}		17		20		25		35	ns
Chip Enable Access Time	t_{ELQV}	t_{ACS}		17		20		25		35	ns
Chip Enable to Output in Low Z (1)	t_{ELQX}	t_{CLZ}	2		5		5		5		ns
Chip Disable to Output in High Z (1)	t_{EHQZ}	t_{CHZ}	0	7	0	7	0	8	0	10	ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	0		0		0		0		ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		10		10		12		15	ns
Output Enable to Output in Low Z (1)	t_{GLQX}	t_{OLZ}	0		0		0		0		ns
Output Disable to Output in High Z(1)	t_{GHQZ}	t_{OHZ}	0	7	0	7	0	8	0	10	ns
LB#, UB# Access Time	t_{UBLQV} t_{LBLQV}	t_{BA}		10		10		12		15	ns
LB#, UB# Enable to Low Z Output	t_{UBLQX} t_{LBLQX}	t_{BLZ}	0	0		0		0		0	ns
LB#, UB# Disable to High Z Output	t_{UBHQZ} t_{LBHQZ}	t_{BHZ}	0	7	0	7	0	8	0	10	ns

NOTE:

1. This parameter is guaranteed by design but not tested.

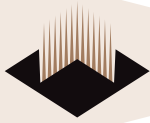
AC CHARACTERISTICS – WRITE CYCLE

$V_{CC} = 5V$, $V_{SS} = 0V$, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$

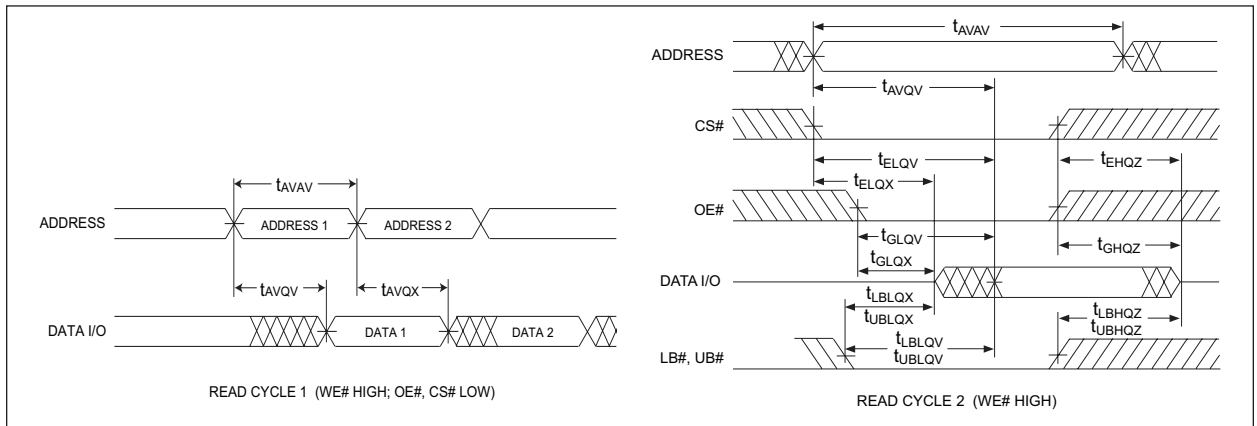
Parameter	Symbol		17ns		20ns		25ns		35ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	17		20		25		35		ns
Chip Enable to End of Write	t_{ELWH}	t_{CW}	14		15		17		20		ns
	t_{ELEH}	t_{CW}	14		15		17		20		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		0		ns
	t_{AVEL}	t_{AS}	0		0		0		0		ns
	t_{AVUBL}	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AVWH}	t_{AW}	14		15		17		20		ns
	t_{AVEH}	t_{AW}	14		15		17		20		ns
	t_{AVUBH}	t_{AW}	14		15		17		20		ns
Write Pulse Width	t_{WLWH}	t_{WP}	14		14		15		17		ns
	t_{WLEH}	t_{WP}	14		14		15		17		ns
Write Recovery Time	t_{WHAX}	t_{WR}	0		0		0		0		ns
	t_{EHAX}	t_{WR}	0		0		0		0		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		0		ns
	t_{EHDX}	t_{DH}	0		0		0		0		ns
Write to Output in High Z (1)	t_{WLQZ}	t_{WHZ}	0	8	0	8	0	8	0	10	ns
Data to Write Time	t_{DVWH}	t_{DW}	10		10		12		15		ns
	t_{DVEH}	t_{DW}	10		10		12		15		ns
Output Active from End of Write (1)	t_{WHQX}	t_{WLZ}	0		0		0		0		ns
LB, UB Valid to End of Write	t_{LBLEH} t_{UBLUBH}	t_{BW}	14		16		18		20		ns

NOTE:

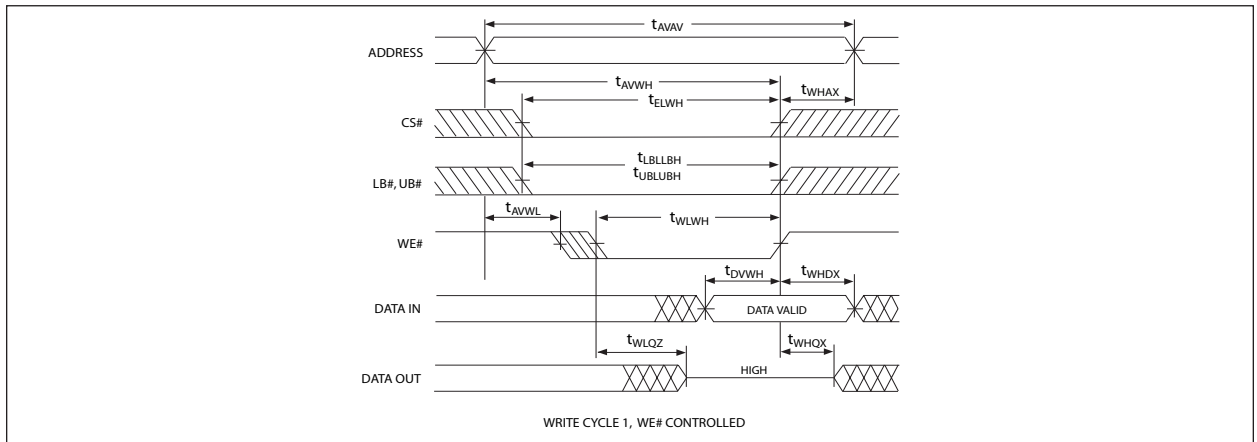
1. This parameter is guaranteed by design but not tested.



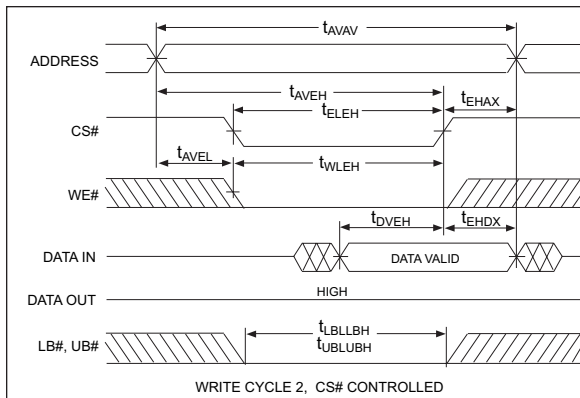
TIMING WAVEFORM – READ CYCLE



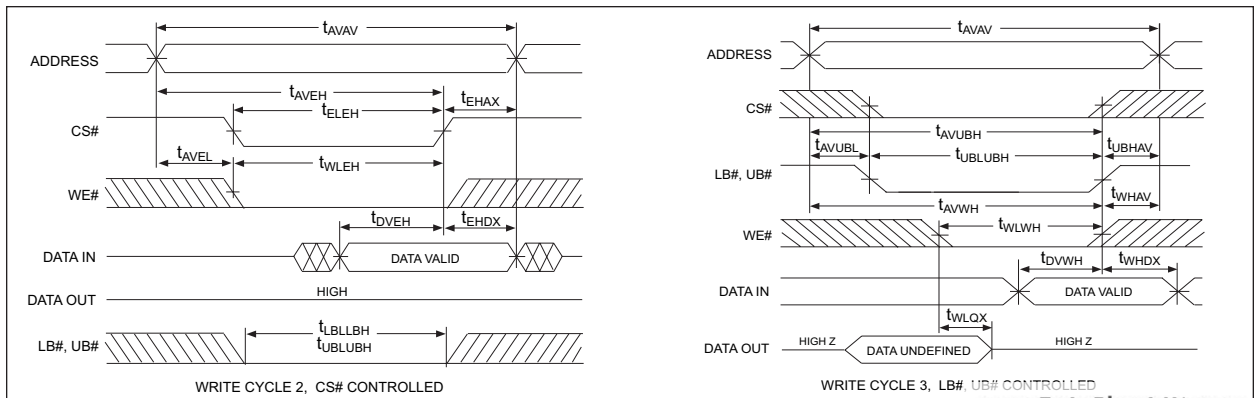
WRITE CYCLE – WE# CONTROLLED



WRITE CYCLE - CS# CONTROLLED



WRITE CYCLE - LB#, UB# CONTROLLED





DATA RETENTION CHARACTERISTICS (EDI816256LPA ONLY)

 $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$

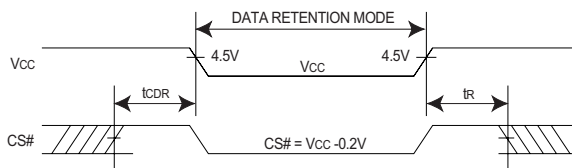
Characteristic Low Power Version only	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage	V_{CC}	$V_{CC} = 2.0\text{V}$	2	—	—	V
Data Retention Quiescent Current	I_{CCDR}	$CS\# \geq V_{CC} - 0.2\text{V}$	—	—	2.2	mA
Chip Disable to Data Retention Time (1)	T_{CDR}	$V_{IN} \geq V_{CC} - 0.2\text{V}$	0	—	—	ns
Operation Recovery Time (1)	T_R	or $V_{IN} \leq 0.2\text{V}$	T_{AVAV}	—	—	ns

NOTE:

1. This parameter is guaranteed by design but not tested.

* Read Cycle Time

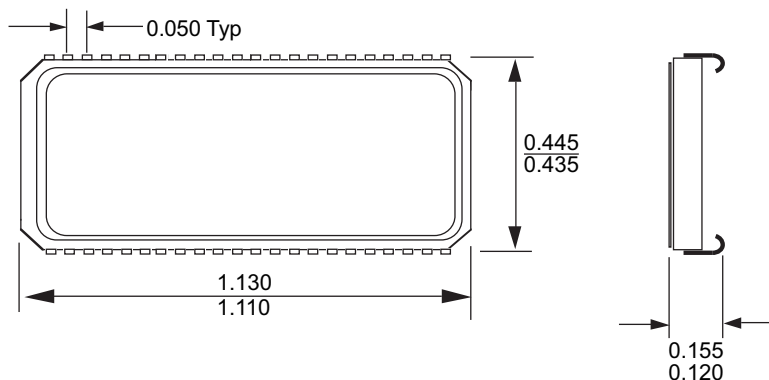
DATA RETENTION – CS# CONTROLLED



DATA RETENTION, CS# CONTROLLED

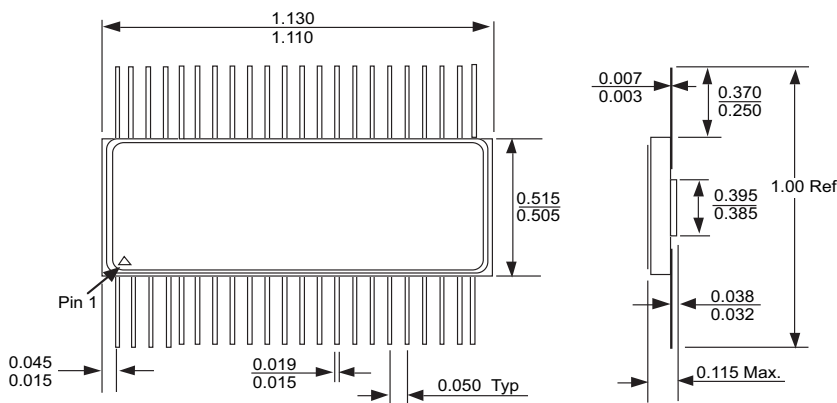


PACKAGE 322: 44 LEAD, CERAMIC SOJ



DIMENSIONS ARE IN INCHES

PACKAGE 323: 44 PIN, CERAMIC FLATPACK



DIMENSIONS ARE IN INCHES



ORDERING INFORMATION

EDI 8 16256 CA X X X

WHITE ELECTRONIC DESIGNS _____

SRAM _____

ORGANIZATION, 256Kx16 _____

TECHNOLOGY: _____

CA = CMOS Standard Power

LPA = Low Power

ACCESS TIME (ns) _____

PACKAGE TYPE: _____

F44 = 44 pin Ceramic Flatpack (Package 323)

N44 = 44 lead Ceramic SOJ (Package 322)

DEVICE GRADE: _____

B = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C