

64Kx4 Static RAM CMOS, High Speed Monolithic

The EDI8465C/P is a high performance CMOS Static RAM organized as 64Kx4 and available in both standard power (C) and low power (P) versions. Inputs and outputs are TTL compatible and allow for direct interfacing with common system bus architecture.

The EDI8465C/P is packaged in a 300 mil wide, 24 pin DIP, which provides excellent board level packing densities.

Military product is available 100% screened to MIL-STD-883C, Class B.

Features

64Kx4 bit CMOS Static

Random Access Memory

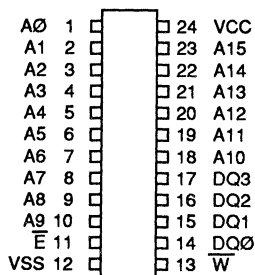
- Access Times 35, 45, and 55ns
- Fully Static, No Clocks
- Data Retention Function on EDI8465P
- Battery Back-up Capability
- TTL Compatible I/O

Jedec Approved Pinout

- 24 Pin Ceramic DIP, 300 mils wide (Q)
- Common Data Inputs and Outputs

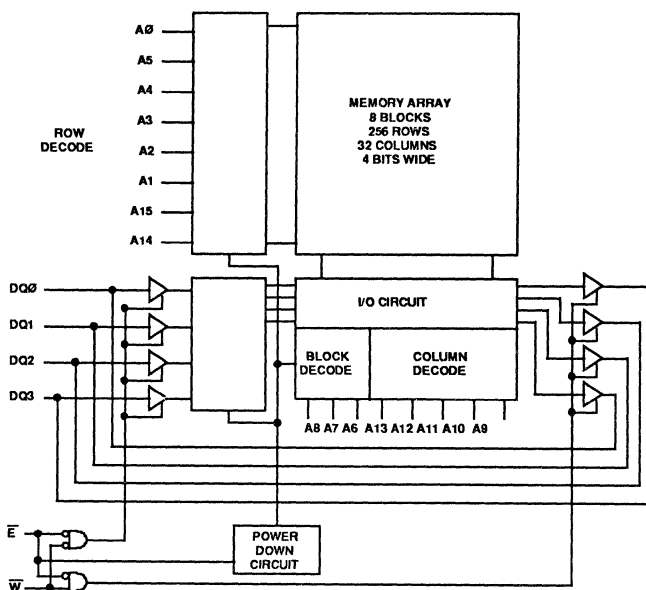
Single +5V ($\pm 10\%$) Supply Operation

Pin Configuration and Block Diagram



Pin Names

A0-A15	Address Inputs
E	Chip Enable
W	Write Enable
DQ0-DQ3	Common Data Input/Output
VCC	Power (+5V $\pm 10\%$)
VSS	Ground



Absolute Maximum Ratings*

Voltage on any pin relative to VSS-0.5V to 7.0V
 Operating Temperature TA (Ambient)
 Industrial.....-40°C to +85°C
 Military.....-55°C to +125°C
 Storage Temperature (Ambient/Ceramic). -65°C to +150°C
 Power Dissipation..... 1 Watt
 Output Current..... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels..... VSS to 3.0V
 Input Rise and Fall Times..... 5ns
 Input and Output Timing Levels..... 1.5V
 Output Load..... 1TTL, CL = 30pF
 (note: For TEHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}, \overline{E} = \text{VIL}, \text{I/O} = 0\text{mA}, \text{Min Cycle}$	C	--	80	120 mA
			P	--	80	100 mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E} \geq \text{VIH}, \text{VIN} \leq \text{VIL} \text{ or } \text{VIN} \geq \text{VIH}$	--	2	25	mA
Full Standby Power Supply Current	ICC3	$\overline{E} \geq \text{VCC}-0.2\text{V}$ $\text{VIN} \geq \text{VCC}-0.2\text{V} \text{ or } \text{VIN} \leq 0.2\text{V}$	C	--	1	10 mA
			P	--	0.5	3 mA
Input Leakage Current	IIL	VIN = 0V to VCC	--	--	±5	μA
Output Leakage Current	IOL	V I/O = 0V to VCC	--	--	±5	μA
Output High Voltage	VOH	IOH = -4.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL = 8.0mA	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{W}$	Mode	Output	Power
H	X	Standby	HIGH Z	ICC3
L	H	Read	DOUT	ICC1
L	L	Write	HIGH Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	CI	10	pF
Capacitance Control (DQ Pins)	CD/Q	12	pF

These parameters are sampled, not 100% tested.

AC Characteristics

Read Cycle

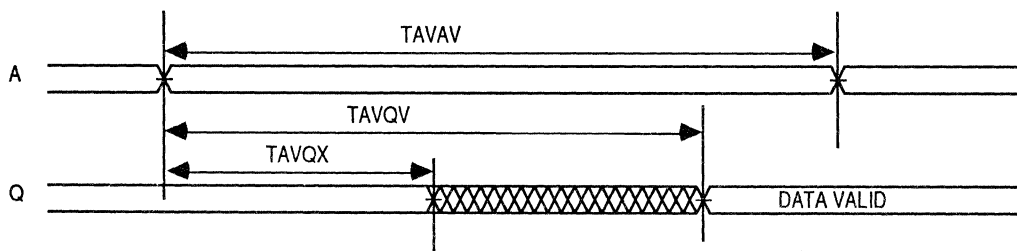
(TA = -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Symbol	45ns		55ns		70ns		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	35		45		55		ns
Address Access Time	TAVQV		35		45		55	ns
Chip Enable Access Time	TELQV		35		45		55	ns
Chip Enable to Output in Low Z (1)	TELQX	5		5		5		ns
Chip Enable to Output in High Z (1)	TEHQZ	0	15	0	20	0	25	ns
Output Hold from Address Change	TAVQX	5		5		5		ns
Chip Enable to Power Up (1)	TPU	0		0		0		ns
Chip Disable to Power Down (1)	TPD		35		45		55	ns

Note 1: Parameter guaranteed, but not tested.

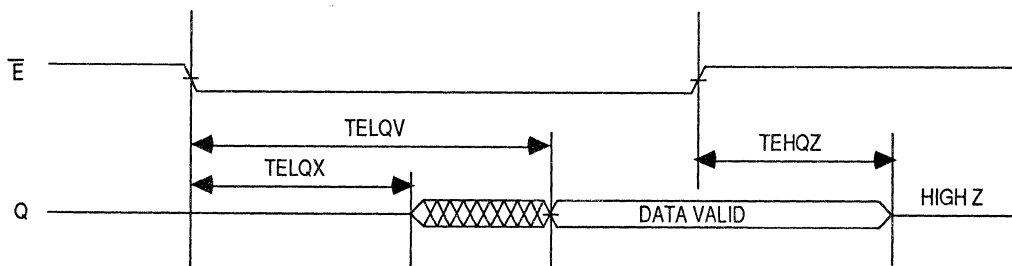
Read Cycle 1

W High (continuously selected, $\overline{E}$ Low)

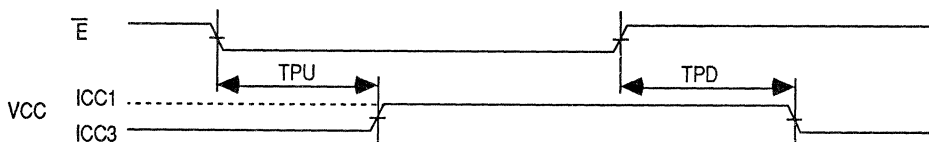


Read Cycle 2

$\overline{E}$ Low, $\overline{W}$ High



$\overline{E}$ Power Down Function



AC Characteristics

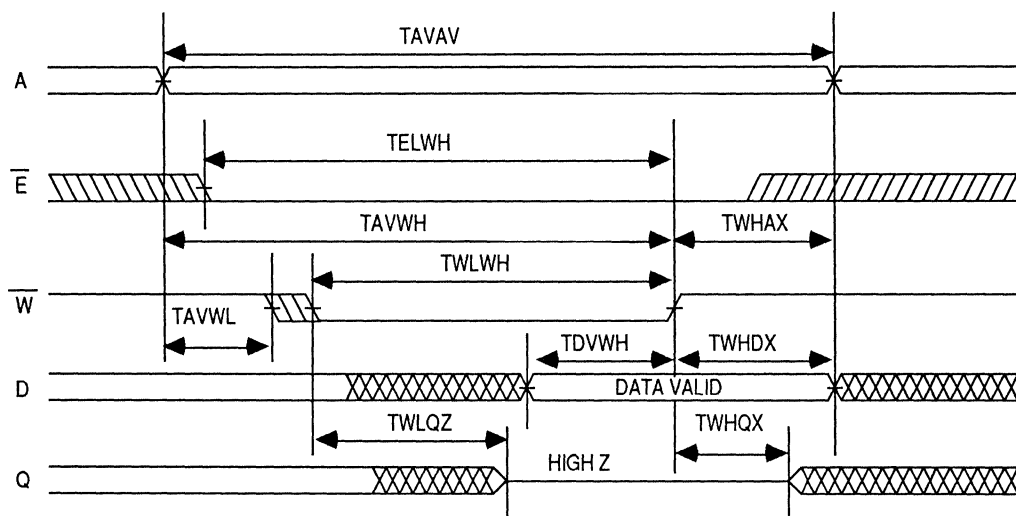
Write Cycle

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

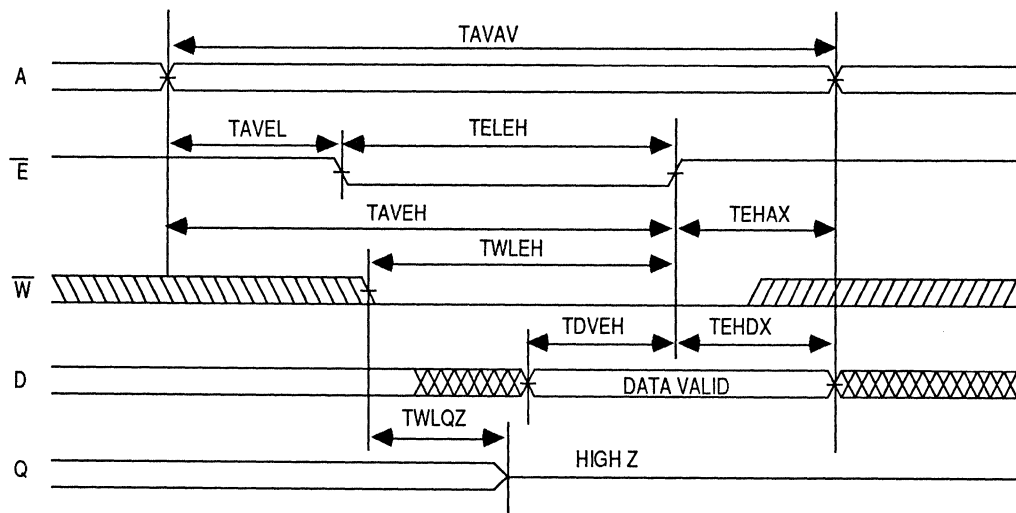
Parameter	Symbol		35ns		45ns		55ns		Units
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		35		45		55		ns
Chip Enable to	TELWH	$\overline{W}$	30		40		50		ns
End of Write	TWLEH	$\overline{E}$	30		40		50		ns
Address Setup Time	TAVWL	$\overline{W}$	0		0		0		ns
	TAVEL	$\overline{E}$	0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$	30		35		40		ns
	TAVEH	$\overline{E}$	30		35		40		ns
Write Pulse Width	TWLWH	$\overline{W}$	30		35		40		ns
	TELEH	$\overline{E}$	30		35		40		ns
Write Recovery Time	TWHAX	$\overline{W}$	5		5		5		ns
	TEHAX	$\overline{E}$	5		5		5		ns
Data Hold Time	TWHDX	$\overline{W}$	0		0		0		ns
	TEHDX	$\overline{E}$	0		0		0		ns
Write to Output in High Z (1)	TWLQZ		0	15	0	20	0	20	ns
Data to Write Time	TDVWH	$\overline{W}$	15		20		20		ns
	TDVEH	$\overline{E}$	15		20		20		ns
Output Active from End of Write (1)	TWHQX		0		0		0		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
***W* Controlled**



Write Cycle 2
***E* Controlled**



Data Retention Characteristics**Low Power (P) Version Only**

(TA = -55°C to +125°C)

Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E} \geq VDD - 0.2V$	--	50	500	μA
Chip Disable to Data Retention Time	TCDR	VIN $\geq$ VDD - 0.2V	0	--	--	ns
Operation Recovery Time	TR	or VIN $\leq$ 0.2V	TAVAV*	--	--	ns

*Read Cycle Time

**Data Retention
 $\overline{E}$ Controlled**