

8Kx8 Static RAM CMOS, Low Power Monolithic

PRELIMINARY

The EDI8810H/L is a 65,653bit, 6 transistor cell CMOS Static RAM organized as 8Kx8.

It is available in both standard (H) and low power (L) versions. Both versions offer battery back-up data retention capability at VDD equal to 2V and 3V.

In addition to 13 address inputs, and 8 common data inputs and outputs, the device contains 4 control lines. The $\bar{E}1$ and E2 lines perform chip enable functions and automatically power-down the device when proper logic levels are applied. The \bar{G} and W lines facilitate read and write operations.

All inputs and outputs are TTL compatible and operate from a single 5V supply.

Military product compliant to MIL-STD-883, Paragraph 1.2.1 is available.

Features

8Kx8 bit CMOS Static Random Access Memory

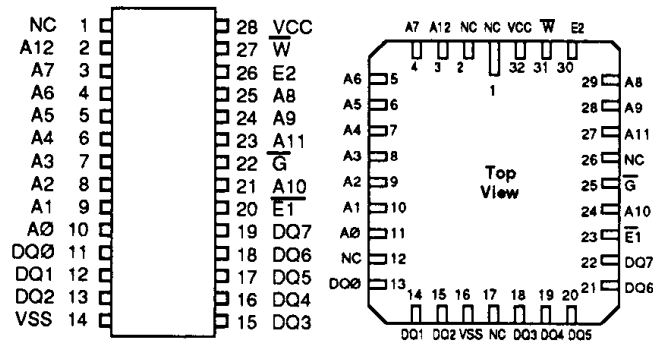
- Access Times 55 through 150ns
- \bar{E} and \bar{G} Functions for Bus Control
- Data Retention Function
- TTL Compatible Inputs and Outputs

Jedec Approved Pinouts

- 28 Pin CERDIP, 600 mils wide, No. 70
- 32 Pad Ceramic LCC, No. 12

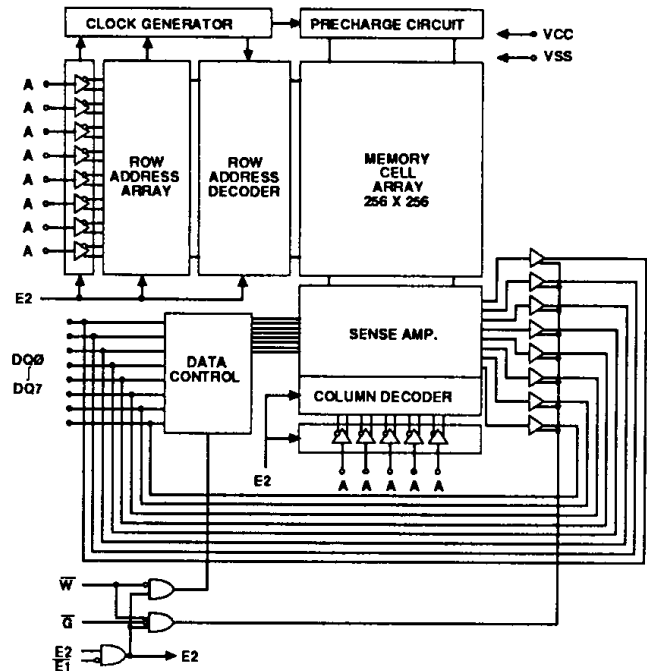
Single +5V ($\pm 10\%$) Supply Operation

Pin Configurations and Block Diagram



Pin Names

| | |
|-----------------|--------------------------|
| A0-A12 | Address Inputs |
| $\bar{E}1$, E2 | Chip Enables |
| W | Write Enable |
| \bar{G} | Output Enable |
| DQ0-DQ7 | Common Data Input/Output |
| VCC | Power (+5V $\pm 10\%$) |
| VSS | Ground |
| NC | No Connection |



Absolute Maximum Ratings*

| | |
|------------------------------------------|-----------------|
| Voltage on any pin relative to VSS | -0.5V to 8.0V |
| Operating Temperature TA (Ambient) | |
| Industrial | -40°C to +85°C |
| Military | -55°C to +125°C |
| Storage Temperature, Ceramic | -65°C to +150°C |
| Power Dissipation | 1 Watt |
| Output Current | 20 mA |
| Junction Temperature, TJ | 175°C |

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

| Parameter | Sym | Min | Typ | Max | Units |
|--------------------|-----|------|-----|-----|-------|
| Supply Voltage | VCC | 4.5 | 5.0 | 5.5 | V |
| Supply Voltage | VSS | 0 | 0 | 0 | V |
| Input High Voltage | VIH | 2.2 | -- | 6.0 | V |
| Input Low Voltage | VIL | -0.5 | -- | 0.8 | V |

AC Test Conditions

| | |
|--------------------------------------|------------------|
| Input Pulse Levels | VSS to 3.0V |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Levels | 1.5V |
| Output Load: | 1TTL, CL = 100pF |

(note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

| Parameter | Sym | Conditions | Min | Typ* | Max | Units | |
|------------------------------------|------|----------------------------------------------------------------------------|-----|------|---------|---------|---------|
| Operating Power Supply Current | ICC1 | $\overline{W}, \overline{E1} = VIL, I/O = 0mA, \text{Min Cycle}; E2 = VIH$ | -- | 45 | 70 | mA | |
| Standby (TTL) Power Supply Current | ICC2 | $\overline{E1} \geq VIH \text{ or } E2 \leq VIL$ | -- | -- | 2 | mA | |
| Full Standby Power Supply Current | ICC3 | $\overline{E1} \geq VCC-0.2V \text{ or } E2 \leq 0.2V$ | H | -- | 1 | 500 | μA |
| | | $VIN \geq VCC-0.2V \text{ or } VIN \leq 0.2V$ | L | -- | 0.2 | 100 | μA |
| Input Leakage Current | ILI | $VIN = 0V \text{ to } VCC$ | -- | -- | ± 5 | μA | |
| Output Leakage Current | ILO | $V I/O = 0V \text{ to } VCC$ | -- | -- | ± 5 | μA | |
| Output High Voltage | VOH | $IOH = -1.0mA$ | 2.4 | -- | -- | V | |
| Output Low Voltage | VOL | $IOL = 4.0mA$ | -- | -- | 0.4 | V | |

*Typical = TA = 25°C, VCC = 5.0V

Truth Table

| \overline{G} | $\overline{E1}$ | E2 | \overline{W} | Mode | Output | Power |
|----------------|-----------------|----|----------------|-----------------|--------|------------|
| X | H | X | X | Standby | High Z | ICC2, ICC3 |
| X | X | L | X | Standby | High Z | ICC2, ICC3 |
| H | L | H | H | Output Deselect | High Z | ICC1 |
| L | L | H | H | Read | DOUT | ICC1 |
| X | L | H | L | Write | DIN | ICC1 |

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

| Parameter | Sym | Max | | Unit |
|------------------------------------|------|-----|-----|------|
| | | LCC | DIP | |
| Input Capacitance (Except DQ Pins) | CI | 6 | 10 | pF |
| Capacitance Control (DQ Pins) | CD/Q | 8 | 12 | pF |

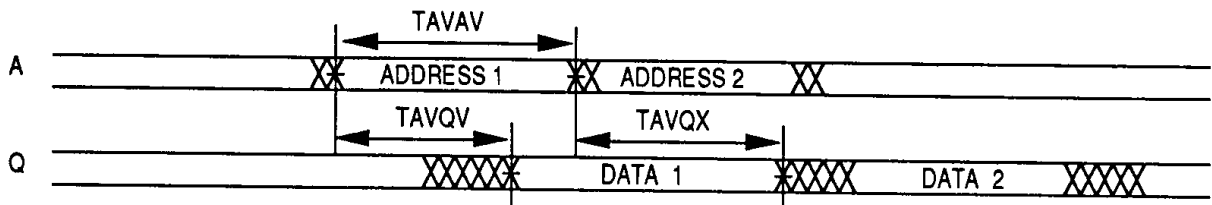
These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle

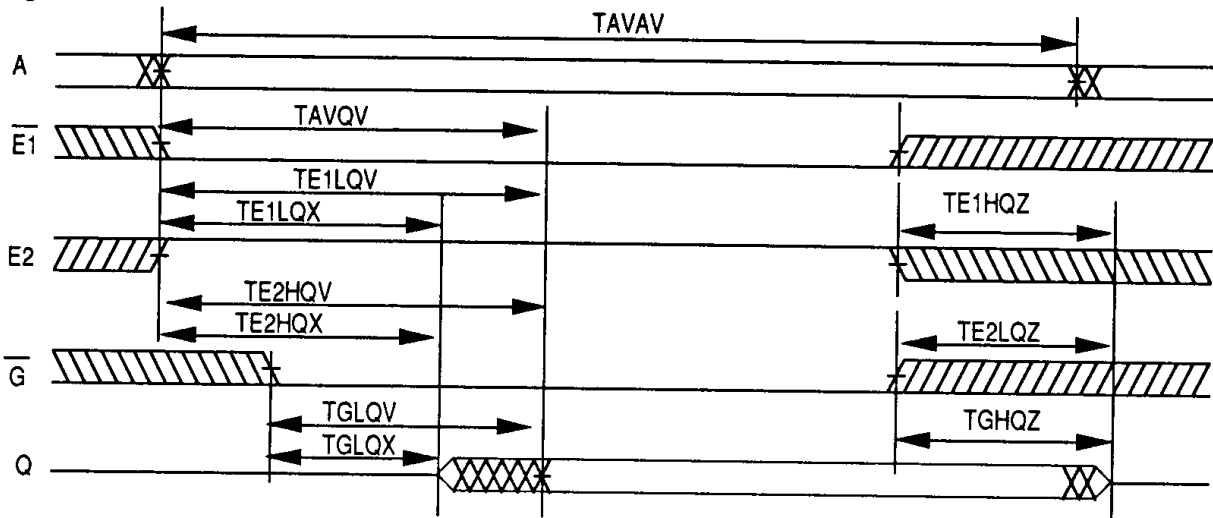
| Parameter | Symbol | 55ns | | 70ns | | 85ns | | 100ns | | 120ns | | 150ns | | Unit |
|----------------------------------------|--------|------|-----|------|-----|------|-----|-------|-----|-------|-----|-------|-----|------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | TAVAV | 55 | | 70 | | 85 | | 100 | | 120 | | 150 | | ns |
| Address Access Time | TAVQV | | 55 | | 70 | | 85 | | 100 | | 120 | | 150 | ns |
| Chip Enable Access Time | TE1LQV | | 55 | | 70 | | 85 | | 100 | | 120 | | 150 | ns |
| | TE2HQV | | 55 | | 70 | | 85 | | 100 | | 120 | | 150 | ns |
| Chip Enable to Output in Low Z (1) | TE1LQX | 5 | | 5 | | 5 | | 10 | | 10 | | 10 | | ns |
| | TE2HQX | 5 | | 5 | | 5 | | 10 | | 10 | | 10 | | ns |
| Output Enable to Output Valid | TGLQV | | 25 | | 35 | | 45 | | 45 | | 50 | | 50 | ns |
| Output Enable to Output in Low Z (1) | TGLQX | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Chip Disable to Output in High Z (1) | TE1HQZ | 0 | 25 | 0 | 35 | 0 | 40 | 0 | 40 | 0 | 40 | 0 | 40 | ns |
| | TE2LQZ | 0 | 25 | 0 | 35 | 0 | 40 | 0 | 40 | 0 | 40 | 0 | 40 | ns |
| Output Disable to Output in High Z (1) | TGHQZ | | 30 | | 35 | | 40 | | 40 | | 40 | | 40 | ns |
| Output Hold from Address Change | TAVQX | 10 | | 10 | | 10 | | 10 | | 10 | | 10 | | ns |

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
W, E2 High; G, E1 Controlled



Read Cycle 2
W High



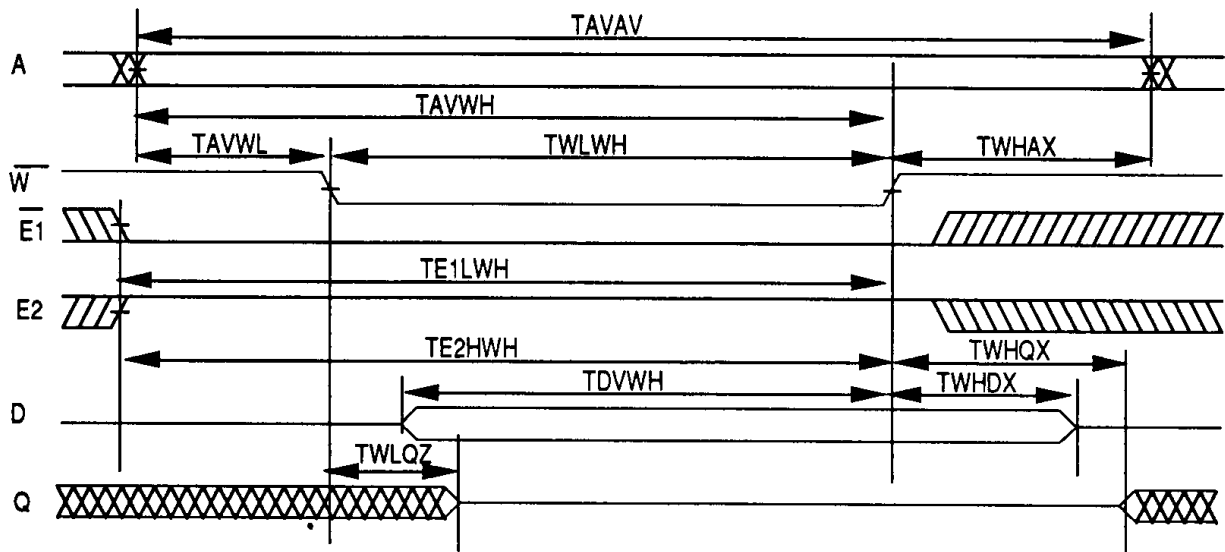
AC Characteristics

Write Cycle

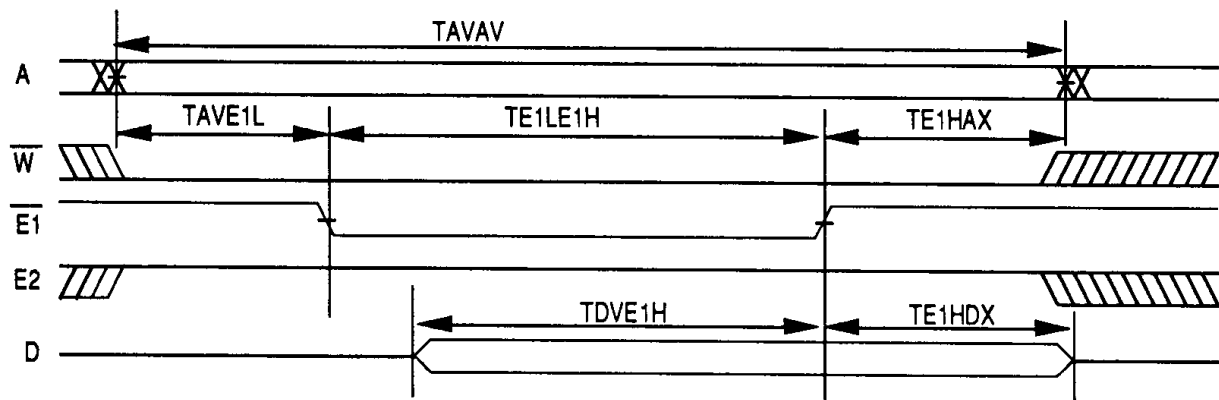
| Parameter | Symbol | | 55ns | | 70ns | | 85ns | | 100ns | | 120ns | | 150ns | | Unit |
|----------------------------------------|---------|-----------------|------|-----|------|-----|------|-----|-------|-----|-------|-----|-------|-----|------|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | TAVAV | | 55 | | 70 | | 85 | | 100 | | 120 | | 150 | | ns |
| Chip Enable to | TE1LWH | $\overline{E1}$ | 40 | | 50 | | 65 | | 65 | | 65 | | 65 | | ns |
| End of Write | TE2HWH | E2 | 40 | | 50 | | 65 | | 65 | | 65 | | 65 | | ns |
| Address Setup Time | TAVWL | \overline{W} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| | TAVE1L | $\overline{E1}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| | TAVE2H | E2 | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Address Valid to | TAVWH | | 40 | | 50 | | 65 | | 65 | | 65 | | 65 | | ns |
| Write Pulse Width | TWLWH | \overline{W} | 35 | | 40 | | 45 | | 45 | | 45 | | 45 | | ns |
| | TE1LE1H | $\overline{E1}$ | 35 | | 40 | | 45 | | 45 | | 45 | | 45 | | ns |
| | TE2HE2L | E2 | 35 | | 40 | | 45 | | 45 | | 45 | | 45 | | ns |
| Write Recovery Time | TWHAX | \overline{W} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| | TE1HAX | E1 | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| | TE2LAX | E2 | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Data Hold Time | TWHDX | \overline{W} | 5 | | 5 | | 5 | | 5 | | 5 | | 5 | | ns |
| | TE1HDX | $\overline{E1}$ | 5 | | 5 | | 5 | | 5 | | 5 | | 5 | | ns |
| | TE2LDX | E2 | 5 | | 5 | | 5 | | 5 | | 5 | | 5 | | ns |
| Write to Output in High Z (1) | TWLQZ | | | 20 | | 25 | | 30 | | 30 | | 30 | | 30 | ns |
| Data to Write Time | TDVWH | \overline{W} | 25 | | 30 | | 35 | | 35 | | 35 | | 35 | | ns |
| | TDVE1H | $\overline{E1}$ | 25 | | 30 | | 35 | | 35 | | 35 | | 35 | | ns |
| | TDVE2L | E2 | 25 | | 30 | | 35 | | 35 | | 35 | | 35 | | ns |
| Output Active from End of Write (1) | TWHQX | | 5 | | 5 | | 5 | | 5 | | 5 | | 5 | | ns |

Note 1: Parameter guaranteed, but not tested.

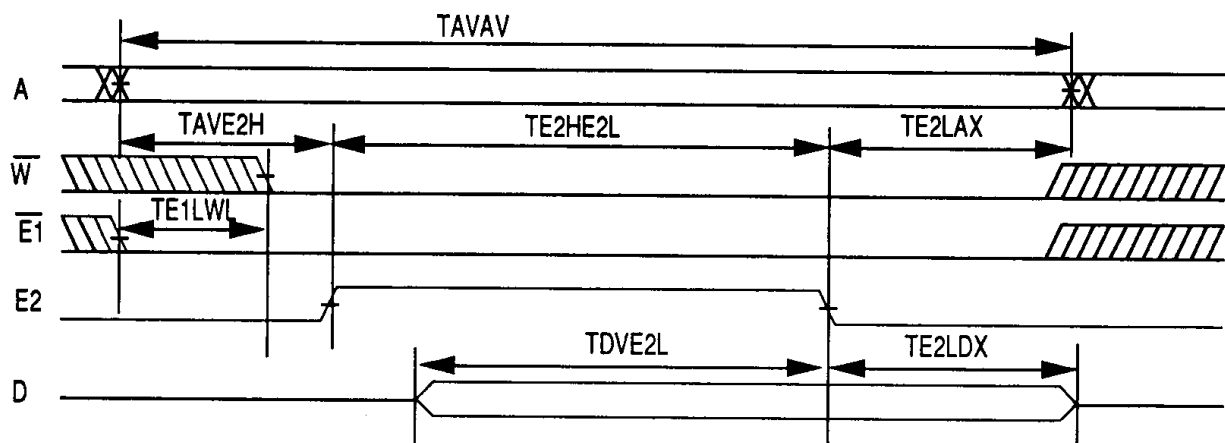
Write Cycle 1
Late Write, \overline{W} Controlled



Write Cycle 2
Early Write, $\overline{E1}$ Controlled



Write Cycle 3
Early Write, E2 Controlled

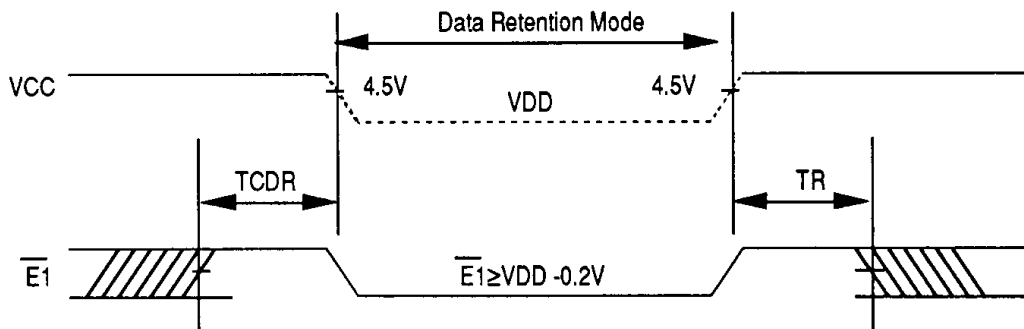


Data Retention Characteristics

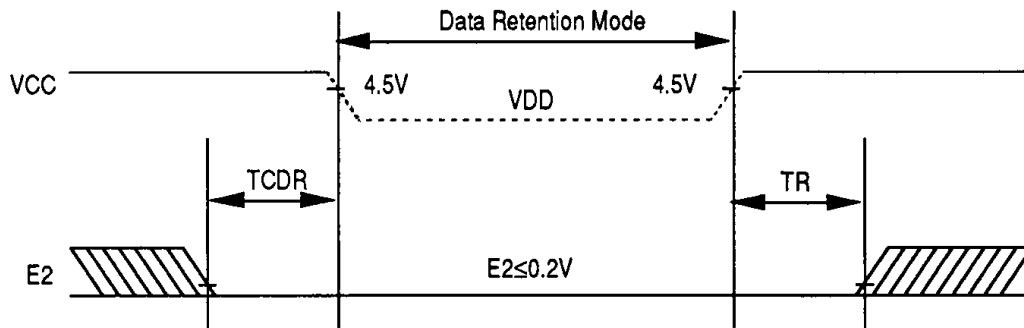
| Characteristic | Sym | Test Conditions | VDD | Min | Typ | Max | | Unit |
|-------------------------------------|-------|-----------------------------------------|-----|--------|-----|-----|----|---------|
| | | | | | | H | L | |
| Data Retention Voltage | VDD | $\bar{E}1 \geq VDD - 0.2V$ | | | 2 | -- | -- | V |
| Data Retention Quiescent Current | ICCDR | $E2 \leq 0.2V$ $VIN \geq VDD - 0.2V$ | 2V | -- | 0.1 | 200 | 50 | μA |
| | | | 3V | -- | 0.3 | 300 | 75 | μA |
| Chip Disable to Data Retention Time | TCDR | or $VIN \leq 0.2V$ | | 0 | -- | -- | -- | ns |
| Operation Recovery Time | TR | | | TAVAV* | -- | -- | -- | ns |

*Read Cycle Time

Data Retention $\bar{E}1$ Controlled



Data Retention E2 Controlled



Since its founding in 1980, Electronic Designs, Incorporated has been a recognized innovator in the packaging of high-performance memory devices, and was the first supplier to provide memory products incorporating the space saving benefits of surface mount technology. EDI's commercial and military CMOS SRAM modules, assembled using surface mount techniques developed at EDI, continue to lead the industry in performance, density, quality and reliability.

Experience in surface mount assembly has led EDI to understand its customers' packaging needs. As a result, EDI provides its customers with high performance monolithic CMOS memory devices in a variety of package styles to suit both surface mount and thru-hole applications.

As chip size increases with megabit+ densities compliant leads become essential for surface mount bond integrity. EDI has taken a leadership role by proposing a J-leaded ce-

ramic package as the next generation standard for military surface mount applications.

This package also brings the military standard closer to the commercial, since the CSOJ offers the same footprint and pinout as the standard commercial device packaged in plastic SOJ. The additional benefit of adopting this standard is an inherent cost reduction in prototyping, handling and testing.

EDI's CSOJ package is included in the latest revision of DESC-SMD 5962-89598 for the 128Kx8 SRAM.

Because EDI recognizes that customer's needs vary, EDI's memory devices are offered in the widest variety of standard package options on the market today, as demonstrated by the 15 pages of package drawings included in this data book. The specific package drawing for each product listed is shown in the Product Selector Guide, the first page of each product specification, and listed by part number beginning on page 343.