



256Kx8 Monolithic SRAM

FEATURES

- Access Times of 20, 25, 35, 45, 55ns
- Data Retention Function (LPA Versions)
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks
- Organized as 256Kx8
- Commercial, Industrial and Military Temperature Ranges
- JEDEC Approved Evolutionary Pinout
 - 32 pin Ceramic DIP, 0.6 mils wide (Package 9)
- Single +5V ($\pm 10\%$) Supply Operation

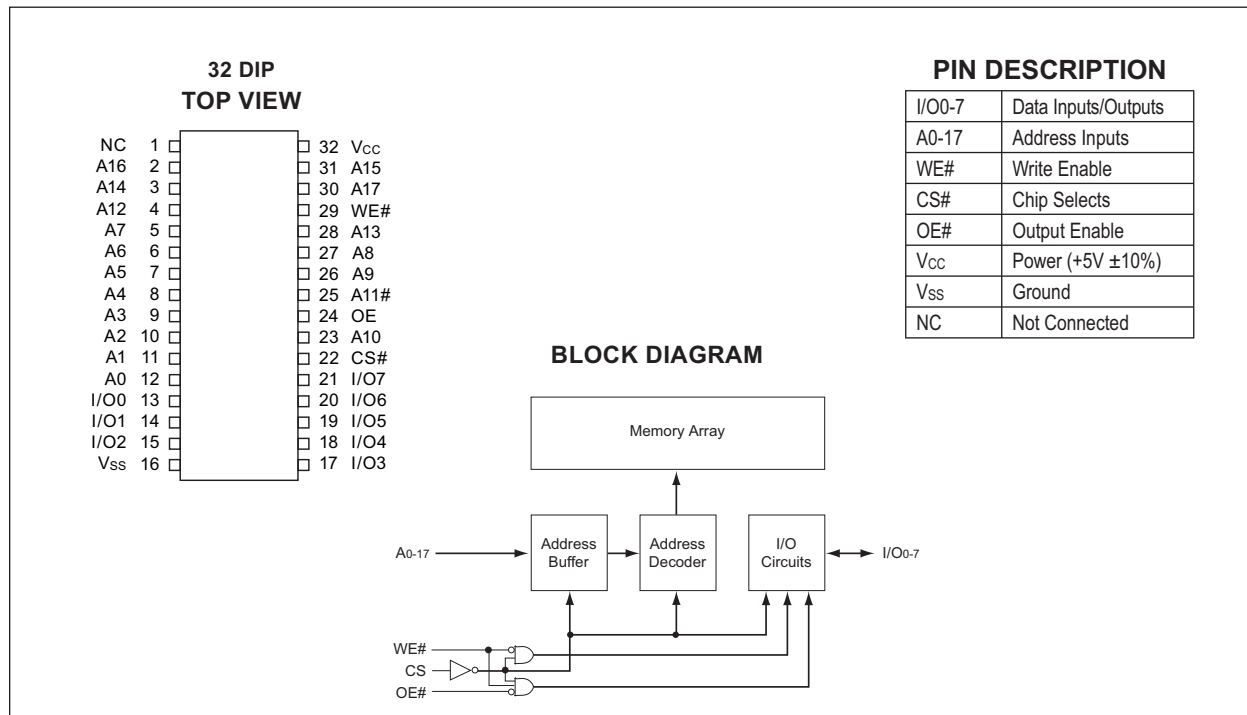
The EDI88257CA is a 2 Megabit 256Kx8 bit Monolithic CMOS Static RAM.

The 32 pin DIP pinout adheres to the JEDEC evolutionary standard for the two megabit device. The device is upgradeable to the 512Kx8 SRAM, the EDI88512CA. Pin 1 becomes the higher order address.

A Low Power version, EDI88257LPA, offers a data retention function for battery back-up operation. Military product is available compliant to Appendix A of MIL-PRF-38535.

This product is subject to change without notice.

FIGURE 1 – PIN CONFIGURATION





ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Voltage on any pin relative to Vss	-0.5 to 7.0	V
Operating Temperature T _A (Ambient)		
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Ceramic	-65 to +150	°C
Power Dissipation	1.5	W
Output Current	20	mA
Junction Temperature, T _J	175	°C

NOTE:

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

OE#	CS#	WE#	Mode	Output	Power
X	H	X	Standby	High Z	I _{CC2} , I _{CC3}
H	L	H	Output Deselect	High Z	I _{CC1}
L	L	H	Read	Data Out	I _{CC1}
X	L	L	Write	Data In	I _{CC1}

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Supply Voltage	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.2	—	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.3	—	+0.8	V

CAPACITANCE

Parameter	Symbol	Condition	Max	Unit
Address Lines	C _I	V _{IN} = V _{CC} or V _{SS} , f = 1.0MHz	12	pF
Data Lines	C _O	V _{OUT} = V _{CC} or V _{SS} , f = 1.0MHz	14	pF

These parameters are sampled, not 100% tested.

DC CHARACTERISTICS

V_{CC} = 5V, T_A = +25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Leakage Current	I _{LI}	V _{IN} = 0V to V _{CC}	-10	—	+10	μA
Output Leakage Current	I _{LO}	V _{IO} = 0V to V _{CC}	-10	—	+10	μA
Operating Power Supply Current	I _{CC1}	WE#, CS# = V _{IL} , I _{IO} = 0mA, Min Cycle (20-25ns) (35-55ns)	—	—	225	mA
Standby (TTL) Power Supply Current	I _{CC2}	CS# ≥ V _{IH} , V _{IN} ≤ V _{IL} , V _{IN} ≥ V _{IH}	—	—	60	mA
Full Standby Power Supply Current	I _{CC3}	CS# ≥ V _{CC} - 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	—	—	25	mA
Output Low Voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4	—	—	V

AC TEST CONDITIONS

Figure 1

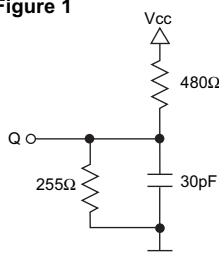
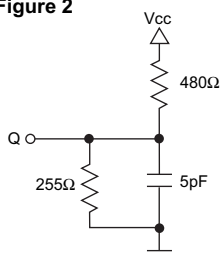


Figure 2



Input Pulse Levels	V _{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For t_{EHQZ}, t_{EHQZ} and t_{WLOZ}, C_L = 5pF Figure 2



AC CHARACTERISTICS – READ CYCLE

$V_{CC} = 5.0V$, $V_{SS} = 0V$, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol		20ns		25ns		35ns		45ns		55ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	20		25		35		45		55		ns
Address Access Time	t _{AVQV}	t _{AA}		20		25		35		45		55	ns
Chip Enable Access Time	t _{ELQV}	t _{ACS}		20		25		35		45		55	ns
Chip Enable to Output in Low Z (1)	t _{ELQX}	t _{CLZ}	3		3		3		3		3		ns
Chip Disable to Output in High Z (1)	t _{EHQZ}	t _{CHZ}	0	8	0	10	0	15	0	20	0	20	ns
Output Hold from Address Change	t _{AVQX}	t _{OH}	0		0		0		0		0		ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		10		12		15		25		25	ns
Output Enable to Output in Low Z (1)	t _{GLQX}	t _{OLZ}	0		0		0		0		0		ns
Output Disable to Output in High Z(1)	t _{GHQZ}	t _{OHZ}	0	8	0	10	0	15	0	20	0	20	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS – WRITE CYCLE

$V_{CC} = 5.0V$, $V_{SS} = 0V$, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol		20ns		25ns		35ns		45ns		55ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	20		25		35		45		55		ns
Chip Enable to End of Write	t _{ELWH}	t _{CW}	15		17		25		30		30		ns
	t _{ELEH}	t _{CW}	15		17		25		30		30		ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		0		0		0		ns
	t _{AVEL}	t _{AS}	0		0		0		0		0		ns
Address Valid to End of Write	t _{AVWH}	t _{AW}	15		17		25		30		30		ns
	t _{AVEH}	t _{AW}	15		17		25		30		30		ns
Write Pulse Width	t _{WLWH}	t _{WP}	15		17		25		30		30		ns
	t _{WLEH}	t _{WP}	15		17		25		30		30		ns
Write Recovery Time	t _{WHAX}	t _{WR}	0		0		0		0		0		ns
	t _{EHAX}	t _{WR}	0		0		0		0		0		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		0		0		ns
	t _{EHDX}	t _{DH}	0		0		0		0		0		ns
Write to Output in High Z (1)	t _{WLQZ}	t _{WHZ}	0	30	0	30	0	25	0	30	0	30	ns
Data to Write Time	t _{DVWH}	t _{DW}	10		12		20		25		25		ns
	t _{DVEH}	t _{DW}	10		12		20		25		25		ns
Output Active from End of Write (1)	t _{WHQX}	t _{WLZ}	0		0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.



FIGURE 2 – TIMING WAVEFORM - READ CYCLE

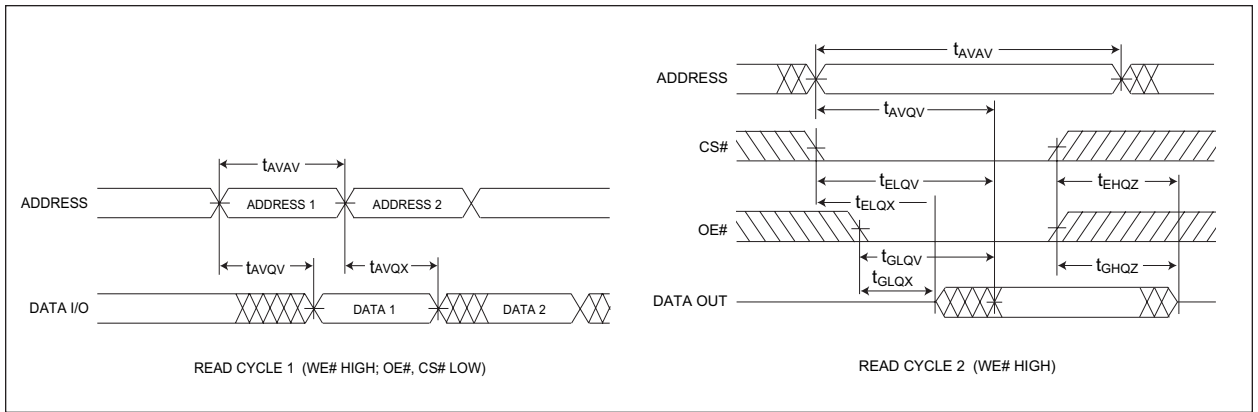


FIGURE 3 – WRITE CYCLE - WE# CONTROLLED

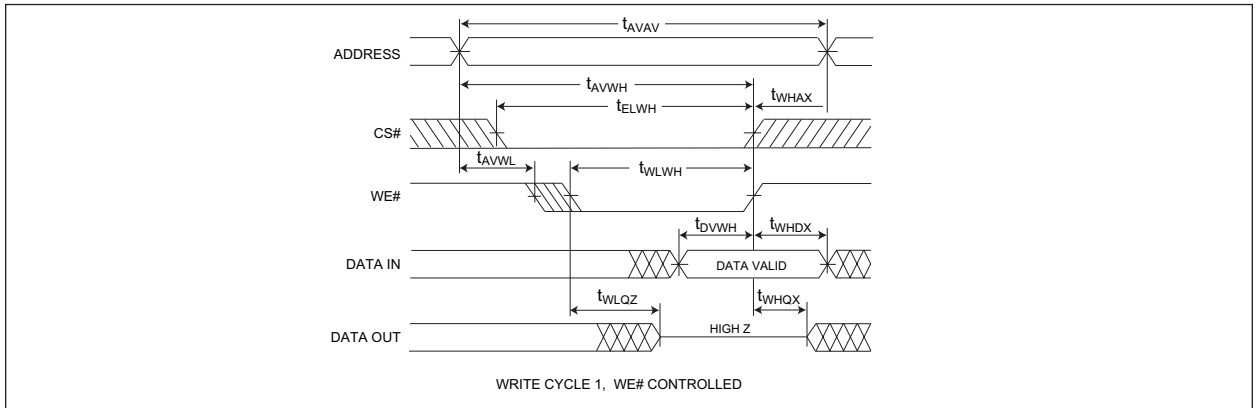
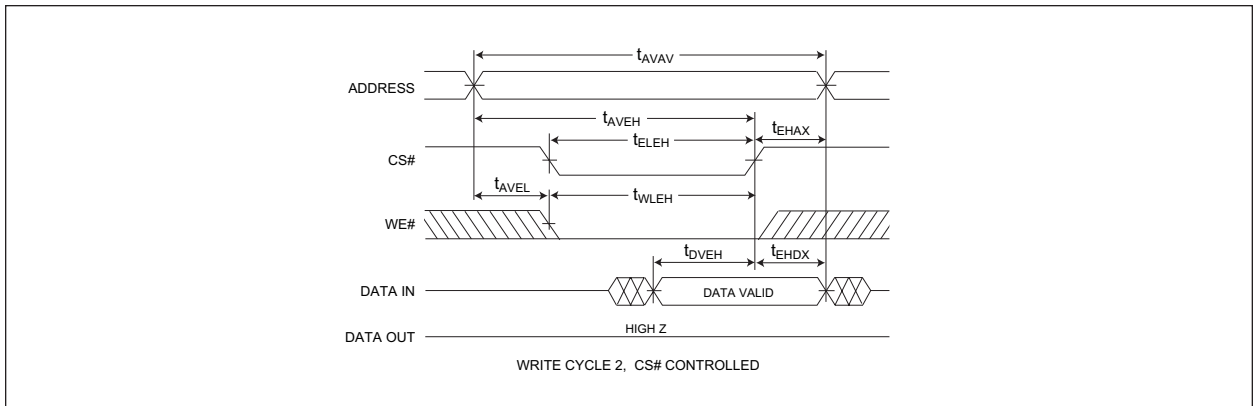


FIGURE 4 – WRITE CYCLE - CS# CONTROLLED



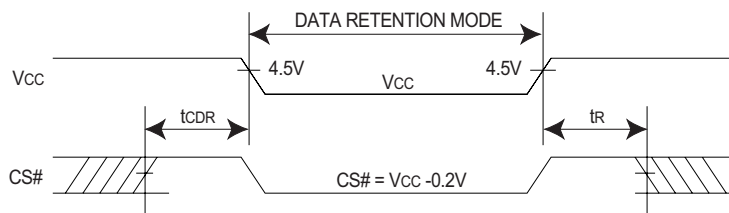


DATA RETENTION CHARACTERISTICS (EDI88512LP ONLY)

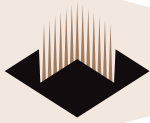
 $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$

Characteristic Low Power Version only	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage	V_{CC}	$V_{CC} = 2.0\text{V}$	2	—	—	V
Data Retention Quiescent Current	I_{CCDR}	$CS\# \geq V_{CC} - 0.2\text{V}$	—	—	2	μA
Chip Disable to Data Retention Time	t_{CDR}	$V_{IN} \geq V_{CC} - 0.2\text{V}$	0	—	—	ns
Operation Recovery Time	t_R	or $V_{IN} \leq 0.2\text{V}$	t_{AVAV}	—	—	ns

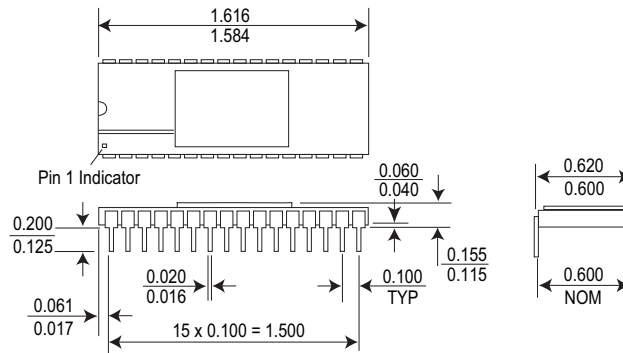
FIGURE 5 – DATA RETENTION - CS# CONTROLLED



DATA RETENTION, CS# CONTROLLED



PACKAGE 9: 32 PIN SIDEBRAZED CERAMIC DIP (600mils wide)



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

EDI 8 8257 CA X X X

WHITE ELECTRONIC DESIGNS

SRAM

ORGANIZATION, 256Kx8

TECHNOLOGY:

CA = CMOS Standard Power

LPA = Low Power

ACCESS TIME (ns)

PACKAGE TYPE:

C = 32 lead Sidebrazed DIP, 600 mil (Package 9)

DEVICE GRADE:

B = MIL-STD-883 Compliant

M = Military Screened

I = Industrial

C = Commercial

-55°C to +125°C

-40°C to +85°C

0°C to +70°C