### 32Kx8 Static RAM
### CMOS, Monolithic

The EDI8832C/P is a high performance, low power CMOS Static RAM organized as 32,768 words by 8 bits each. It is available in both standard power (C) and low power (P) versions.

Inputs and outputs are TTL compatible and allow for direct interfacing with common system bus structures.

The EDI8832C/P offers battery back-up data retention capability at VDD equal to 2V and operates from a 5 volt supply.

Military product is available 100% screened to MIL-STD-883C, Class B.

### Features

32Kx8 bit CMOS Static
Random Access Memory

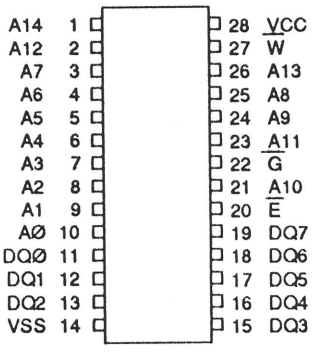
- Access Times 55,70, 85, 100, 120, and 150ns
- Data Retention Function
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

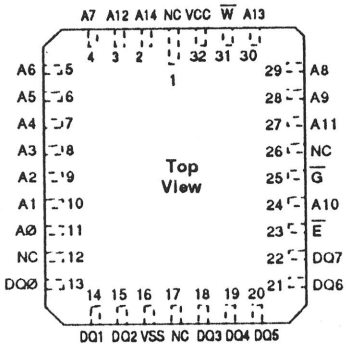
Jedec Approved Pinouts

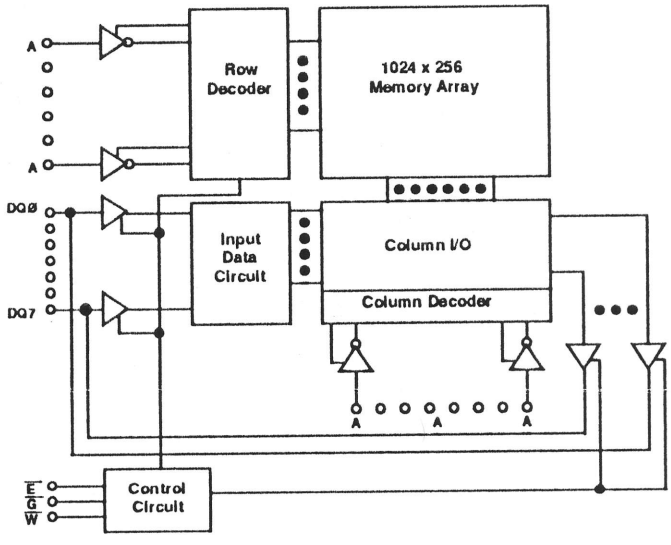
- 28 Pin Ceramic DIP, 300 mils wide (Q)
- 28 Pin Ceramic DIP, 600 mils wide (C)
- 32 Pad Ceramic LCC (L)

Single +5V (±10%) Supply Operation

### Pin Configuration and Block Diagram




### Pin Names

| | |
|---|---|
| AØ-A14 | Address Inputs |
| E | Chip Enable |
| W | Write Enable |
| G | Output Enable |
| DQØ-DQ7 | Common Data Input/Output |
| VCC | Power (+5V±10%) |
| VSS | Ground |

## Absolute Maximum Ratings*

Voltage on any pin relative to VSS .....-0.5V to 7.0V
Operating Temperature TA (Ambient)
Industrial.....-40°C to +85°C
Military.....-55°C to +125°C
Storage Temperature (Ambient/Ceramic). -65°C to +150°C
Power Dissipation..... 1 Watt
Output Current..... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended DC Operating Conditions

| Parameter | Sym | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Supply Voltage | VCC | 4.5 | 5.0 | 5.5 | V |
| Supply Voltage | VSS | 0 | 0 | 0 | V |
| Input High Voltage | VIH | 2.2 | -- | 6.0 | V |
| Input Low Voltage | VIL | -0.3 | -- | 0.8 | V |

## AC Test Conditions

Input Pulse Levels..... VSS to 3.0V
Input Rise and Fall Times..... 5ns
Input and Output Timing Levels..... 1.5V
Output Load.: 55/70ns..... 1TTL, CL =30pF
85/150ns..... 1TTL, CL = 100pF
(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

## DC Electrical Characteristics

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

| Parameter | Sym | Conditions | | Min | Typ* | Max | Units |
|---|---|---|---|---|---|---|---|
| Operating Power Supply Current | ICC1 | $\overline{W}$, $\overline{E}$ = VIL, I/O = 0mA, Min Cycle | | -- | 60 | 95 | mA |
| Standby (TTL) Power Supply Current | ICC2 | $\overline{E}$ ≥ VIH | | -- | 1 | 3 | mA |
| Full Standby Power Supply Current | ICC3 | $\overline{E}$ ≥ VCC-0.2V | C | -- | 200 | 1000 | µA |
| | | VIN ≥VCC-0.2V or VIN≤0.2V | P | -- | 20 | 250 | µA |
| Input Leakage Current | IIL | VIN = 0V to VCC | | -- | -- | ±5 | µA |
| Output Leakage Current | IOL | V I/O = 0V to VCC | | -- | -- | ±5 | µA |
| Output High Voltage | VOH | IOH = -1.0mA | | 2.4 | -- | -- | V |
| Output Low Voltage | VOL | IOL = 4.0mA | | -- | -- | 0.4 | V |

*Typical: TA = 25°C, VCC = 5.0V

## Truth Table

| $\overline{G}$ | $\overline{E}$ | $\overline{W}$ | Mode | Output | Power |
|---|---|---|---|---|---|
| X | H | X | Standby | High Z | ICC2, ICC3 |
| H | L | H | Output Deselect | High Z | ICC1 |
| L | L | H | Read | DOUT | ICC1 |
| X | L | L | Write | DIN | ICC1 |

## Capacitance

(f=1.0MHz, VIN=VCC or VSS)

| Parameter | Sym | Max | | Unit |
|---|---|---|---|---|
| | | LCC | DIP | |
| Input Capacitance (Except DQ Pins) | CI | 6 | 10 | pF |
| Capacitance Control (DQ Pins) | CD/Q | 8 | 12 | pF |

These parameters are sampled, not 100% tested.



## AC Characteristics

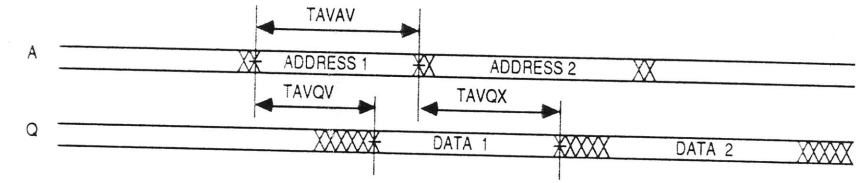
### Read Cycle

(TA = -55°C to +125°C; VCC = 5.0V ±10%)

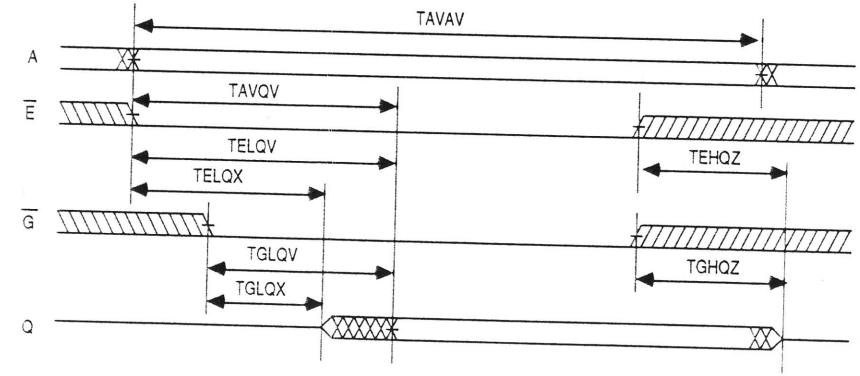
| Parameter | Symbol | 55ns | | 70ns | | 85ns | | 100ns | | 120ns | | 150ns | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | TAVAV | 55 | | 70 | | 85 | | 100 | | 120 | | 150 | | ns |
| Address Access Time | TAVQV | | 55 | | 70 | | 85 | | 100 | | 120 | | 150 | ns |
| Chip Enable Access Time | TELQV | | 55 | | 70 | | 85 | | 100 | | 120 | | 150 | ns |
| Chip Enable to Output in Low Z (1) | TELQX | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| Output Enable to Output Valid | TGLQV | | 30 | | 35 | | 35 | | 60 | | 60 | | 75 | ns |
| Output Enable to Output in Low Z (1) | TGLQX | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Chip Enable to Output in High Z (1) | TEHQZ | 0 | 30 | 0 | 35 | 0 | 35 | 0 | 35 | 0 | 40 | 0 | 45 | ns |
| Output Enable to Output in High Z (1) | TGHQZ | 0 | 30 | 0 | 35 | 0 | 35 | 0 | 35 | 0 | 40 | 0 | 45 | ns |
| Output Hold from Address Change | TAVQX | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |

Note 1: Parameter guaranteed, but not tested.

### Read Cycle 1
### W High; G, E Low




### Read Cycle 2
### W High



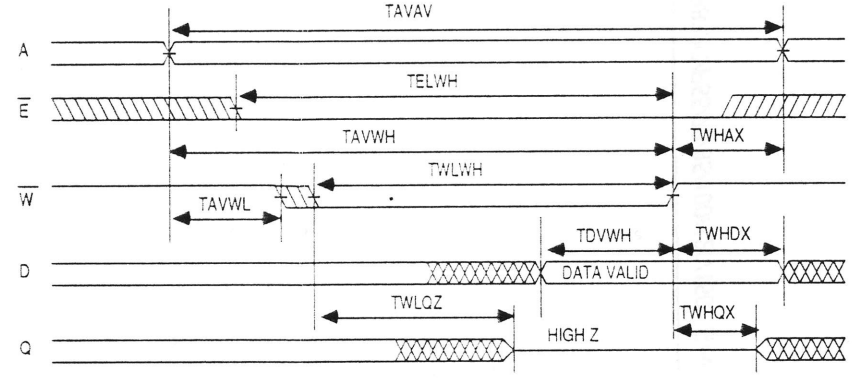
## AC Characteristics
### Write Cycle
(TA = -55°C to +125°C; VCC = 5.0V ±10%)

| Parameter | Symbol | | 55ns | | 70ns | | 85ns | | 100ns | | 120ns | | 150ns | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | TAVAV | | 55 | | 70 | | 85 | | 100 | | 120 | | 150 | | ns |
| Chip Enable to | TELWH | $\overline{W}$ | 45 | | 60 | | 70 | | 80 | | 85 | | 90 | | ns |
| End of Write | TWLEH | $\overline{E}$ | 50 | | 65 | | 65 | | 80 | | 85 | | 90 | | ns |
| Address Setup Time | TAVWL | $\overline{W}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| | TAVEL | $\overline{E}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Address Valid to | TAVWH | $\overline{W}$ | 45 | | 60 | | 70 | | 80 | | 85 | | 90 | | ns |
| End of Write | TAVEH | $\overline{E}$ | 45 | | 60 | | 70 | | 80 | | 85 | | 90 | | ns |
| Write Pulse Width | TWLWH | $\overline{W}$ | 35 | | 45 | | 55 | | 70 | | 70 | | 80 | | ns |
| | TELEH | $\overline{E}$ | 35 | | 45 | | 55 | | 70 | | 70 | | 80 | | ns |
| Write Recovery Time | TWHAX | $\overline{W}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| | TEHAX | $\overline{E}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Data Hold Time | TWHDX | $\overline{W}$ | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| | TEHDX | $\overline{E}$ | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| Write to Output in High Z (1) | TWLQZ | | 0 | 30 | 0 | 40 | 0 | 45 | 0 | 50 | 0 | 50 | 0 | 50 | ns |
| Data to Write Time | TDVWH | $\overline{W}$ | 25 | | 30 | | 35 | | 35 | | 40 | | 50 | | ns |
| | TDVEH | $\overline{E}$ | 25 | | 30 | | 35 | | 35 | | 40 | | 50 | | ns |
| Output Active from End of Write (1) | TWHQX | | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |

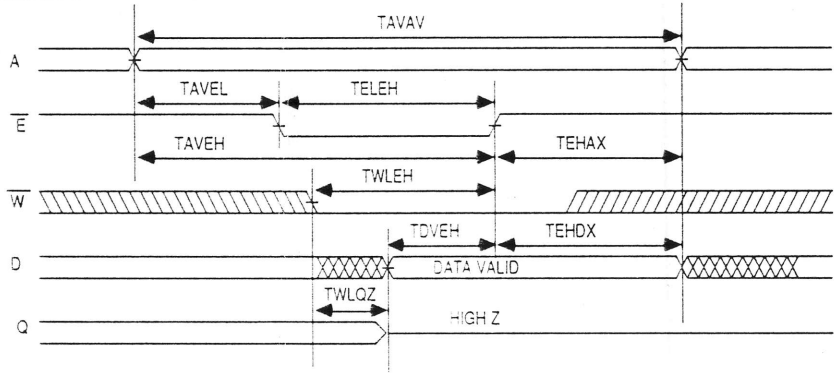
Note 1: Parameter guaranteed, but not tested.



### Write Cycle 1
### $\overline{W}$ Controlled




### Write Cycle 2
### $\overline{E}$ Controlled



## Data Retention Characteristics

(TA =-55°C to +125°C)

| Characteristic | Sym | Test Conditions | Min | | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Data Retention Voltage | VDD | VDD = 2.0V | 2 | | -- | -- | V |
| Data Retention Quiescent Current | ICCDR | $\overline{E}$≥ VDD -0.2V | C | -- | 100 | 500 | µA |
| | | VIN ≥VDD -0.2V | P | -- | 10 | 150 | µA |
| Chip Disable to Data Retention Time | TCDR | or VIN ≤0.2V | 0 | | -- | -- | ns |
| Operation Recovery Time | TR | | TAVAV* | | -- | -- | ns |

*Read Cycle Time

## Data Retention
## $\overline{E}$ Controlled