

512Kx8 Plastic Monolithic SRAM CMOS

FEATURES

- 512Kx8 bit CMOS Static
- Random Access Memory
 - Access Times of 17, 20, 25ns
 - Data Retention Function (LPA version)
 - Extended Temperature Testing
 - Data Retention Functionality Testing
- 36 lead JEDEC Approved Revolutionary Pinout
 - Plastic SOJ (Package 319)
- Single +5V ($\pm 10\%$) Supply Operation
- RoHS compliant

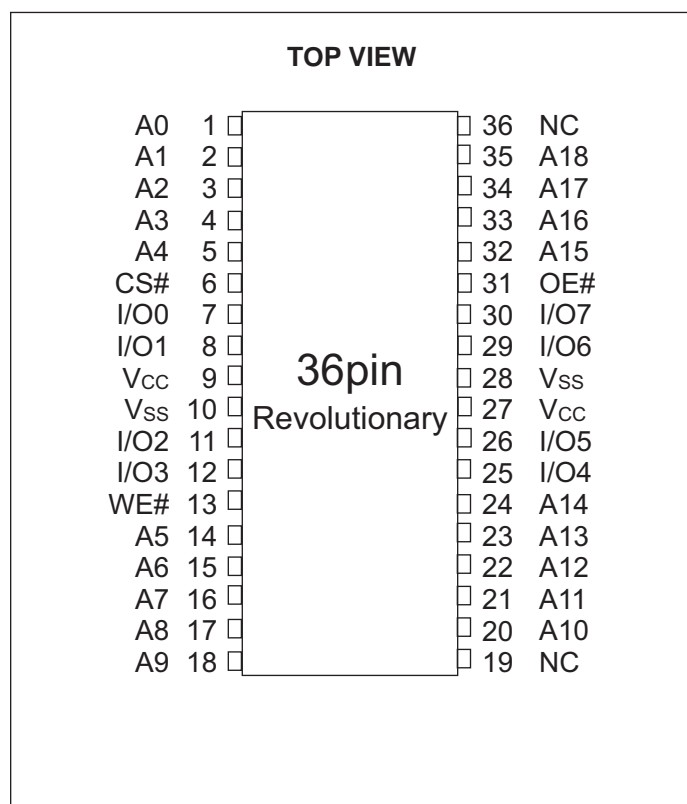
WEDC's ruggedized plastic 512Kx8 SRAM that allows the user to capitalize on the cost advantage of using a plastic component while not sacrificing all of the reliability available in a full military device.

Extended temperature testing is performed with the test patterns developed for use on WEDC's fully compliant 512Kx8 SRAMs. WEDC fully characterizes devices to determine the proper test patterns for testing at temperature extremes. This is critical because the operating characteristics of device change when it is operated beyond the commercial guarantee a device that operates reliably in the field at temperature extremes. Users of WEDC's ruggedized plastic benefit from WEDC's extensive experience in characterizing SRAMs for use in military systems.

WEDC ensures Low Power devices will retain data in Data Retention mode by characterizing the devices to determine the appropriate test conditions. This is crucial for systems operating at -40°C or below and using dense memories such as 512Kx8s.

WEDC's ruggedized plastic SOJ is footprint compatible with WEDC's full military ceramic 36 pin SOJ.

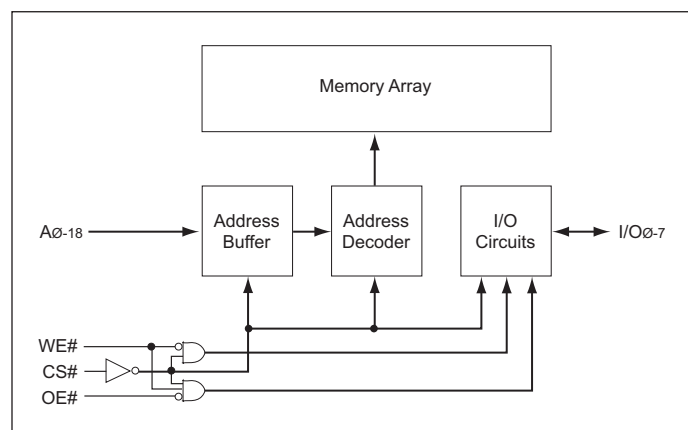
FIGURE 1 – PIN CONFIGURATION



PIN Description

I/O0-7	Data Inputs/Outputs
A0-18	Address Inputs
WE#	Write Enables
CS#	Chip Selects
OE#	Output Enable
VCC	Power (+5V $\pm 10\%$)
VSS	Ground
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on any pin relative to Vss	-0.5 to 7.0	V
Operating Temperature TA (Ambient)		
Commercial	0 to +70	°C
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Plastic	-65 to +150	°C
Power Dissipation	1.5	W
Output Current	20	mA
Junction Temperature, TJ	175	°C

NOTE:

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TRUTH TABLE

OE#	CS#	WE#	Mode	Output	Power
X	H	X	Standby	High Z	Icc2, Icc3
H	L	H	Output Deselect	High Z	Icc1
L	L	H	Read	Data Out	Icc1
X	L	L	Write	Data In	Icc1

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Supply Voltage	Vss	0	0	0	V
Input High Voltage	VIH	2.0	—	Vcc + 0.5	V
Input Low Voltage	VIL	-0.5	—	+0.8	V

CAPACITANCE

TA = +25°C

Parameter	Symbol	Condition	Max	Unit
Address Lines	CI	VIN = Vcc or Vss, f = 1.0MHz	8	pF
Data Lines	CO	VIN = Vcc or Vss, f = 1.0MHz	8	pF

These parameters are sampled, not 100% tested.

DC CHARACTERISTICS

Vcc = 5V, Vss = 0V, -55°C ≤ TA ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	ILI	Vcc = 5.5, VIN = Vss to Vcc		10	μA
Output Leakage Current	ILO	CS# = VIL, OE# = VIH, VOUT = Vss to Vcc		10	μA
Operating Supply Current	Icc	CS# = VIL, OE# = VIH, f = 5MHz, Vcc = 5.5		180	mA
Standby Current	ISB	CS# = VIH, OE# = VIH, f = 5MHz, Vcc = 5.5		15	mA
Output High Voltage	VOH	IOL = -4.0mA, Vcc = 4.5	2.4		V
Output Low Voltage	VOL	IOL = 8.0mA, Vcc = 4.5		0.4	V

NOTE: DC test conditions: VIL = 0.3V, VIH = Vcc - 0.3V

AC TEST CONDITIONS

Figure 1

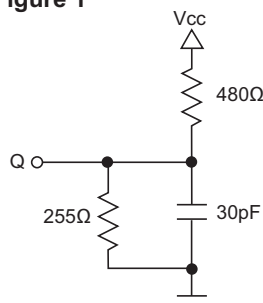
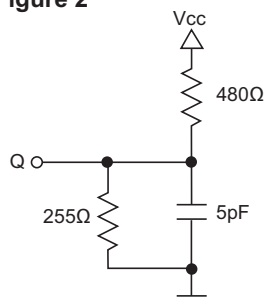


Figure 2



Input Pulse Levels	Vss to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For tEHQZ, tGHQZ and tWLQZ, CL = 5pF (Figure 2)

AC CHARACTERISTICS – READ CYCLE

 $V_{CC} = 5.0V, V_{SS} = 0V, 0^{\circ}C \leq T_A \leq +70^{\circ}C$

Parameter	Symbol		17ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	17		20		25		ns
Address Access Time	t _{AVQV}	t _{AA}		17		20		25	ns
Chip Enable Access Time	t _{ELQV}	t _{ACS}		17		20		25	ns
Chip Enable to Output in Low Z (1)	t _{ELQX}	t _{CLZ}	3		3		3		ns
Chip Disable to Output in High Z (1)	t _{EHQZ}	t _{CHZ}	0	7	0	8	0	10	ns
Output Hold from Address Change	t _{AVQX}	t _{OH}	0		0		0		ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		8		10		12	ns
Output Enable to Output in Low Z (1)	t _{GLQX}	t _{OLZ}	0		0		0		ns
Output Disable to Output in High Z(1)	t _{GHQZ}	t _{OHZ}	0	7	0	8	0	10	ns

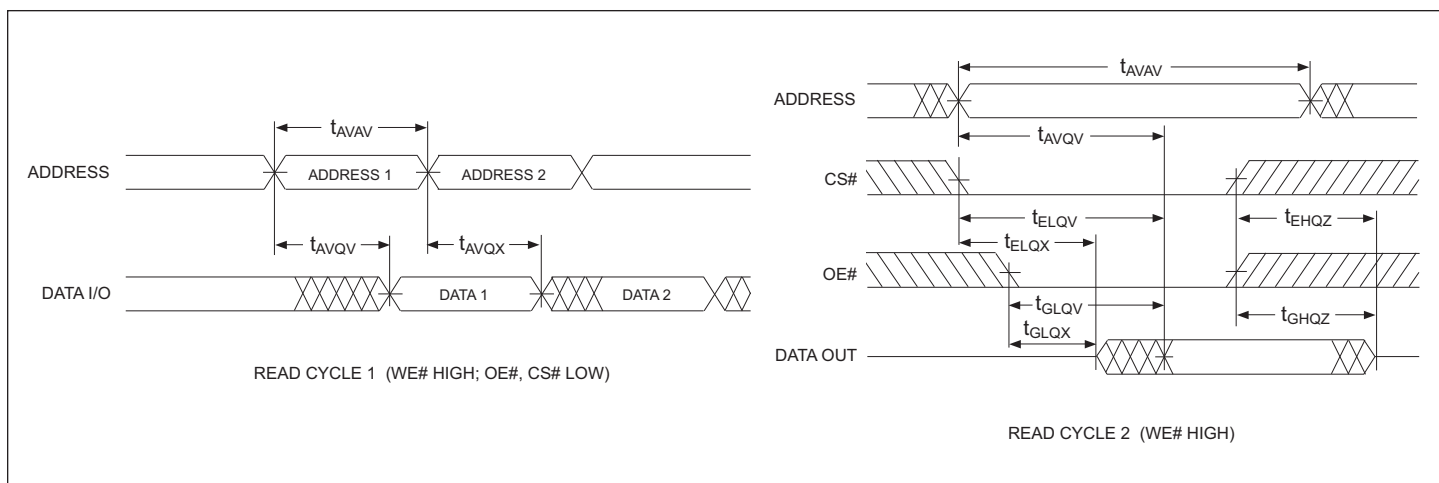
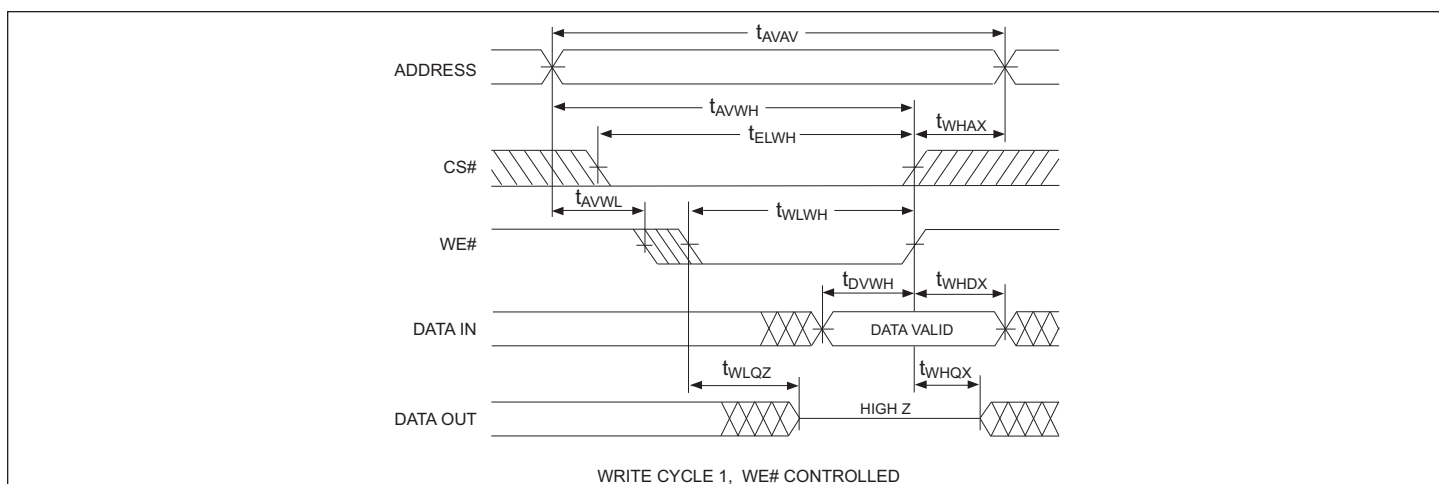
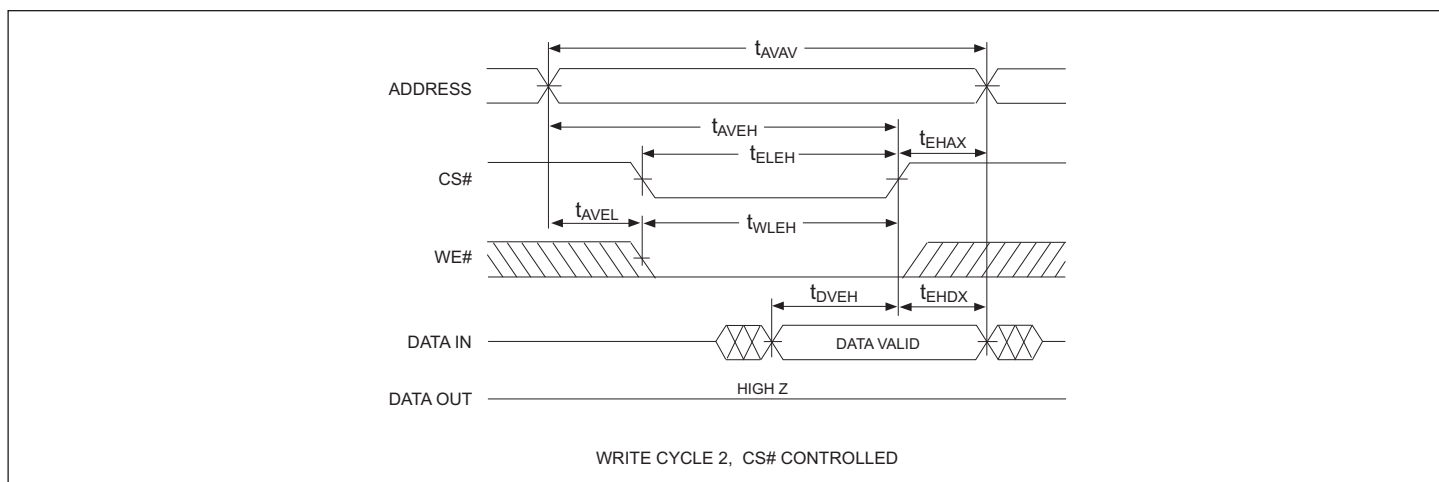
1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS – WRITE CYCLE

 $V_{CC} = 5.0V, V_{SS} = 0V, 0^{\circ}C \leq T_A \leq +70^{\circ}C$

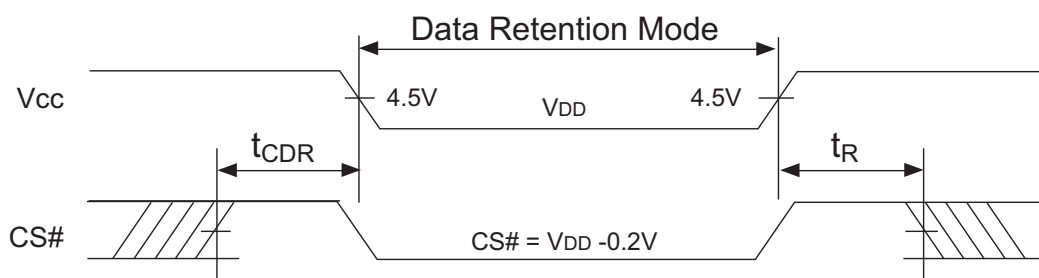
Parameter	Symbol		17ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	17		20		25		ns
Chip Enable to End of Write	t _{ELWH}	t _{CW}	14		15		17		ns
	t _{ELEH}	t _{CW}	14		15		17		ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		0		ns
	t _{AVEL}	t _{AS}	0		0		0		ns
Address Valid to End of Write	t _{AVWH}	t _{AW}	14		15		17		ns
	t _{AVEH}	t _{AW}	14		15		17		ns
Write Pulse Width	t _{WLWH}	t _{WP}	14		15		17		ns
	t _{WLEH}	t _{WP}	14		15		17		ns
Write Recovery Time	t _{WHAX}	t _{WR}	0		0		0		ns
	t _{EHAX}	t _{WR}	0		0		0		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		ns
	t _{EHDX}	t _{DH}	0		0		0		ns
Write to Output in High Z (1)	t _{WLQZ}	t _{WHZ}	0	8	0	8	0	10	ns
Data to Write Time	t _{DVWH}	t _{DW}	8		10		12		ns
	t _{DVEH}	t _{DW}	8		10		12		ns
Output Active from End of Write (1)	t _{WHQX}	t _{WLZ}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

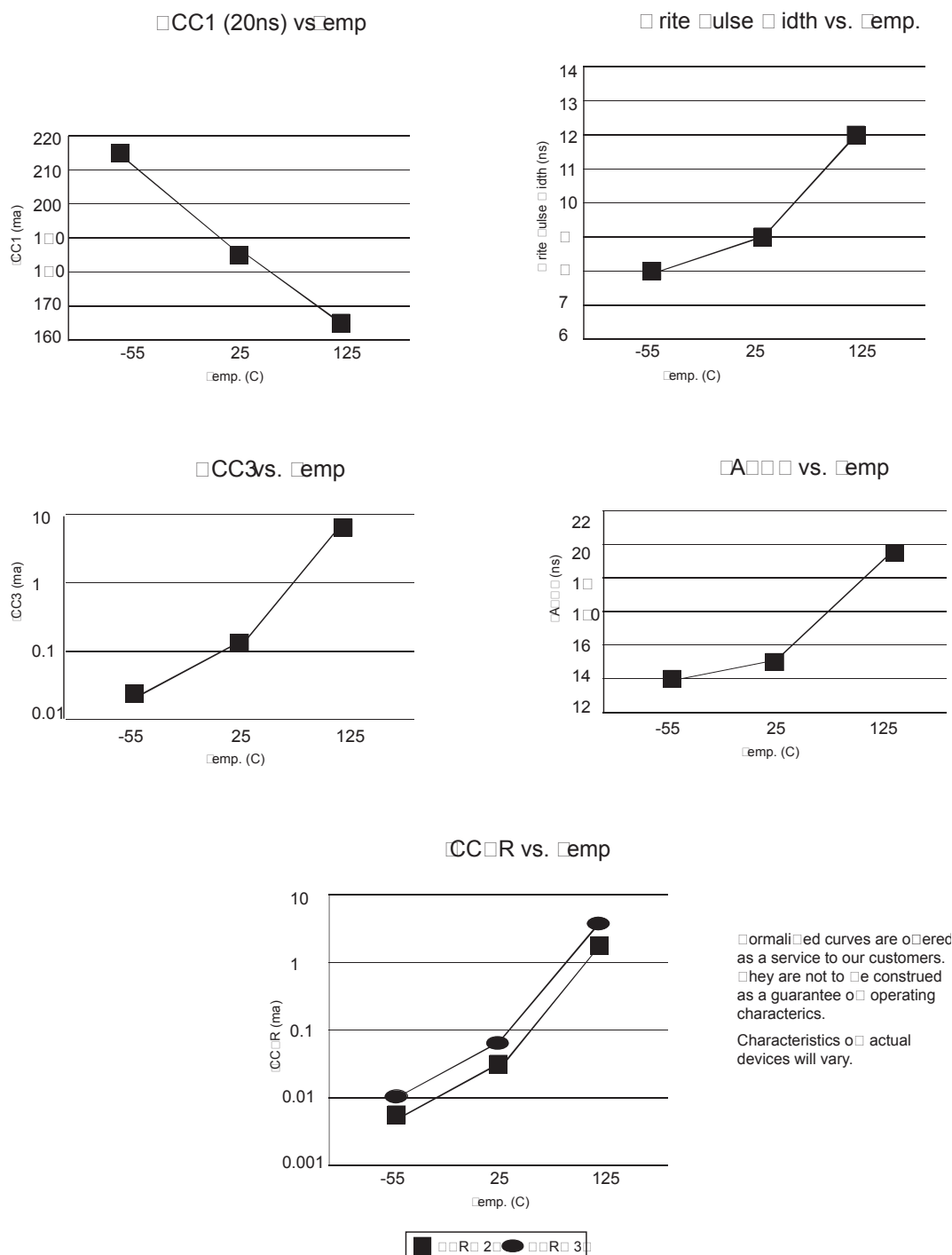
FIGURE 2 – TIMING WAVEFORM — READ CYCLE

FIGURE 3 – WRITE CYCLE — WE# CONTROLLED

FIGURE 4 – WRITE CYCLE — CS# CONTROLLED


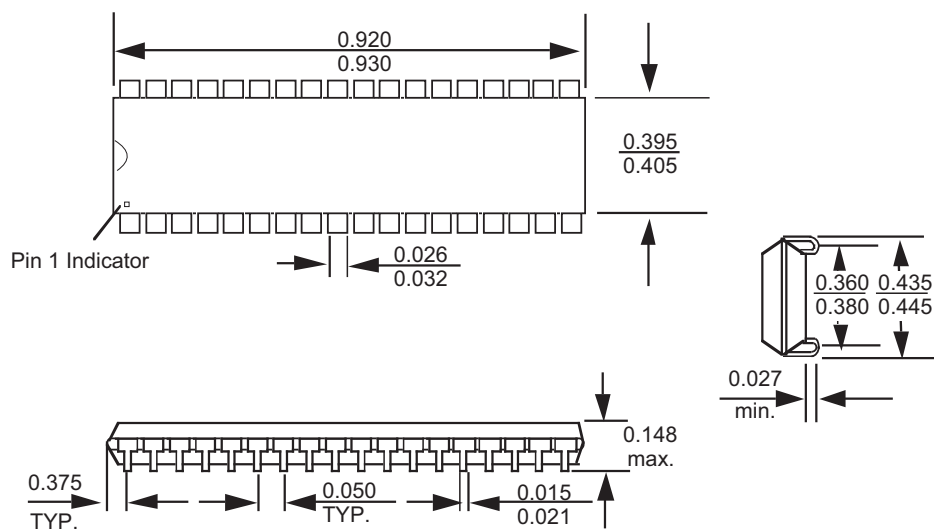
DATA RETENTION CHARACTERISTICS (EDI88512LPA ONLY)
 $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$

Characteristic Low Power Version only	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage	V_{DD}	$V_{DD} = 2.0\text{V}$	2	–	–	V
Data Retention Quiescent Current	I_{CCDR}	$CS\# \geq V_{DD} - 0.2\text{V}$	–	–	15	mA
Chip Disable to Data Retention Time	T_{CDR}	$V_{IN} \geq V_{DD} - 0.2\text{V}$	0	–	–	ns
Operation Recovery Time	T_R	or $V_{IN} \leq 0.2\text{V}$	T_{AVAV}	–	–	ns

FIGURE 5 – DATA RETENTION — CS# CONTROLLED


DATA RETENTION, CS# CONTROLLED

FIGURE 6 – NORMALIZED OPERATING GRAPHS


PACKAGE 319: 36 LEAD, PLASTIC SMALL OUTLINE J-LEAD (SOJ)


ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

	EDI	8	8512	CA	-	X	X	X	G
MICROSEMI CORPORATION: _____									
SRAM: _____									
ORGANIZATION, 512Kx8: _____									
TECHNOLOGY: _____									
CA = CMOS Standard Power									
LPA = Low Power									
ACCESS TIME (ns): _____									
PACKAGE TYPE: _____									
M = 36 lead Plastic SOJ									
RJ = Relvoutionary									
DEVICE GRADE: _____									
B = Military Grade*									
M = Military Screened -55°C to +125°C									
I = Industrial -40°C to +85°C									
C = Commercial 0°C to +70°C									
RoHS COMPLIANT: _____									

*This product is processed the same as the 5962-XXXXXMX product but all test and mechanical requirements are per the Microsemi data sheet.

ORDERING INFORMATION

	W	P	S	512K	8	X	X	-	XXX	RJ	X	G	A
MICROSEMI CORPORATION: _____													
PLASTIC PLUS®: _____													
SRAM: _____													
ORGANIZATION, 512K x 8: _____													
POWER: _____													
Blank = Standard Power													
L = Low Power													
IMPROVEMENT MARK: _____													
B = Burn-in													
T = Temperature Cycling													
C = Burn-in and Temperature Cycle													
ACCESS TIME (ns): _____													
PACKAGE: _____													
RJ = Revolutionary													
DEVICE GRADE: _____													
M = Military Temperature -55°C to +125°C													
I = Industrial Temperature -40°C to +85°C													
RoHS COMPLIANT: _____													
SOLDER DIPPED: _____													

Document Title

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Revision History

Rev #	History	Release Date	Status
Rev 7	Added RoHS compliance	November 2008	Final
Rev 8	Changes (Pg. 2, 8) 8.1 Add solder dipped to package options 8.2 Change CI to 8pF 8.3 Change V _{IH} to 2.0V and V _{IL} to -0.5V	February 2009	Final
Rev 9	Changes (Pg. 9) 9.1 Change document title: 512K x 8 Plastic Monolithic SRAM CMOS	March 2009	Final
Rev 10	Changes (Pg. 1-9) 10.1 Change document layout from White Electronic Designs to Microsemi	February 2011	Final
Rev 11	Changes (Pg. 8) 11.1 Changed EDI88512CA-XXMG Device Grade "B" description from "MIL-STD-883 Compliant" to "Military Grade*."	May 2014	Final