256Kx4 Static RAM CMOS, High Speed Module

The EDI8F4258C is a Megabit (256Kx4) high speed Static RAM Module with separate input/output lines. It is intended for use in any application where large quantities of memory are required and/or board space is of prime concern. The module is constructed of four 256Kx1 Static RAMs in plastic small outline J-leaded (SOJ) packages mounted onto a multilayered epoxy laminate (FR4) substrate.

Fully asynchronous, the EDI8F4258C requires no clocks or refreshing for operation. All inputs and outputs are TTL compatible and operate from a single 5 volt supply.

Features

256Kx4 bit CMOS Static
Random Access Memory Module
- Fast Access Times 20, 25, 35, 45, 55, and 70ns
- Fully Static, No Clocks
- Separate Data Inputs and Outputs

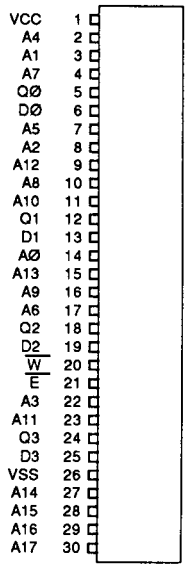
30 Pin Single-in-line package, No. 130
- Plastic SOJ on FR4 Substrate

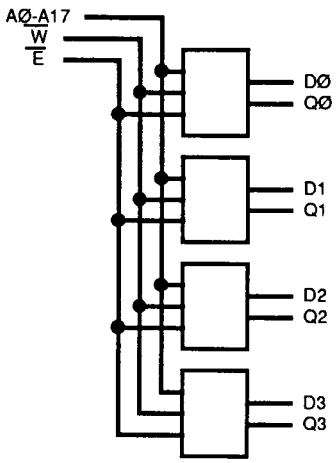
Single +5V (±10%) Supply Operation

Pin Names

AØ-A17	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
DØ-D3	Data Inputs
QØ-Q3	Data Outputs
VCC	Power (+5V±10%)
VSS	Ground

Pin Configuration and Block Diagram





Absolute Maximum Ratings*

Voltage on any pin relative to VSS ..... -0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial ..... 0°C to +70°C
Industrial ..... -40°C to +85°C
Storage Temperature, Plastic ..... -55°C to +125°C
Power Dissipation ..... 4 Watts
Output Current. ..... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels ..... VSS to 3.0V
Input Rise and Fall Times 5ns
Input and Output Timing Levels 1.5V
Output Load ..... 1TTL, CL = 30pF
(note: For TEHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	--	240	480	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$≥ VIH, VIN ≤ VIL or VIN ≥ VIH	--	--	100	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$≥ VCC-0.2V VIN ≥VCC-0.2V or VIN≤0.2V	--	--	40	mA
Input Leakage Current	ILI	VIN = 0V to VCC	--	--	±10	µA
Output Leakage Current	ILO	V I/O = 0V to VCC	--	--	±10	µA
Output High Voltage	VOH	IOH= -4.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL= 8.0mA	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{W}$	Mode	Output	Power
H	X	Standby	HIGH Z	ICC2, ICC3
L	H	Read	DOUT	ICC1
L	L	Write	HIGH Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance (Except D/Q Pins)	CI	32	pF
Capacitance Control (D/Q Pins)	CD/Q	15	pF

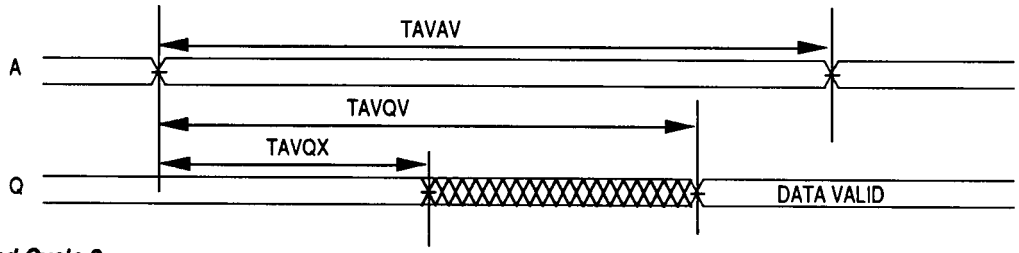
These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle

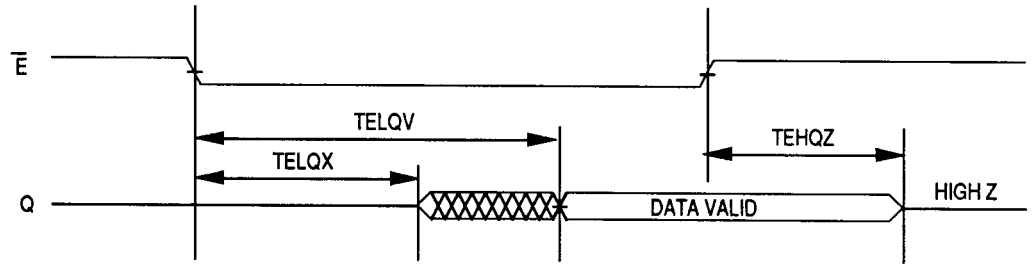
Parameter	Symbol	20ns		25ns		35ns		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	20		25		35		ns
Address Access Time	TAVQV		20		25		35	ns
Chip Enable Access Time	TELQV		20		25		35	ns
Chip Enable to Output in Low Z (1)	TELQX	3		3		5		ns
Chip Enable to Output in High Z (1)	TEHQZ	0	12	0	12	0	20	ns
Output Hold from Address Change	TAVQX	2		2		5		ns
Chip Enable to Power Up (1)	TPU	0		0		0		ns
Chip Disable to Power Down (1)	TPD	0	20	0	25	0	35	ns

Note 1: Parameter guaranteed, but not tested.

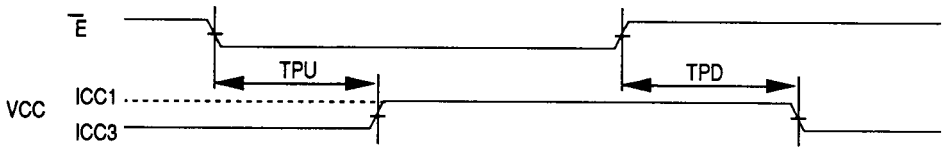
Read Cycle 1
$\overline{W}$ High (continuously selected, $\overline{E}$ Low)



Read Cycle 2
$\overline{E}$ Low, $\overline{W}$ High



$\overline{E}$ Power Down Function



AC Characteristics
Read Cycle

Parameter	Symbol	45ns		55ns		70ns		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	45		55		70		ns
Address Access Time	TAVQV		45		55		70	ns
Chip Enable Access Time	TELQV		45		55		70	ns
Chip Enable to Output in Low Z (1)	TELQX	5		5		5		ns
Chip Enable to Output in High Z (1)	TEHQZ	0	20	0	20	0	20	ns
Output Hold from Address Change	TAVQX	5		5		5		ns
Chip Enable to Power Up (1)	TPU	0		0		0		ns
Chip Disable to Power Down (1)	TPD	0	45	0	55	0	70	ns

Note 1: Parameter guaranteed, but not tested.

AC Characteristics
Write Cycle

Parameter	Symbol			20ns		25ns		35ns		Units
				Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV			20		25		35		ns
Chip Enable to	TELWH	$\overline{W}$		15		20		30		ns
End of Write	TELEH	$\overline{E}$		15		20		30		ns
Address Setup Time	TAVWL	$\overline{W}$		0		0		0		ns
	TAVEL	$\overline{E}$		0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$		15		20		30		ns
End of Write	TAVEH	$\overline{E}$		15		20		30		ns
Write Pulse Width	TWLWH	$\overline{W}$		10		15		25		ns
	TWLEH	$\overline{E}$		10		15		25		ns
Write Recovery Time	TWHAX	$\overline{W}$		0		0		5		ns
	TEHAX	$\overline{E}$		0		0		5		ns
Data Hold Time	TWHDX	$\overline{W}$		0		0		0		ns
	TEHDX	$\overline{E}$		0		0		0		ns
Write to Output in High Z (1)	TWLQZ			0	10	0	15	0	15	ns
Data to Write Time	TDVWH	$\overline{W}$		10		15		20		ns
	TDVEH	$\overline{E}$		10		15		20		ns
Output Active from End of Write (1)	TWHQX			0		0		0		ns

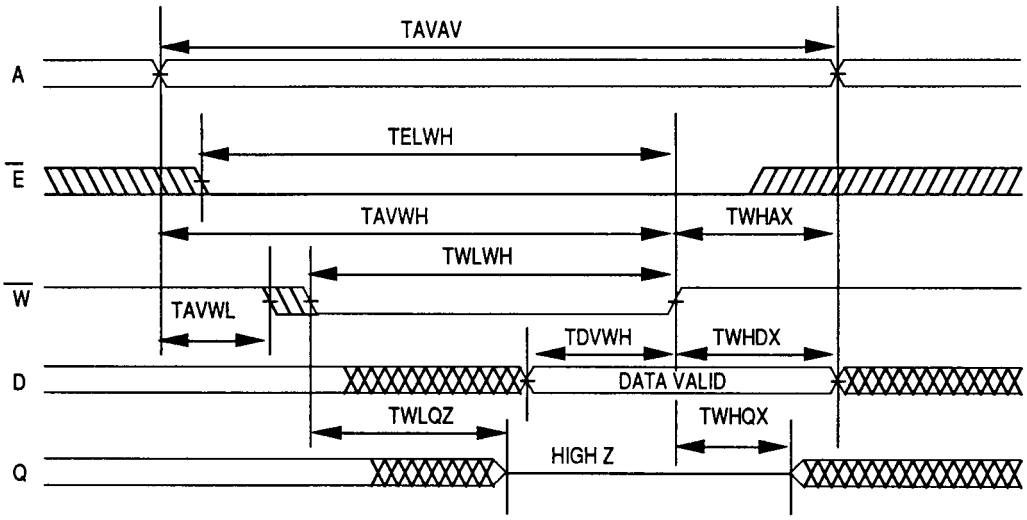
Note 1: Parameter guaranteed, but not tested.

AC Characteristics
Write Cycle

Parameter	Symbol			45ns		55ns		70ns		Units
				Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV			45		55		70		ns
Chip Enable to	TELWH	$\overline{W}$		35		40		45		ns
End of Write	TELEH	$\overline{E}$		35		40		45		ns
Address Setup Time	TAVWL	$\overline{W}$		0		0		0		ns
	TAVEL	$\overline{E}$		0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$		35		40		45		ns
End of Write	TAVEH	$\overline{E}$		35		40		45		ns
Write Pulse Width	TWLWH	$\overline{W}$		25		30		30		ns
	TWLEH	$\overline{E}$		25		30		30		ns
Write Recovery Time	TWHAX	$\overline{W}$		5		5		5		ns
	TEHAX	$\overline{E}$		5		5		5		ns
Data Hold Time	TWHDX	$\overline{W}$		0		0		0		ns
	TEHDX	$\overline{E}$		0		0		0		ns
Write to Output in High Z (1)	TWLQZ			0	15	0	20	0	20	ns
Data to Write Time	TDVWH	$\overline{W}$		25		25		25		ns
	TDVEH	$\overline{E}$		25		25		25		ns
Output Active from End of Write (1)	TWHQX			0		0		0		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled