



# 512Kx8 STATIC RAM CMOS, MODULE

## FEATURES

- 512Kx8 bit CMOS Static
- Random Access Memory
  - Access Times 20 through 100ns
  - Data Retention Function (EDI8F8512LP)
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- High Density Packaging
  - 36 Pin SIP, No. 63
  - 32 Pin DIP, JEDEC Pinout, No. 91 (55-100ns)
  - 32 Pin DIP, JEDEC Pinout, No. 183 (20-35ns)
- Single +5V ( $\pm 10\%$ ) Supply Operation

\*This product is subject to change without notice.

## DESCRIPTION

The EDI8F8512C is a 4096K bit CMOS Static RAM based on four 128Kx8 or 256Kx4 (high speed) Static RAMs mounted on a multi-layered epoxy laminate (FR4) substrate.

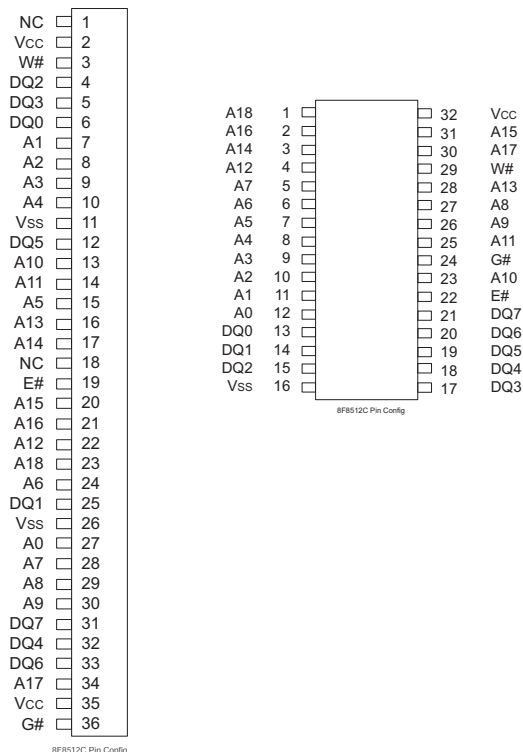
Functional equivalence to the monolithic four megabit Static RAM is achieved by utilization of an on-board decoder that interprets the higher order address(es) to select one of the 128Kx8 or 256Kx4 Static RAMs.

The 32 pin DIP pinout adheres to the JEDEC standard for the four megabit device, to ensure compatibility with future monolithics.

A low power version with data retention (EDI8F8512LP) is also available.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous, the EDI8F8512C requires no clocks or refreshing for operation.

FIG. 1 PIN CONFIGURATIONS

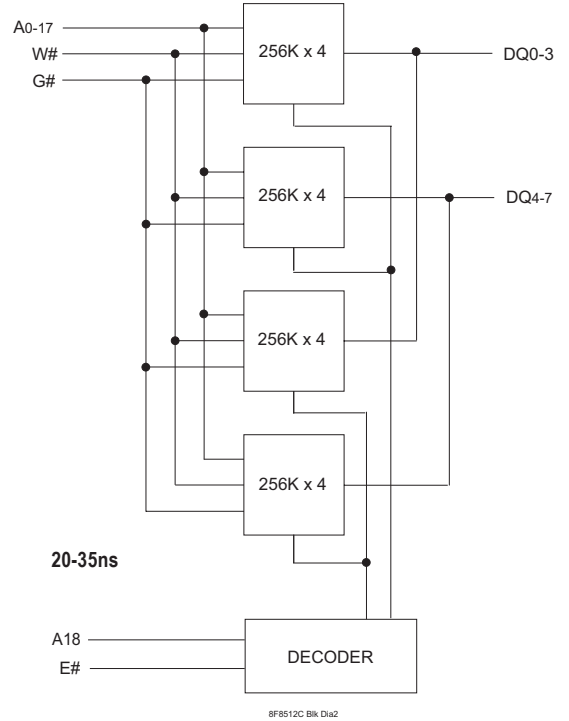
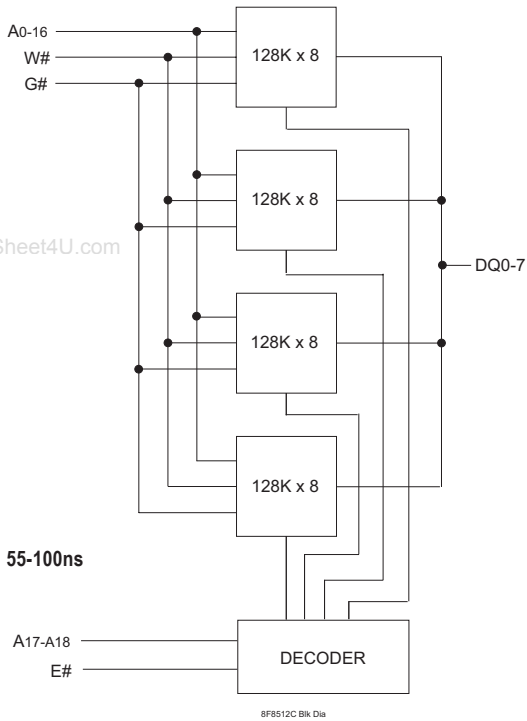


### PIN NAMES

A0-A18	Address Inputs
E#	Chip Enable
W#	Write Enable
G#	Output Enable
DQ0-DQ7	Common Data Input/Output
Vcc	Power (+5V $\pm 10\%$ )
Vss	Ground
NC	No Connection



**FIG. 2 BLOCK DIAGRAMS**





**ABSOLUTE MAXIMUM RATINGS\***

Voltage on any pin relative to V <sub>SS</sub>	-0.5V to 7.0V
Operating Temperature T <sub>A</sub> (Ambient)	0°C to +70°C Commercial Industrial -40°C to +85°C
Storage Temperature	-55°C to +125°C
Power Dissipation	4 Watt
Output Current	20 mA

\*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Supply Voltage	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.2	-	6.0	V
Input Low Voltage	V <sub>IL</sub>	-0.3	-	0.8	V

**AC TEST CONDITIONS**

Input Pulse Levels	V <sub>SS</sub> to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	20-35ns 70-100ns
	1TTL = 30pF 1TTL, CL = 100pF

(Note: For t<sub>EHQZ</sub>, t<sub>GHQZ</sub> and t<sub>WLQZ</sub>, CL = 5pF)

**DC ELECTRICAL CHARACTERISTICS**

Parameter	Sym	Conditions	Min					Typ*					Units	
			≤35					≤55						
Operating Power Supply Current	I <sub>CC1</sub>	W#, E# = V <sub>IL</sub> , I/O = 0mA, Min Cycle	340	70	570	390	130							mA
Standby (TTL) Power Supply Current	I <sub>CC2</sub>	E# ≥ V <sub>IH</sub> , V <sub>IN</sub> ≤ V <sub>IL</sub> V <sub>IN</sub> ≥ V <sub>IH</sub>	DIP	-	50	10	85	85	55					mA
			SIP	-	-	-	-	65						mA
Full Standby Power Supply Current (CMOS)	I <sub>CC3</sub>	E# ≥ V <sub>CC</sub> -0.2V V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤ 0.2V	C	-	5	2	40	40	5					mA
			LP	-	-	40	-	-	400					μA
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = 0V to V <sub>CC</sub>	-	-	-	-	±10	±10	±10					μA
Output Leakage Current	I <sub>LO</sub>	V I/O = 0V to V <sub>CC</sub>	-	-	-	-	±10	±10	±10					μA
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA (≥70), or -4.0 (≤35)	2.4	-	-	-	-	-	-					V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1mA (≥70), or 8.0mA (≤35)	-	-	-	-	0.4	0.4	0.4					V

\*Typical: T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0V

**TRUTH TABLE**

G#	E#	W#	Mode	Output	Power
X	H	X	Standby	HIGH Z	I <sub>CC2</sub> /I <sub>CC3</sub>
H	L	H	Output Deselect	HIGH Z	I <sub>CC1</sub>
L	L	H	Read	D <sub>OUT</sub>	I <sub>CC1</sub>
X	L	L	Write	D <sub>IN</sub>	I <sub>CC1</sub>

**CAPACITANCE**

(f=1.0MHz, V<sub>IN</sub>=V<sub>CC</sub> or V<sub>SS</sub>)

Parameter	Sym	Max	Unit
Address Lines	CI	30	pF
Data Lines	CD/Q	43	pF
Chip Enable Line	CC	10	pF
Write and Output Enable Lines	CW	32	pF

These parameters are sampled, not 100% tested.

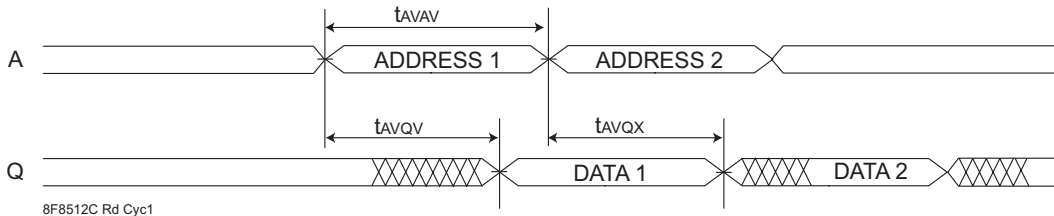


**AC CHARACTERISTICS READ CYCLE**

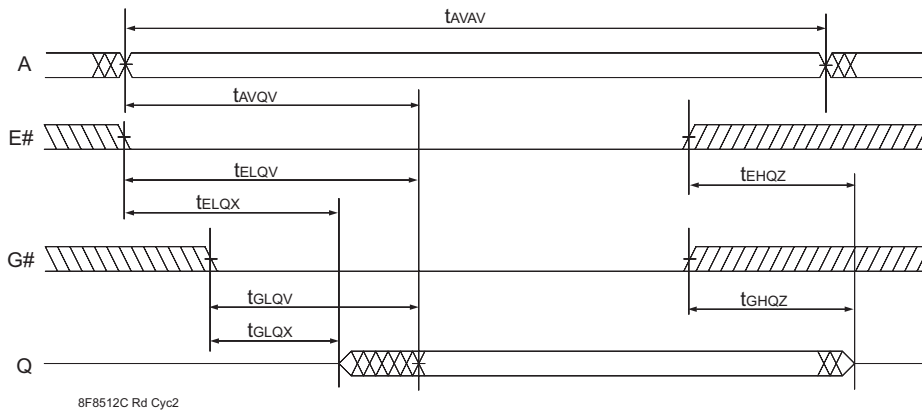
Parameter	Symbol		20ns		25ns		35ns		Units
	JEDEC	Alt.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t <sub>AVAV</sub>	t <sub>RC</sub>	20		25		35		ns
Address Access Time	t <sub>AVQV</sub>	t <sub>AA</sub>		20		25		35	ns
Chip Enable Access Time	t <sub>ELQV</sub>	t <sub>ACS</sub>		20		25		35	ns
Chip Enable to Output in Low Z (1)	t <sub>ELQX</sub>	t <sub>CLZ</sub>	3		3		3		ns
Chip Disable to Output in High Z (1)	t <sub>EHQZ</sub>	t <sub>CHZ</sub>		10		12		15	ns
Output Hold from Address Change	t <sub>AVQX</sub>	t <sub>OH</sub>	3		3		3		ns
Output Enable to Output Valid	t <sub>GLQV</sub>	t <sub>OE</sub>		13		15		20	ns
Output Enable to Output in Low Z (1)	t <sub>GLQX</sub>	t <sub>OLZ</sub>	0		0		0		ns
Output Disable to Output in High Z (1)	t <sub>GHQZ</sub>	t <sub>OHZ</sub>		8		10		12	ns

Note: Parameter guaranteed, but not tested.

**FIG. 3 READ CYCLE 1 - W# HIGH, G#, E# LOW**



**FIG. 4 READ CYCLE 2 - W# HIGH**





**AC CHARACTERISTICS READ CYCLE**

Parameter	Symbol		55ns		70ns		85ns		100ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tAVAV	tRC	55		70		85		100		ns
Address Access Time	tAVQV	tAA		55		70		85		100	ns
Chip Enable Access Time	tELQV	tACS		55		70		85		100	ns
Chip Enable to Output in Low Z (1)	tELQX	tCLZ	5		5		5		5		ns
Chip Disable to Output in High Z (1)	tEHQZ	tCHZ		30		30		35		40	ns
Output Hold from Address Change	tAVQX	tOH	3		3		3		3		ns
Output Enable to Output Valid	tGLQV	tOE		40		40		45		50	ns
Output Enable to Output in Low Z (1)	tGLQX	tOLZ	0		0		0		0		ns
Output Disable to Output in High Z (1)	tGHQZ	tOHZ		30		30		35		40	ns

Note 1: Parameter guaranteed, but not tested.

**AC CHARACTERISTICS WRITE CYCLE**

Write Cycle Parameter	Symbol		20ns		25ns		35ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	20		25		35		ns
Chip Enable to End of Write	tELWH	tCW	15		20		30		ns
	tELEH	tCW	15		20		30		ns
Address Setup Time	tAVWL	tAS	0		0		0		ns
	tAVEL	tAS	0		0		0		ns
Address Valid to End of Write	tAVWH	tAW	15		20		30		ns
	tAVEH	tAW	15		20		30		ns
Write Pulse Width	tWLWH	tWP	15		20		25		ns
	tWLEH	tWP	15		20		25		ns
Write Recovery Time	tWHAX	tWR	0		0		0		ns
	tEHAX	tWR	0		0		0		ns
Data Hold Time	tWHDX	tDH	3		3		3		ns
	tEHDX	tDH	3		3		3		ns
Write to Output in High Z (1)	tWLQZ	tWHZ	0	10	0	12	0	15	ns
Data to Write Time	tDVWH	tDW	12		15		20		ns
	tDVEH	tDW	12		15		20		ns
Output Active from End of Write (1)	tWHQX	tWLZ	3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

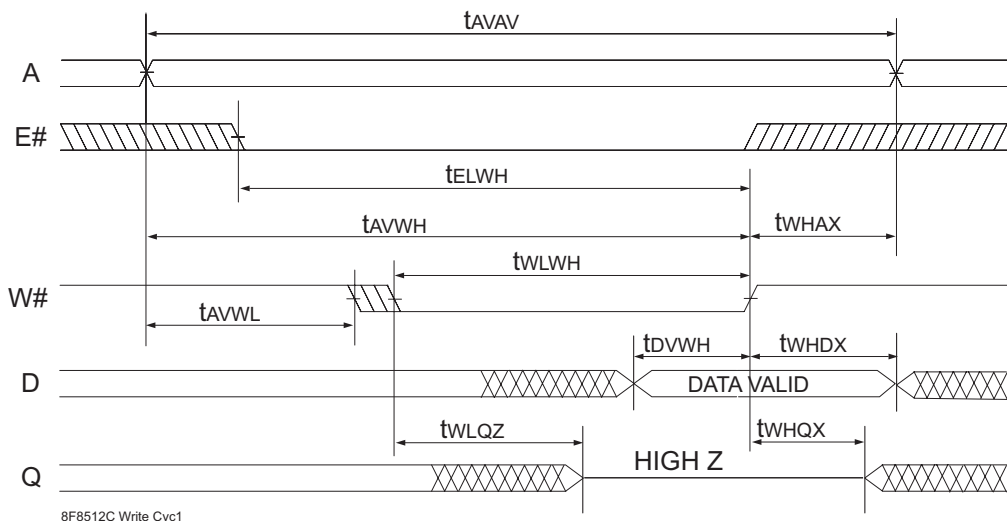


**AC CHARACTERISTICS WRITE CYCLE**

Parameter	Symbol		55ns		70ns		85ns		100ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>AVAV</sub>	t <sub>WC</sub>	55		70		85		100		ns
Chip Enable to End of Write	t <sub>ELWH</sub>	t <sub>CW</sub>	50		65		70		80		ns
	t <sub>LEH</sub>	t <sub>CW</sub>	50		65		70		80		ns
Address Setup Time	t <sub>AVWL</sub>	t <sub>AS</sub>	0		0		0		0		ns
	t <sub>AVEL</sub>	t <sub>AS</sub>	0		0		0		0		ns
Address Valid to End of Write	t <sub>AVWH</sub>	t <sub>AW</sub>	50		65		70		80		ns
	t <sub>AVEH</sub>	t <sub>AW</sub>	50		65		70		80		ns
Write Pulse Width	t <sub>WLWH</sub>	t <sub>WP</sub>	50		65		70		80		ns
	t <sub>WLEH</sub>	t <sub>WP</sub>	50		65		70		80		ns
Write Recovery Time	t <sub>WHAX</sub>	t <sub>WR</sub>	0		0		0		0		ns
	t <sub>EHAX</sub>	t <sub>WR</sub>	0		0		0		0		ns
Data Hold Time	t <sub>WHDX</sub>	t <sub>DH</sub>	0		0		0		0		ns
	t <sub>EHDX</sub>	t <sub>DH</sub>	0		0		0		0		ns
Write to Output in High Z (1)	t <sub>WLQZ</sub>	t <sub>WHZ</sub>	0	30	0	30	0	35	0	40	ns
Data to Write Time	t <sub>DVWH</sub>	t <sub>DW</sub>	30		30		35		40		ns
	t <sub>DVEH</sub>	t <sub>DW</sub>	30		30		35		40		ns
Output Active from End of Write (1)	t <sub>WHQX</sub>	t <sub>WLZ</sub>	5		5		3		5		ns

Note 1: Parameter guaranteed, but not tested.

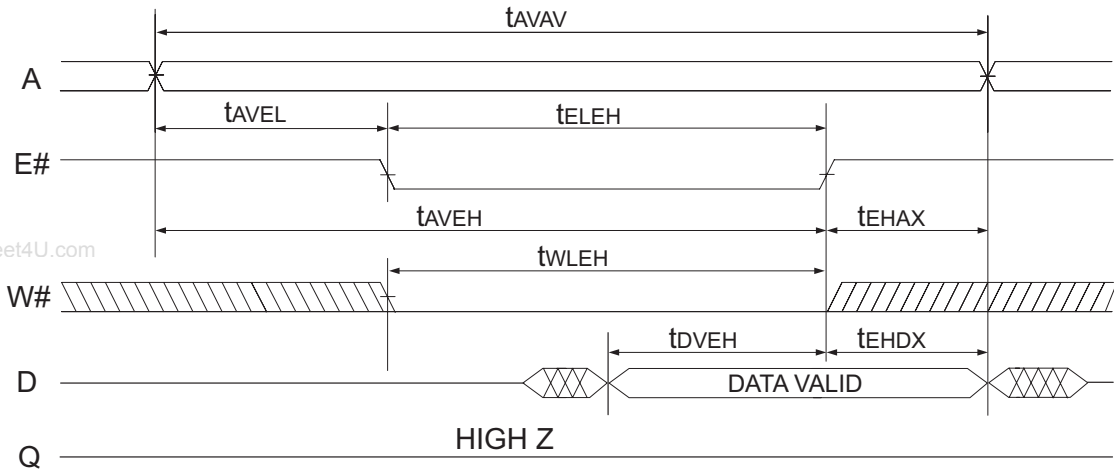
**FIG. 7 WRITE CYCLE 1 - W# CONTROLLED**



8F8512C Write Cyc1



FIG. 8 WRITE CYCLE 2 - E# CONTROLLED



8F8512C Write Cyc2



**DATA RETENTION CHARACTERISTICS**

*LP 70-100ns Only*

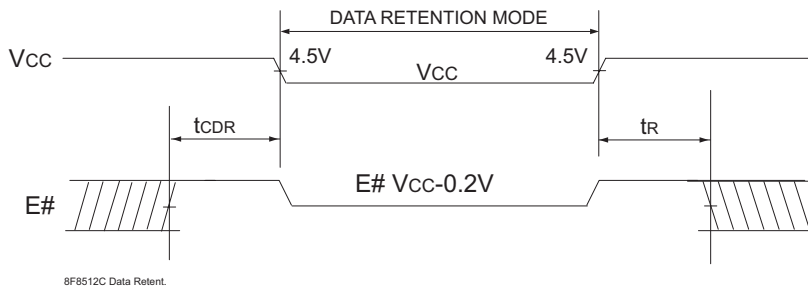
Characteristic	Sym	Test Conditions	V <sub>CC</sub>	Min	Typ	Max		Unit
						70°C	85°C	
Data Retention Voltage	V <sub>CC</sub>	V <sub>CC</sub> = 0.2V		2	-	-	-	V
Data Retention Quiescent Current	I <sub>CCDR</sub>	E# ≥ V <sub>CC</sub> - 0.2V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V	2V	-	10	125	185	μA
			3V	-	20	200	250	μA
Chip Disable to Data Retention Time (1)	t <sub>CDR</sub>			0	-	-	-	ns
Operation Recovery Time (1)	t <sub>R</sub>			t <sub>AVAV</sub> *	-	-	-	ns

\*Read Cycle Time

Note: Parameter guaranteed, but not tested.

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**FIG. 9 DATA RETENTION E# CONTROLLED**



**ORDERING INFORMATION**

Standard Power	Speed (ns)	Package No.
EDI8F8512C20M6C	20	183
EDI8F8512C25M6C	25	183
EDI8F8512C35M6C	35	183
EDI8F8512C70BSC	70	63
EDI8F8512C85BSC	85	63
EDI8F8512C100BSC	100	63
EDI8F8512C55B6C	55	91
EDI8F8512C70B6C	70	91
EDI8F8512C85B6C	85	91
EDI8F8512C100B6C	100	91

Low Power with Data Retention	Speed (ns)	Package Leads
EDI8F8512LP70BSC	70	63
EDI8F8512LP85BSC	85	63
EDI8F8512LP100BSC	100	63
EDI8F8512LP70B6C	70	91
EDI8F8512LP85B6C	85	91
EDI8F8512LP100B6C	100	91

Note:

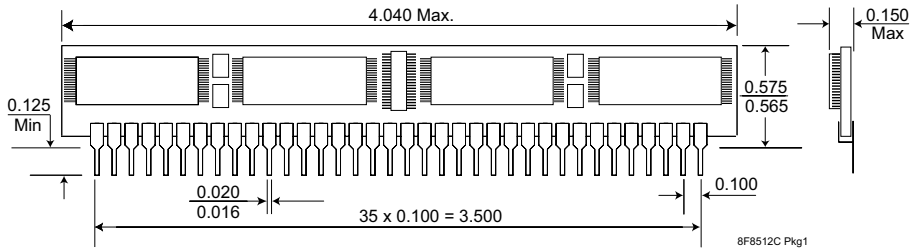
To order an Industrial grade product substitute the letter C in the Suffix with the letter I, e.g., EDI8F8512C70B6C becomes EDI8F8512C70B6I.





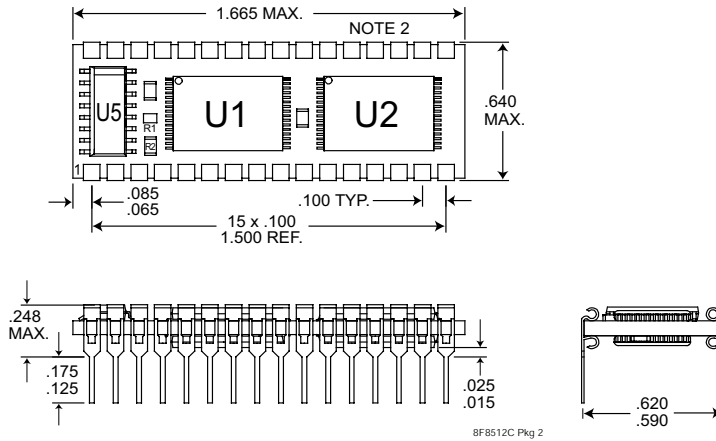
PACKAGE DESCRIPTIONS

PACKAGE NO. 63: 36 PIN SINGLE-IN-LINE PACKAGE

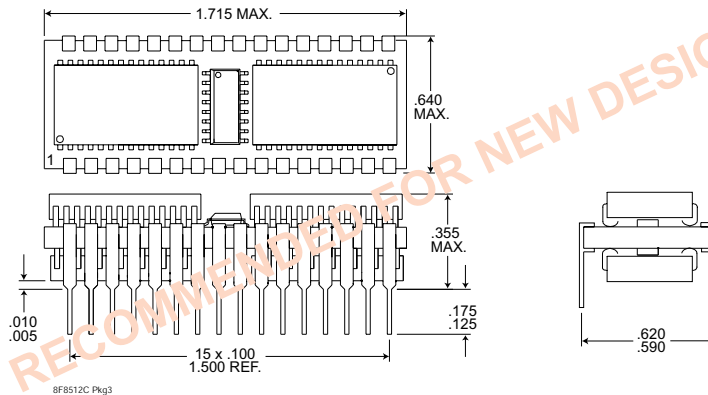


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PACKAGE NO. 91: 32 PIN DUAL-IN-LINE PACKAGE



PACKAGE NO. 183: 32 PIN DUAL-IN-LINE PACKAGE



NOT RECOMMENDED FOR NEW DESIGNS

ALL DIMENSIONS ARE IN INCHES