64Kx16 Static RAM CMOS, Module

The EDI8M1664C is a high speed 64Kx16 CMOS Static RAM Module consisting of four (4) 32Kx8 CMOS Static RAMs in leadless chip carriers, surface mounted onto a multi-layered ceramic substrate. The 32Kx8 RAMs are organized as two banks of 32Kx16 bits each. Functional equivalence to proposed monolithic megabit Static RAMs is achieved with an on-board decoder that interprets the higher order address (A15) to select one of the two banks as the x16 output, and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for Lower Byte (DQØ-DQ7) and Upper Byte (DQ8-DQ15) control, respectively.

The EDI8M81664C is available with access times as fast as 50ns.

Fully asynchronous circuitry requires no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

EDI Military Modules are constructed using semiconductor components which have been 100% processed to the test methods of MIL-STD-883C, Class B., making them ideally suited to applications demanding the highest level of performance and reliability.

Features

64Kx16 bit CMOS Static Random Access Memory Module

- Access Times 50, 60, 70, 85, and 100ns
- Fully Static, No Clocks
- Inputs and Outputs Directly TTL Compatible
- Data Retention Function

Jedec Approved Pinout

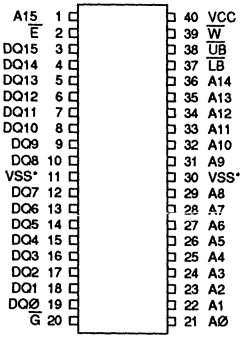
- 40 Pin Ceramic Dual-in-line Package

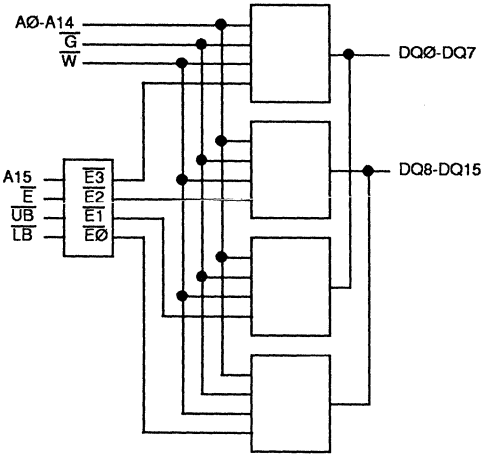
Single +5V (±10%) Supply Operation

Pin Names

AØ-A15	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ15	Data Input/ Output
$\overline{UB}$	Upper Byte Control
$\overline{LB}$	Lower Byte Control
VCC	Power (+5V±10%)
VSS	Ground

Pin Configuration and Block Diagram





*Note: Both ground pins (VSS) need to be grounded for proper operation.

Absolute Maximum Ratings*

Voltage on any pin relative to VSS .....-0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial..... 0°C to +70°C.
Industrial.....-40°C to +85°C
Military..... -55°C to +125°C
Storage Temperature (Ambient/Ceramic). -65°C to +150°C
Power Dissipation.....4 Watts
Output Current..... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels. .....VSS to 3.0V
Input Rise and Fall Times. 5ns
Input and Output Timing Levels 1.5V
Output Load.: 50/70ns. .....1TTL, CL = 30pF
. 85/100ns.....1TTL, CL = 100pF
(Note: For TEHQZ, TGHQZ, and TWLQZ, CL = 5pF.)

DC Electrical Characteristics

(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions	Min	Typ*	Max		Units
					50/70	85/100	
Operating Power Supply Current, x16 mode	ICC1	$\overline{W}$, $\overline{E}$, $\overline{LB}$, $\overline{UB}$ = VIL, II/O = 0mA, Min Cycle	--	170	240	195	mA
Operating Power Supply Current, x8 mode	ICC1	$\overline{E}$ = VIL; $\overline{LB}$ or $\overline{UB}$ =VIL; II/O = 0mA, Min Cycle	--	115	160	120	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH or $\overline{LB}$ & $\overline{UB}$ ≥ VIL	--	50	95	75	mA
Full Standby (CMOS) Power Supply Current	ICC3	$\overline{E}$ ≥ VCC- 0.2V or $\overline{LB}$ & $\overline{UB}$ ≥ VCC-0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V	--	1	10	3	mA
Input Leakage Current	IIL	VIN = 0V to VCC	--	--	±10		µA
Output Leakage Current	IOL	V I/O = 0V to VCC	--	--	±10		µA
Output High Voltage	VOH	IOH = -1.0mA	2.4	--	--		V
Output Low Voltage	VOL	IOL = 2.1mA	--	--	0.4		V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{UB}$	$\overline{LB}$	$\overline{W}$	$\overline{G}$	Mode	Output	Power
H	X	H	X	X	Standby	HIGH Z	ICC2, ICC3
L	H	H	X	X	Standby	HIGH Z	ICC2, ICC3
L	X	X	H	H	Read, Output Deselect	HIGH Z	ICC1
L	L	H	L	X	$\overline{UB}$ Write	DIN(8-15)	ICC1
L	H	L	L	X	$\overline{LB}$ Write	DIN(0-7)	ICC1
L	L	L	L	X	Write	DIN(0-15)	ICC1
L	L	H	H	L	$\overline{UB}$ Read	DOUT(8-15)	ICC1
L	H	L	H	L	$\overline{LB}$ Read	DOUT(0-7)	ICC1
L	L	L	H	L	Read	DOUT(0-15)	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Pins	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	$\overline{G}$,A	CI	60	pF
Capacitance Control (DQ Pins)	CD/Q	CD/Q	30	pF
Input Capacitance Control Lines	$\overline{E}$, $\overline{UB}$, $\overline{LB}$	CC	30	pF
Input Capacitance $\overline{W}$ Line	$\overline{W}$	CW	50	pF

These parameters are sampled, not 100% tested.

AC Characteristics

Read Cycle

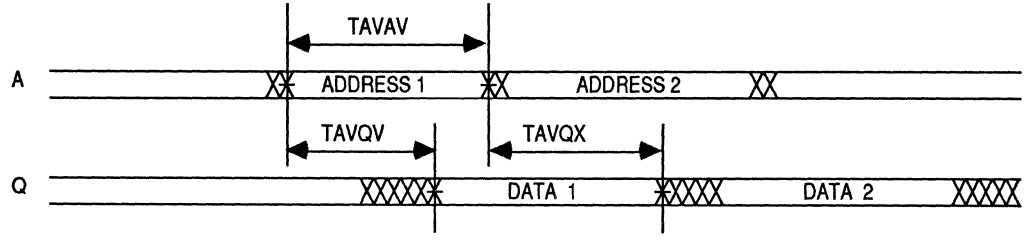
(TA = -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Symbol	50ns*		60ns		70ns		85ns		100ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	50		60		70		85		100		ns
Address Access Time	TAVQV		50		60		70		85		100	ns
Chip EnableAccess Time	TELQV $\overline{E}$		50		60		70		85		100	ns
Chip Enable to Output in Low Z (1)	TELQX $\overline{E}$	30		30		30		30		30		ns
Output Enable to Output Valid	TGLQV		30		35		40		50		60	ns
Output Enable to Output in Low Z (1)	TGLQX	5		5		5		5		5		ns
Chip Enable to Output in High Z (1)	TEHQZ $\overline{E}$		35		35		35		40		45	ns
Output Enable to Output in High Z (1)	TGHQZ		35		35		35		40		40	ns
Output Hold from Address Change	TAVQX	10		10		10		10		10		ns

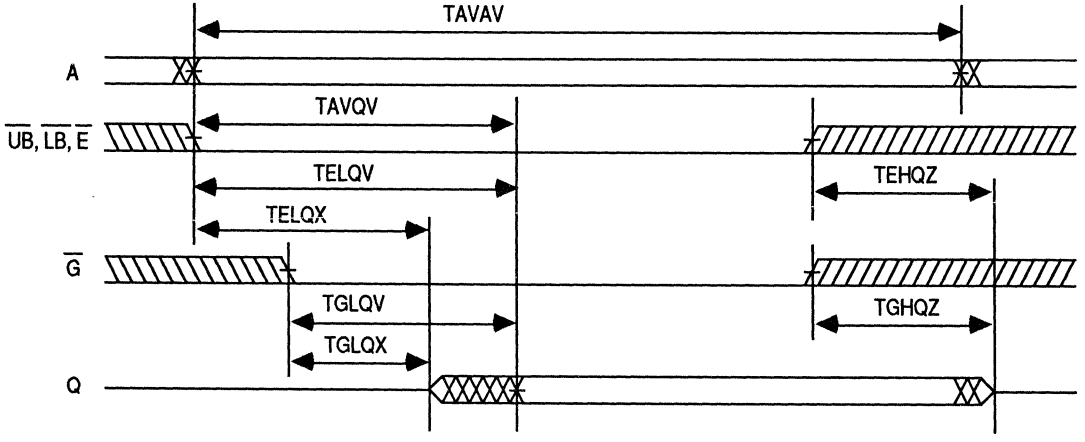
Note 1: Parameter guaranteed, but not tested.

*Preliminary data.

Read Cycle 1
$\overline{W}$ High; $\overline{G}$, $\overline{E}$ Low



Read Cycle 2
$\overline{W}$ High



AC Characteristics
Write Cycle

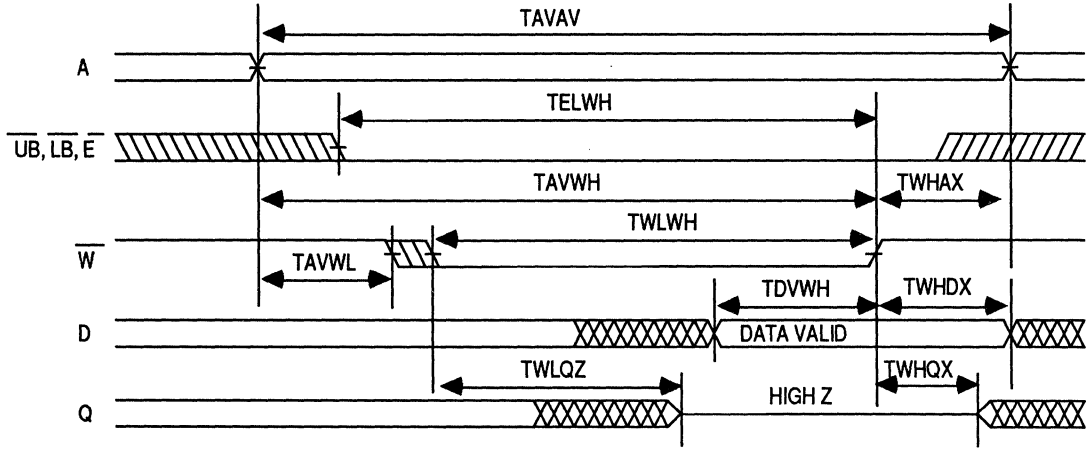
(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Symbol		50ns*		60ns		70ns		85ns		100ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		50		60		70		85		100		ns
Chip Enable to	TELWH	$\overline{W}$	45		50		65		70		80		ns
End of Write	TWLEH	$\overline{E}$	45		50		65		70		80		ns
Address Setup Time	TAVWL	$\overline{W}$	10		10		10		10		10		ns
	TAVEL	$\overline{E}$	10		10		10		10		10		ns
Address Valid to	TAVWH	$\overline{W}$	40		50		65		70		80		ns
End of Write	TAVEH	$\overline{E}$	40		50		65		70		80		ns
Write Pulse Width	TWLWH	$\overline{W}$	35		45		55		55		70		ns
	TELEH	$\overline{E}$	35		45		55		55		70		ns
Write Recovery Time	TWHAX	$\overline{W}$	5		5		5		5		5		ns
	TEHAX	$\overline{E}$	5		5		5		5		5		ns
Data Hold Time	TWHDX	$\overline{W}$	5		5		5		5		5		ns
	TEHDX	$\overline{E}$	5		5		5		5		5		ns
Write to Output in High Z (1)	TWLQZ		0	25	0	25	0	30	0	45	0	50	ns
Data to Write Time	TDVWH	$\overline{W}$	25		25		30		35		35		ns
	TDVEH	$\overline{E}$	25		25		30		35		35		ns
Output Active from End of Write (1)	TWHQX		0		0		0		0		0		ns

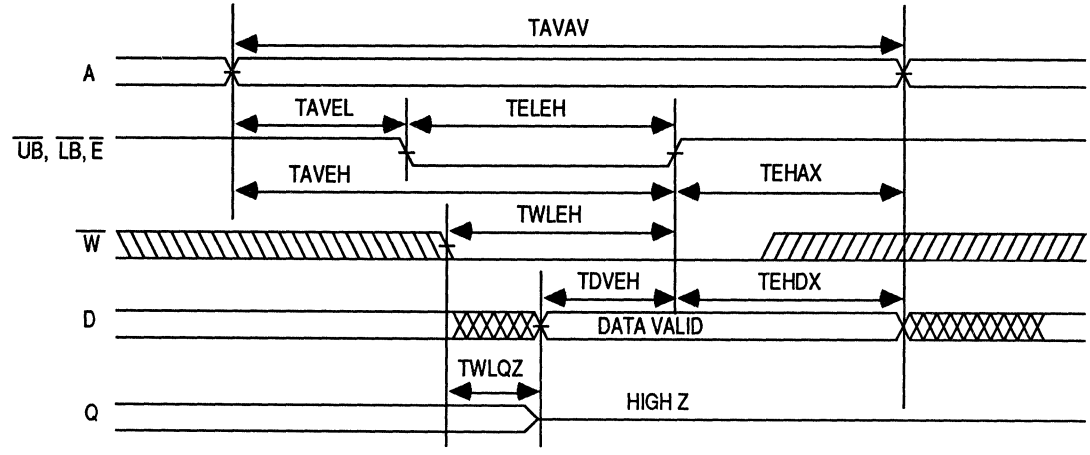
Note 1: Parameter guaranteed, but not tested.

*Preliminary data.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled



Data Retention Characteristics

(TA = 0°C to +70°C or -55°C to +125°C)

Characteristic	Sym	Test Conditions	Min	Typ	Max		Unit
					50/70	85/100	
Data Retention Voltage	VDD	VDD = 2.0V	2.0	--	--		V
Data Retention Quiescent Current	ICCDR	$\overline{E}$≥ VDD -0.2V	--	300	2500	1500	µA
Chip Disable to Data Retention Time	TCDR	VIN ≥VDD -0.2V	0	--	--	--	ns
Operation Recovery Time	TR	or VIN ≤0.2V	TAVAV*	--	--	--	ns

*Read Cycle Time

Data Retention
$\overline{E}$ Controlled