64Kx16 Static RAM CMOS, Module

PRELIMINARY
T-46-23-14

The EDI8M1664C/LP/P is a high speed 64Kx16 CMOS Static RAM module consisting of four (4) 32Kx8 CMOS Static RAMs surface mounted onto a multi-layered substrate.

The 32Kx8 RAMs are organized as two banks of 32Kx16 bits each. Functional equivalence to the proposed monolithic megabit Static RAM is achieved with an on-board decoder that interprets the higher order address (A15) to select one of the two banks as the x16 output, and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for Lower Byte (DQØ-DQ7) and Upper Byte (DQ8-DQ15) control, respectively.

All outputs and inputs are TTL-compatible and operate from a +5V supply. Fully asynchronous circuitry requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

Two Low Power versions (P & LP) are available for Military applications. The LP version features a data retention function for battery backed-up applications.

EDI's Military modules are constructed using RAMs which are compliant to MIL-STD-883, Paragraph 1.2.1.

Features

64Kx16 bit CMOS Static Random Access Memory Module

- Access Times
  45, 55, 70, 85 and 100ns
- Data Retention Function (LP Version)
- Fully Static, No Clocks
- Inputs and Outputs Directly TTL Compatible

Jedec Approved 40 Pin DIP Pinout

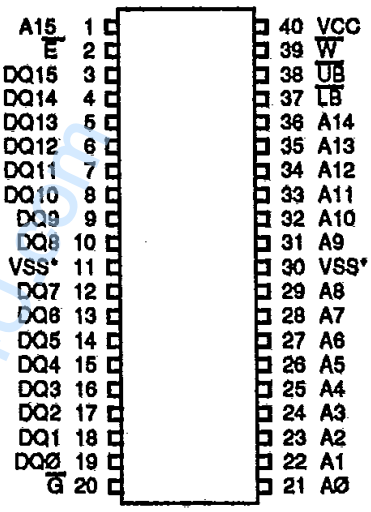
- Ceramic LCCs on Ceramic Substrate, No. 66

Single +5V (±10%) Supply Operation

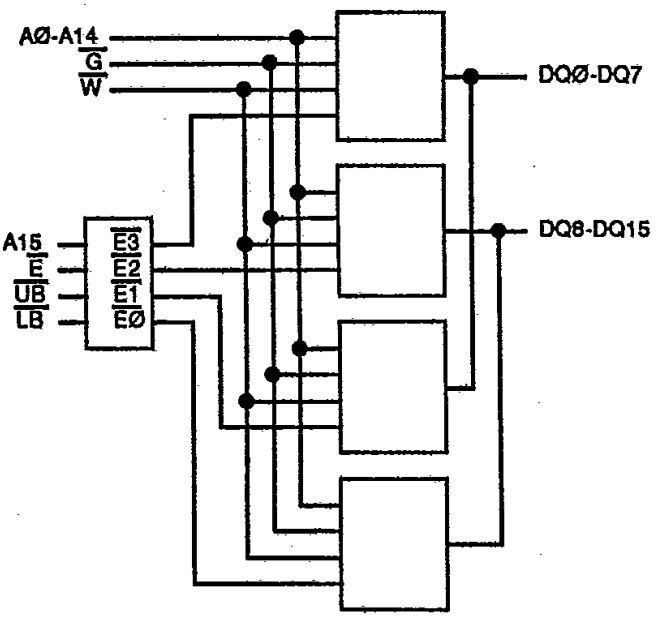
Pin Names

AØ-A15	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ15	Data Input/Output
$\overline{UB}$	Upper Byte Control
$\overline{LB}$	Lower Byte Control
VCC	Power (+5V±10%)
VSS	Ground

Pin Configurations and Block Diagram



*Note: Both ground pins (VSS) need to be grounded for proper operation.



Absolute Maximum Ratings*

Voltage on any pin relative to VSS ..... -0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial ..... 0°C to +70°C
Industrial ..... -40°C to +85°C
Military ..... -55°C to +125°C
Storage Temperature,Ceramic ..... -65°C to +150°C
Power Dissipation ..... 4 Watts
Output Current ..... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

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AC Test Conditions

Input Pulse Levels ..... VSS to 3.0V
Input Rise and Fall Times 5ns
Input and Output Timing Levels 1.5V
Output Load 45/70ns ..... 1TTL, CL = 30pF
85/100ns ..... 1TTL, CL = 100pF
(Note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ*	Max		Unit
					45/70	85/100	
Operating Power Supply Current, x16 mode	ICC1	$\overline{W}$, $\overline{E}$, $\overline{LB}$, $\overline{UB}$ = VIL, I/O = 0mA, Min Cycle	--	170	280	195	mA
Operating Power Supply Current, x8 mode	ICC1	$\overline{W}$, $\overline{E}$ = VIL; $\overline{LB}$ or $\overline{UB}$ =VIL; I/O = 0mA, Min Cycle	--	115	220	120	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH or $\overline{LB}$ & $\overline{UB}$ ≥ VIH	--	50	180	80	mA
Full Standby (CMOS) Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V or $\overline{LB}$ & $\overline{UB}$ ≥ VCC-0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V	--	1	25	15	mA
Input Leakage Current	ILI	VIN = 0V to VCC	--	--	±10		µA
Output Leakage Current	ILO	V I/O = 0V to VCC	--	--	±10		µA
Output High Voltage	VOH	IOH = -1.0mA	2.4	--	--		V
Output Low Voltage	VOL	IOL = 2.1mA	--	--	0.4		V

*Typical = TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{UB}$	$\overline{LB}$	$\overline{W}$	$\overline{G}$	Mode	Output	Power
H	X	H	X	X	Standby	HIGH Z	ICC2, ICC3
L	H	H	X	X	Standby	HIGH Z	ICC2, ICC3
L	X	X	H	H	Read, Output Deselect	HIGH Z	ICC1
L	L	H	L	X	UB Write	DIN(8-15)	ICC1
L	H	L	L	X	LB Write	DIN(0-7)	ICC1
L	L	L	L	X	Standby	DIN(0-15)	ICC1
L	L	H	H	L	Standby	DOUT(8-15)	ICC1
L	H	L	H	L	Standby	DOUT(0-7)	ICC1
L	L	L	H	L	Standby	DOUT(0-15)	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Pins	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	G,A	CI	60	pF
Capacitance Control (DQ Pins)	CD/Q	CD/Q	30	pF
Input Capacitance Control Lines	$\overline{E}$, $\overline{UB}$, $\overline{LB}$	CC	30	pF
Input Capacitance $\overline{W}$ Line	$\overline{W}$	CW	50	pF

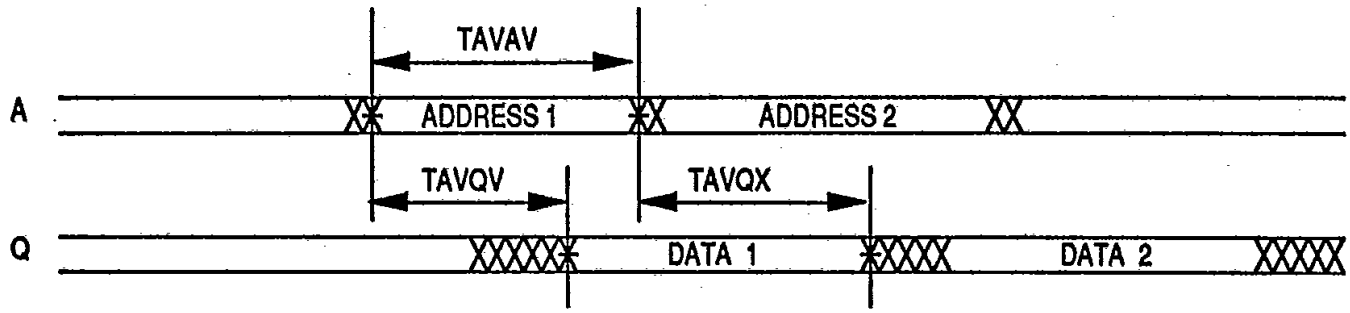
These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle

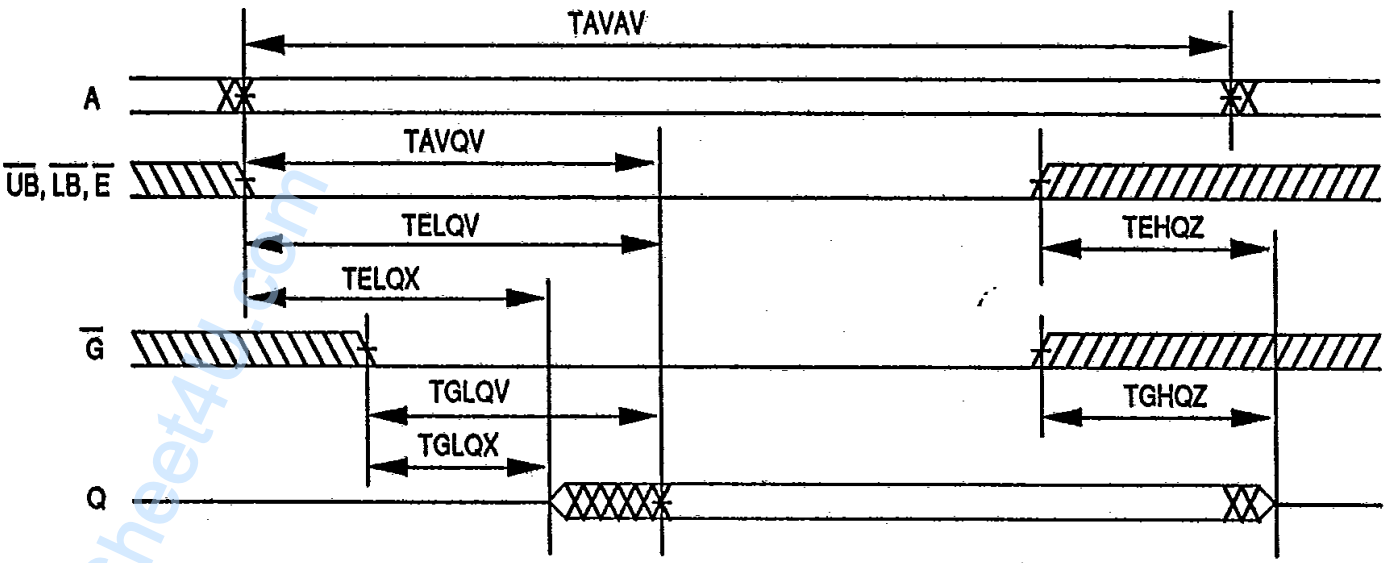
Parameter	Symbol			45ns		55ns		Units
				Min	Max	Min	Max	
Read Cycle Time	TAVAV			45		55		ns
Address Access Time	TAVQV				45		55	ns
Chip EnableAccess Time	TELQV	$\overline{E}$			45		55	ns
Chip Enable to Output In Low Z (1)	TELQX	$\overline{E}$		5		5		ns
Output Enable to Output Valid	TGLQV				20		25	ns
Output Enable to Output In Low Z (1)	TGLQX			3		3		ns
Chip Enable to Output In High Z (1)	TEHQZ	$\overline{E}$			20		25	ns
Output Enable to Output In High Z (1)	TGHQZ				20		25	ns
Output Hold from Address Change	TAVQX			5		5		ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
$\overline{W}$ High; $\overline{G}$, $\overline{E}$ Low



Read Cycle 2
$\overline{W}$ High



AC Characteristics
Read Cycle

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Parameter	Symbol			70ns		85ns		100ns		Units
				Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV			70		85		100		ns
Address Access Time	TAVQV				70		85		100	ns
Chip EnableAccess Time	TELQV	$\overline{E}$			70		85		100	ns
Chip Enable to Output In Low Z (1)	TELQX	$\overline{E}$		5		5		5		ns
Output Enable to Output Valid	TGLQV				35		35		50	ns
Output Enable to Output In Low Z (1)	TGLQX			0		0		0		ns
Chip Enable to Output In High Z (1)	TEHQZ	$\overline{E}$			35		35		35	ns
Output Enable to Output In High Z (1)	TGHQZ				35		35		35	ns
Output Hold from Address Change	TAVQX			3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

AC Characteristics
Write Cycle

Parameter	Symbol			45ns		55ns		Units
				Min	Max	Min	Max	
Write Cycle Time	TAVAV			45		55		ns
Chip Enable to End of Write	TWLWH	$\overline{W}$		40		50		ns
	TWLEH	$\overline{E}$		40		50		ns
Address Setup Time	TAVWL	$\overline{W}$		0		0		ns
	TAVEL	$\overline{E}$		0		0		ns
Address Valid to End of Write	TAVWH	$\overline{W}$		40		50		ns
	TAVEH	$\overline{E}$		40		50		ns
Write Pulse Width	TWLWH	$\overline{W}$		25		25		ns
	TELEH	$\overline{E}$		25		25		ns
Write Recovery Time	TWHAX	$\overline{W}$		0		0		ns
	TEHAX	$\overline{E}$		0		0		ns
Data Hold Time	TWHDX	$\overline{W}$		0		0		ns
	TEHDX	$\overline{E}$		0		0		ns
Write to Output In High Z (1)	TWLQZ			0	20	0	25	ns
Data to Write Time	TDVWH	$\overline{W}$		20		25		ns
	TDVEH	$\overline{E}$		20		25		ns
Output Active from End of Write (1)	TWHQX			5		5		ns

Note 1: Parameter guaranteed, but not tested.

AC Characteristics
Write Cycle

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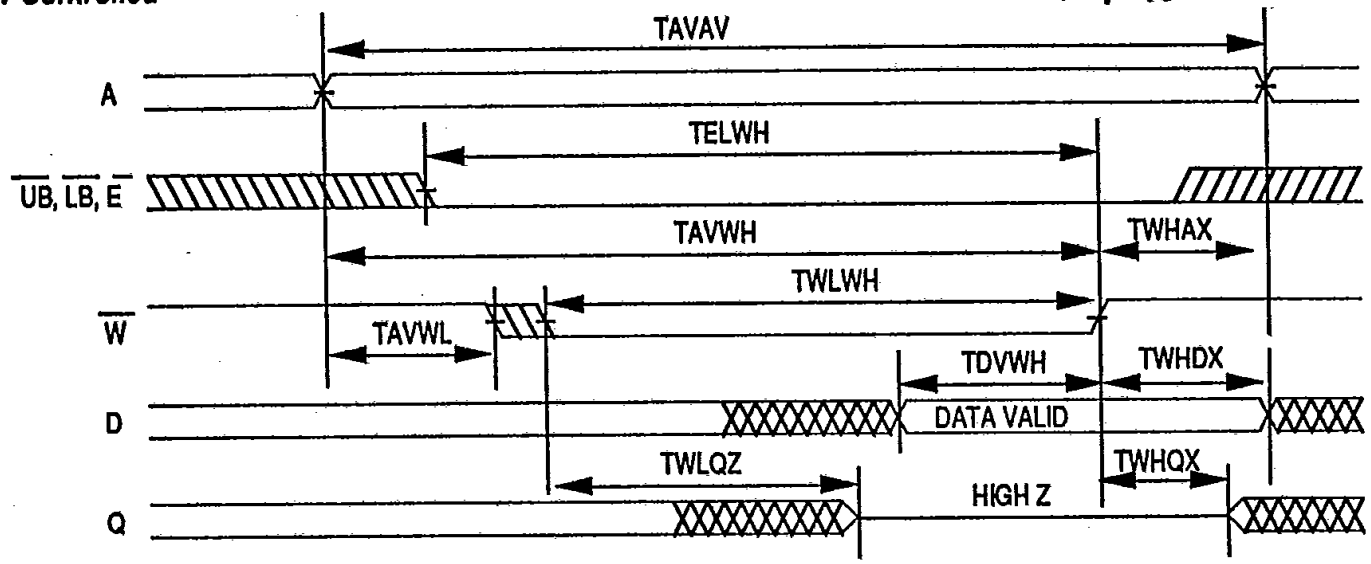
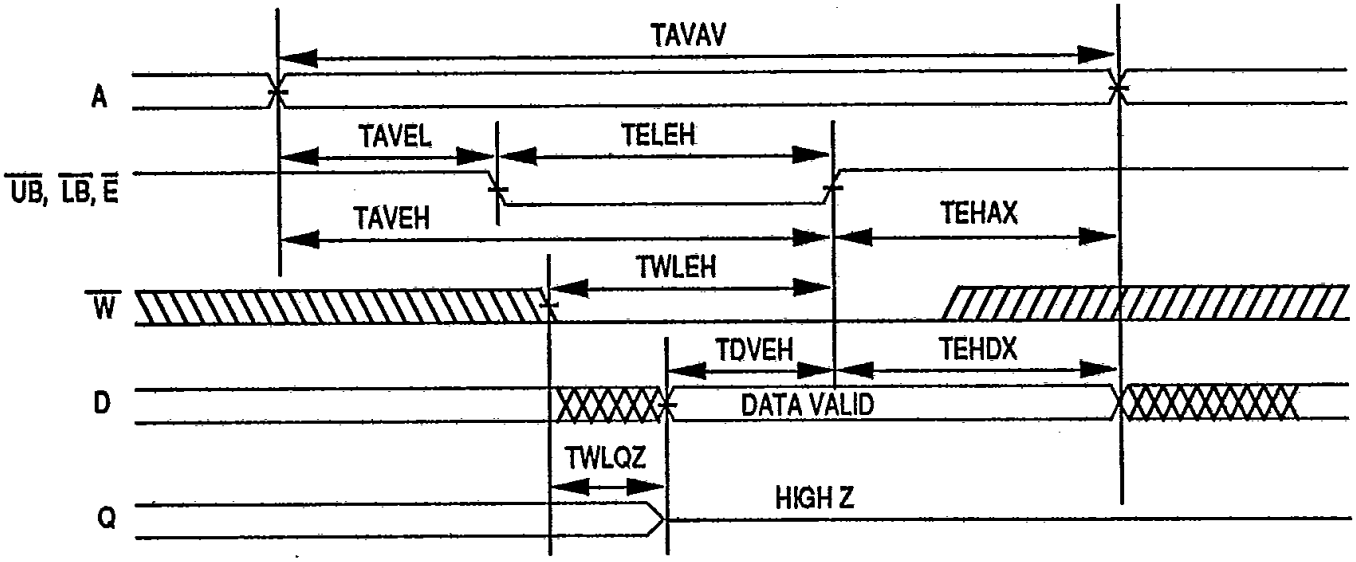
Parameter	Symbol			70ns Min	70ns Max	85ns Min	85ns Max	100ns Min	100ns Max	Units
Write Cycle Time	TAVAV			70		85		100		ns
Chip Enable to	TWLWH	$\overline{W}$		60		70		80		ns
End of Write	TWLEH	$\overline{E}$		60		70		80		ns
Address Setup Time	TAVWL	$\overline{W}$		0		0		0		ns
	TAVEL	$\overline{E}$		0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$		60		70		80		ns
End of Write	TAVEH	$\overline{E}$		60		70		80		ns
Write Pulse Width	TWLWH	$\overline{W}$		45		50		70		ns
	TELEH	$\overline{E}$		45		50		70		ns
Write Recovery Time	TWHAX	$\overline{W}$		0		0		0		ns
	TEHAX	$\overline{E}$		0		0		0		ns
Data Hold Time	TWHDX	$\overline{W}$		3		3		3		ns
	TEHDX	$\overline{E}$		3		3		3		ns
Write to Output In High Z (1)	TWLQZ			0	40	0	45		50	ns
Data to Write Time	TDVWH	$\overline{W}$		30		35		35		ns
	TDVEH	$\overline{E}$		30		35		35		ns
Output Active from End of Write (1)	TWHQX			3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled



Data Retention Characteristics

LP Version Only
EDI8M1664LP, 85 and 100ns only

Characteristic	Sym	Test Conditions	Min	Typ	Max 85/100	Unit
Data Retention Voltage	VDD	VCC = 2.0V	2.0	--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E} \geq$ VDD - 0.2V	--	--	2500	µA
Chip Disable to Data Retention Time	TCDR	VIN ≥ VDD -0.2V	0	--	--	ns
Operation Recovery Time	TR	or VIN ≤ 0.2V	5	--	--	ms

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Data Retention
$\overline{E}$ Controlled