64Kx16 CMOS, High Speed Programmable, Static RAM Module

The EDI8M1665C is a 1024K-bit high speed CMOS Static RAM Module consisting of four (4) 64Kx4 Static RAMs in leadless chip carriers surface-mounted onto a multilayered ceramic substrate. Four Chip Select lines (one for each 64Kx4) allow the user to configure the memory into a 64Kx16, 128Kx8 or 256Kx4 organizations.

The EDI8M1665C is available with access times as fast as 35ns. The high density module, a 40 pin sidebrazed DIP on 900 mil centers, is a pin for pin replacement for EDI's EDH816H64C module.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Dual ground pins are provided for maximum noise immunity.

Fully asynchronous circuitry requires no clocks or refreshing for operation.

EDI Military Modules are constructed using semiconductor components which are compliant to MIL-STD-883, paragraph 1.2.1.

Features

High Density 1024K-bit CMOS Static Random Access Memory Module

- Access Times 35, 45, 55, and 70ns
- Fully Static, No Clocks
- Inputs and Outputs Directly TTL Compatible
- Customer Configured Memory, as 64Kx16, 128Kx8 or 256Kx4

40 Pin Dual-in-line Package, No. 98

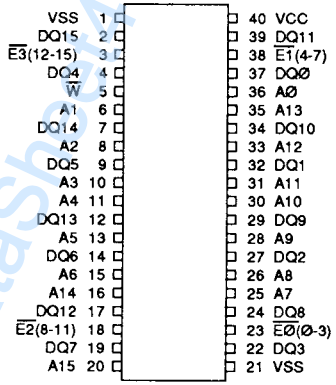
- Dual Ground Pins for Maximum Noise Immunity

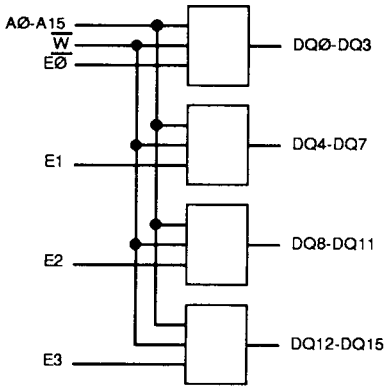
Single +5V (±10%) Supply Operation

Pin Names

AØ-A15	Address Inputs
$\overline{E}$Ø-$\overline{E}$3	Chip Enables
$\overline{W}$	Write Enable
DQØ-DQ15	Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Pin Configuration and Block Diagram





Absolute Maximum Ratings*

Voltage on any pin relative to VSS ..... -0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial ..... 0°C to+70°C
Industrial ..... -40°C to +85°C
Military ..... -55°C to +125°C
Storage Temperature, Ceramic ..... -65°C to +150°C
Power Dissipation ..... 8 Watts
Output Current ..... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels ..... VSS to 3.0V
Input Rise and Fall Times 5ns
Input and Output Timing Levels 1.5V
Output Load ..... 1TTL, CL = 30pF
(note: For TEHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Mode	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	x16	--	320	480	mA
			x8	--	165	280	
			x4	--	85	180	
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH, VIN ≤ VIL or VIN ≥ VIH		--	10	120	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V		--	5	80	mA
Input Leakage Current	ILI	VIN = 0V to VCC		--	--	±10	µA
Output Leakage Current	ILO	V I/O = 0V to VCC		--	--	±10	µA
Output High Voltage	VOH	IOH = -4.0mA		2.4	--	--	V
Output Low Voltage	VOL	IOL = 8.0mA		--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{E}$	$\overline{W}$	Mode	Output	Power
H	X	Standby	HIGH Z	ICC2, ICC3
L	H	Read	DOUT	ICC1
L	L	Write	HIGH Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Units
Input Capacitance (Address, $\overline{W}$)	CI	40	pF
Input Capacitance Enable Line ($\overline{E}$)	CE	12	pF
Capacitance (DQ Lines)	CO	16	pF

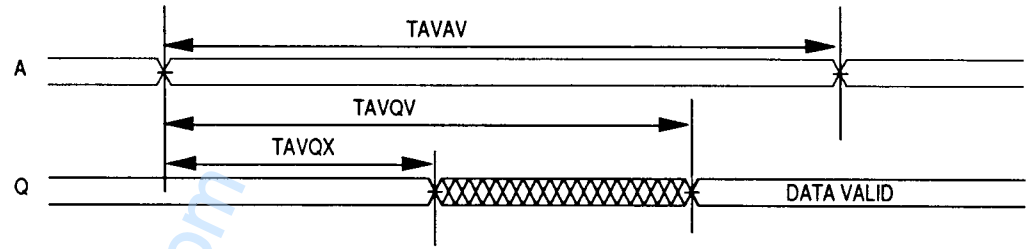
These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle

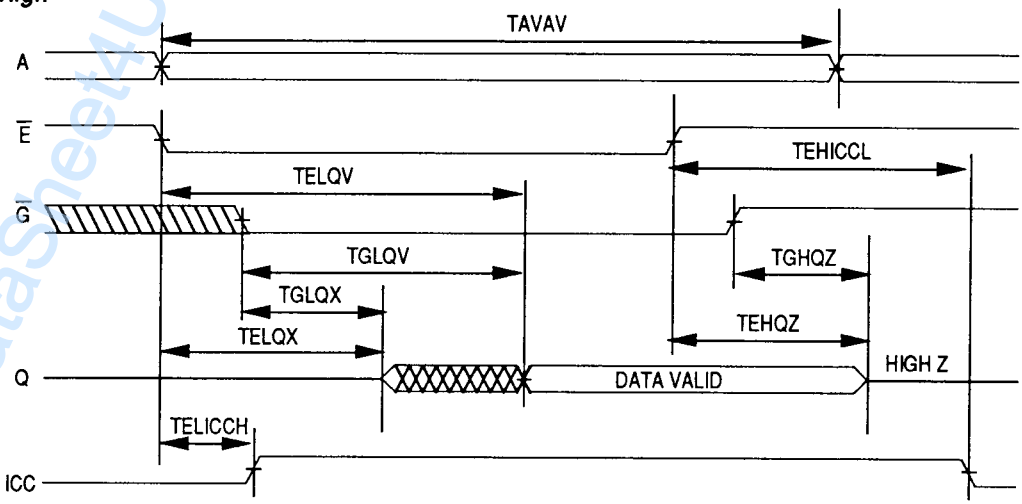
Parameter	Symbol JEDEC	Symbol Alt.		35ns Min	35ns Max	45ns Min	45ns Max	55ns Min	55ns Max	70ns Min	70ns Max	Units
Read Cycle Time	TAVAV	TRC		35		45		55		70		ns
Address Access Time	TAVQV	TAA			35		45		55		70	ns
Chip Enable Access Time	TELQV	TACS			35		45		55		70	ns
Chip Enable to Output Low Z (1)	TELQX	TCLZ		5		5		5		5		ns
Chip Enable to Output in High Z (1)	TEHQZ	TCHZ		0	15	0	20	0	25	0	30	ns
Output Hold from Address Change	TAVQX	TOH		5		5		5		5		ns
Chip Enable to Power Up (1)	TELICCH	TPU		0		0		0		0		ns
Chip Disable to Power Down (1)	TEHICCL	TPD		0	35	0	45	0	55	0	70	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
$\overline{W}$ High, $\overline{E}$ Low



Read Cycle 2
$\overline{W}$ High

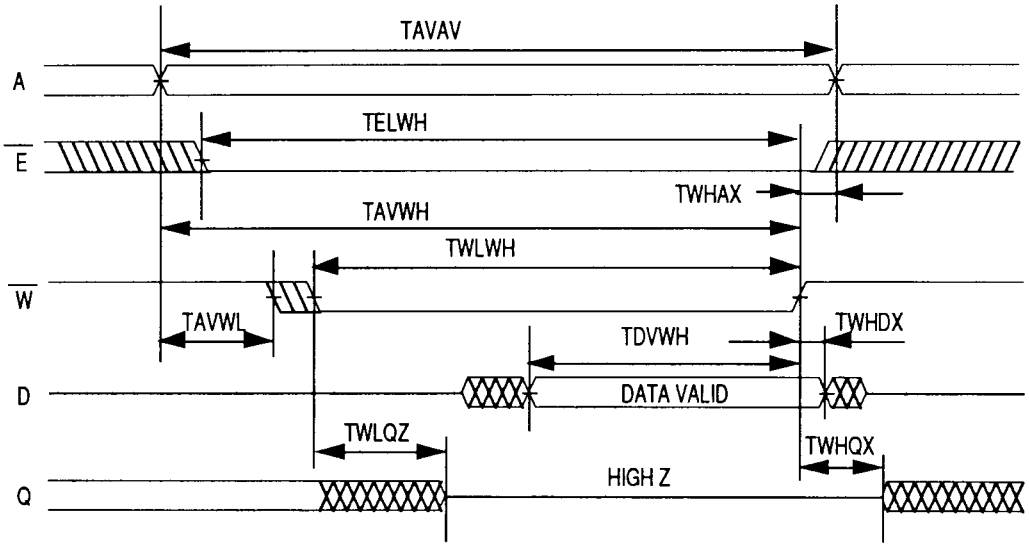


AC Characteristics
Write Cycle

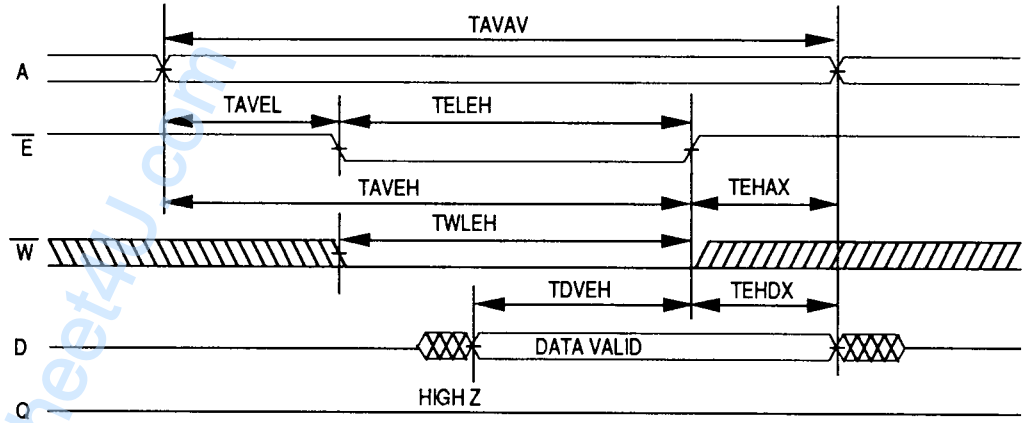
Parameter	Symbol JEDEC	Symbol Alt.		35ns Min	35ns Max	45ns Min	45ns Max	55ns Min	55ns Max	70ns Min	70ns Max	Units
Write Cycle Time	TAVAV	TWC		35		45		55		70		ns
Chip Enable to	TELWH	TCW		30		40		50		65		ns
End of Write	TELEH	TCW		30		40		50		65		ns
Address Setup Time	TAVWL	TAS		0		0		0		0		ns
	TAVEL	TAS		0		0		0		0		ns
Address Valid to	TAVWH	TAW		30		35		40		55		ns
End of Write	TAVEH	TAW		30		35		40		55		ns
Write Pulse Width	TWLWH	TWP		30		35		40		55		ns
	TWLEH	TWP		30		35		40		55		ns
Write Recovery Time	TWHAX	TWR		5		5		5		5		ns
	TEHAX	TWR		5		5		5		5		ns
Data Hold Time	TWHDX	TDH		0		0		0		0		ns
	TEHDX	TDH		0		0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ		0	15	0	20	0	20	0	30	ns
Data to Write Time	TDVWH	TDW		15		20		20		30		ns
	TDVEH	TDW		15		20		20		30		ns
Output Active from End of Write (1)	TWHQX	TWLZ		0		0		0		0		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled



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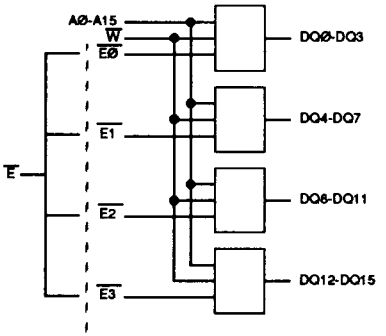
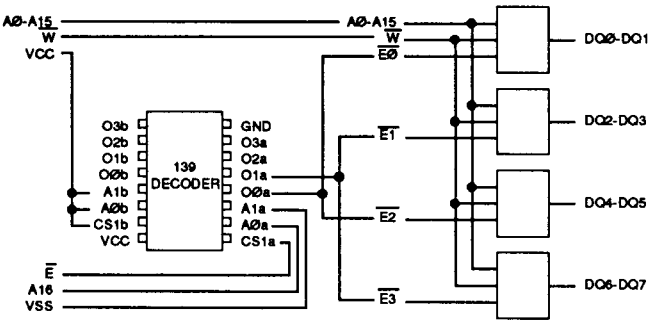
Device Configurations for 139 Decoder Applications

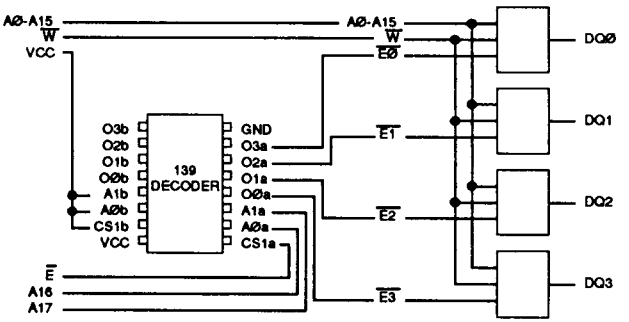
64Kx16 Configuration



128Kx8 Configuration



256Kx4 Configuration



Ordering Information

Part No.	Speed (ns)	Leads	Package Style	No.
EDI8M1665C35C9B	35	40	0.9 DIP	98
EDI8M1665C45C9B	45	40	0.9 DIP	98
EDI8M1665C55C9B	55	40	0.9 DIP	98
EDI8M1665C70C9B	70	40	0.9 DIP	98