

128Kx8 Static RAM CMOS, Module

The EDI8M8130C is a 1024K bit CMOS Static RAM Module based on four 32Kx8 Static RAMs in leadless chip carriers mounted on a multi-layered ceramic substrate.

The EDI8M8130C has an on-board decoder circuit that interprets the higher order address to select one of the 32Kx8 Static RAMs. The $\bar{E}$ and S lines perform the chip enable functions that automatically power down the device when proper logic levels are applied.

All inputs and outputs are TTL compatible and operate from a 5V supply. Fully asynchronous, the EDI8M8130C requires no clocks or refreshing for operation.

EDI Military Modules are constructed using semiconductor components which have been 100% processed to the test methods of MIL-STD-883C, Class B.

Features

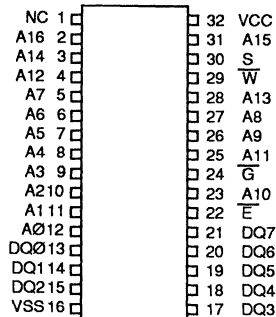
128Kx8 bit CMOS Static
Random Access Memory

- Access Times 50, 60, 70, and 80ns
- $\bar{E}$, S, and $\bar{G}$ Functions for Bus Control
- Data Retention Function
- Inputs and Outputs Directly TTL Compatible
- Fully Static, No Clocks

Jedec Approved Pinout

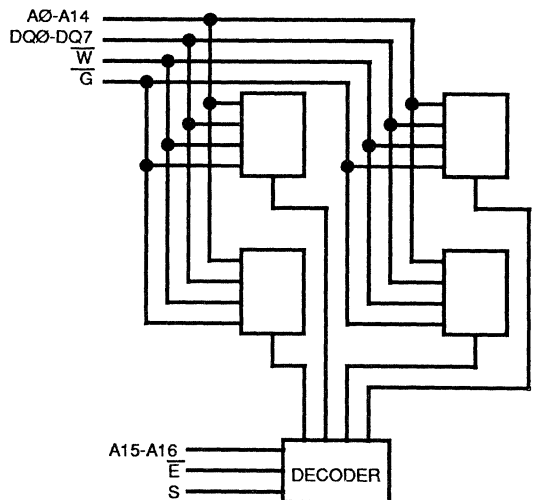
- 32 Pin Ceramic Dual-in-line Package
- Single +5V ($\pm 10\%$) Supply Operation

Pin Configurations and Block Diagram



Pin Names

A0-A16	Address Inputs
$\bar{E}$	Chip Enable
S	Chip Select
$\bar{W}$	Write Enable
$\bar{G}$	Output Enable
DQ0-DQ7	Data Input/Output
VCC	Power (+5V $\pm 10\%$)
VSS	Ground



Absolute Maximum Ratings*

Voltage on any pin relative to VSS -0.5V to 7.0V
 Operating Temperature TA (Ambient)
 Commercial 0°C to +70°C
 Military -55°C to +125°C
 Storage Temperature (Ambient/Ceramic). -65°C to +150°C
 Power Dissipation 1 Watt
 Output Current 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}, \overline{E} = \text{VIL}, \text{I/O} = 0\text{mA}, \text{Min Cycle}$ $S = \text{VIH}, \text{Min Cycle}$	--	70	120	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E} \geq \text{VIH}$ or $S \leq \text{VIL}$	--	20	75	mA
Full Standby Power Supply Current	ICC3	$\overline{E} \geq \text{VCC}-0.2\text{V}$ or $S \leq 0.2\text{V}$ $\text{VIN} \geq \text{VCC}-0.2\text{V}$ or $\text{VIN} \leq 0.2\text{V}$	--	4	10	mA
Input Leakage Current	IIL	$\text{VIN} = 0\text{V}$ to VCC	--	--	±10	μA
Output Leakage Current	IOL	$\text{V I/O} = 0\text{V}$ to VCC; $\overline{E}, \overline{G} = \text{VIH}$ or $S = \text{VIL}$	--	--	±10	μA
Output High Voltage	VOH	$\text{IOH} = -4.0\text{mA}$	2.4	--	--	V
Output Low Voltage	VOL	$\text{IOL} = 8.0\text{mA}$	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{G}$	$\overline{E}$	S	$\overline{W}$	Mode	Output	Power
X	H	X	X	Standby	High Z	ICC2, ICC3
X	X	L	X	Standby	High Z	ICC2, ICC3
H	L	H	H	Output Deselect	High Z	ICC1
L	L	H	H	Read	DOUT	ICC1
X	L	H	L	Write	DIN	ICC1

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels VSS to 3.0V
 Input Rise and Fall Times 5ns
 Input and Output Timing Levels 1.5V
 Output Load 1TTL, CL = 30pF
 (note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	CI	50	pF
Capacitance Control (DQ Pins)	CD/Q	43	pF
Input Capacitance Control Lines ($\overline{E}, S$)	CC	10	pF
Input Capacitance $\overline{W}$ Line	CW	50	pF

Note: These parameters are sampled, not 100% tested.

AC Characteristics

Read Cycle

(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

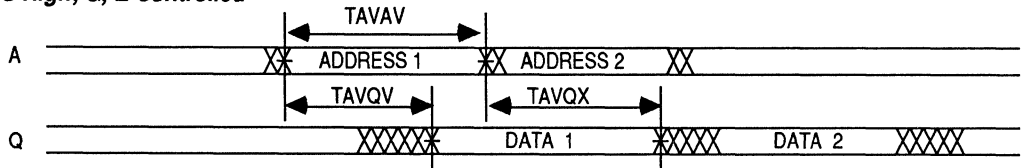
Parameter	Symbol	50ns*		60ns		70ns		80ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	50		60		70		80		ns
Address Access Time	TAVQV		50		60		70		80	ns
Chip Enable Access Time	TELQV $\bar{E}$		50		60		70		80	ns
	TSHQV S		50		60		70		80	ns
Chip Enable to Output in Low Z (1)	TELQX $\bar{E}$	30		30		30		30		ns
	TSHQX S	30		30		30		30		ns
Chip Disable to Output in High Z (1)	TEHQZ $\bar{E}$		25		25		25		30	ns
	TSLQZ S		25		25		25		30	ns
Output Hold from Address Change	TAVQX	10		10		10		10		ns
Output Enable to Output Valid	TGLQV		40		40		45		50	ns
Output Enable to Output in Low Z (1)	TGLQX	10		10		10		10		ns
Output Disable to Output in High Z (1)	TGHQZ		25		25		25		30	ns

Note 1: Parameter guaranteed, but not tested.

*Available in Commercial Temperature Range Only

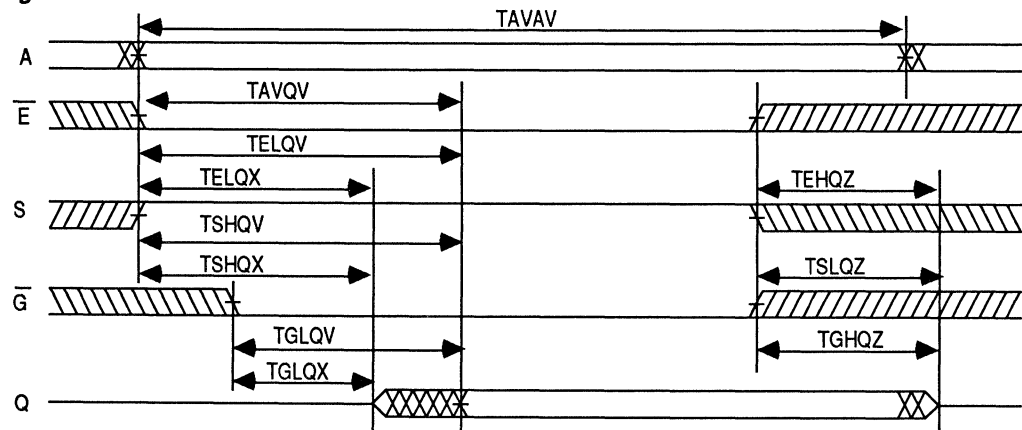
Read Cycle 1

W, S High; $\bar{G}$, $\bar{E}$ Controlled



Read Cycle 2

W High



AC Characteristics

Write Cycle

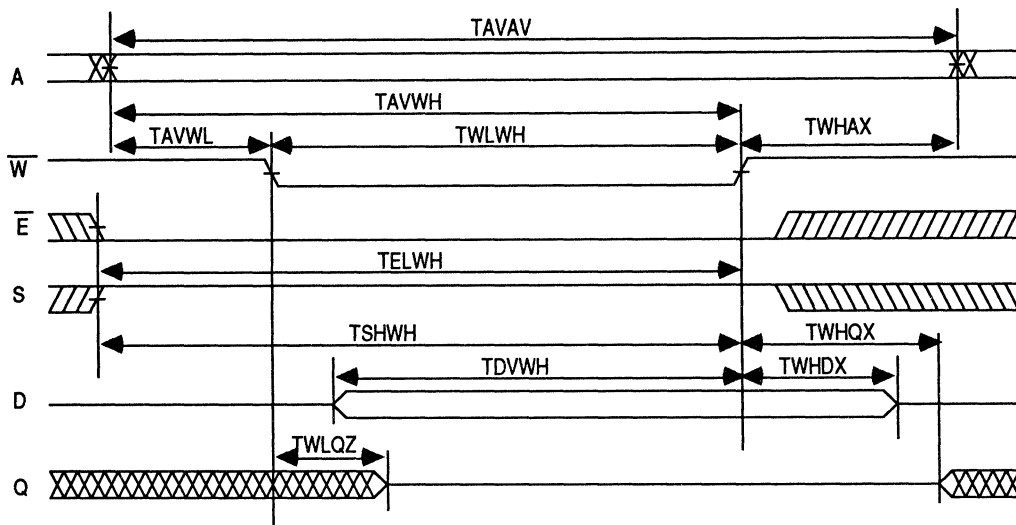
(TA = 0°C to +70°C or -55°C to +125°C; VCC = 5.0V ±10%)

Parameter	Symbol		50ns*		60ns		70ns		80ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		50		60		70		80		ns
Chip Enable to End of Write	TELWH	$\overline{E}$	45		55		60		70		ns
	TSHWH	S	45		55		60		70		ns
Address Setup Time	TAVWL	$\overline{W}$	20		20		20		20		ns
	TAVEL	$\overline{E}$	0		0		0		0		ns
	TAVSH	S	0		0		0		0		ns
Address Valid to End of Write	TAVWH		45		55		60		70		ns
Write Pulse Width	TWLWH	$\overline{W}$	40		50		55		60		ns
	TELEH	$\overline{E}$	40		50		55		60		ns
	TSHSL	S	40		50		55		60		ns
Write Recovery Time	TWHAX	$\overline{W}$	5		5		5		5		ns
	TEHAX	$\overline{E}$	5		5		5		5		ns
	TSLAX	S	5		5		5		5		ns
Data Hold Time	TWHDX	$\overline{W}$	5		5		5		5		ns
	TEHDX	$\overline{E}$	5		5		5		5		ns
	TSLDX	S	5		5		5		5		ns
Write to Output in High Z (1)	TWLQZ			25		25		30		35	ns
Data to Write Time	TDVWH	$\overline{W}$	25		25		30		35		ns
	TDVEH	$\overline{E}$	25		25		30		35		ns
	TDVSL	S	25		25		30		35		ns
Output Active from End of Write (1)	TWHQX		0		0		0		0		ns

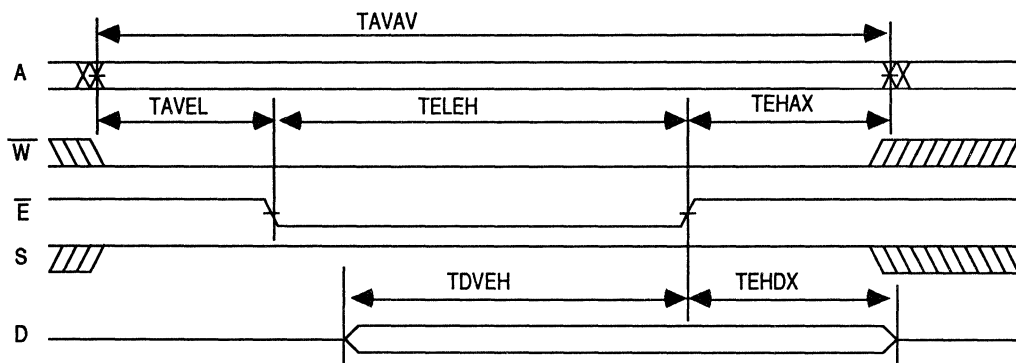
Note 1: Parameter guaranteed, but not tested.

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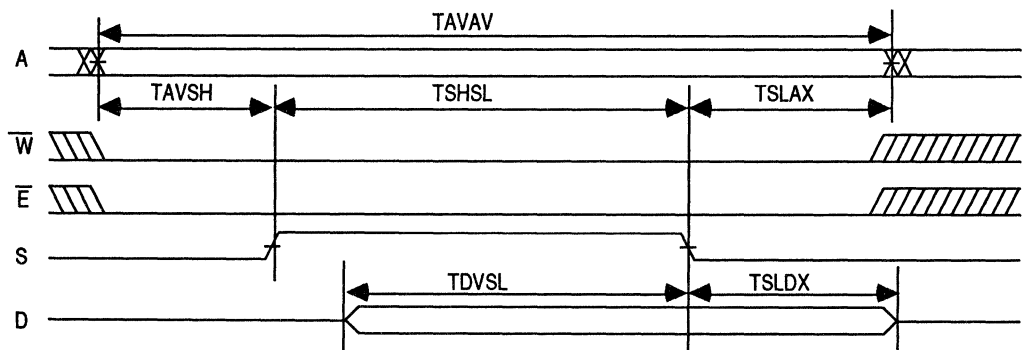
Write Cycle 1
Late Write, $\overline{W}$ Controlled



Write Cycle 2
Early Write, $\overline{E}$ Controlled



Write Cycle 3
Early Write, S Controlled



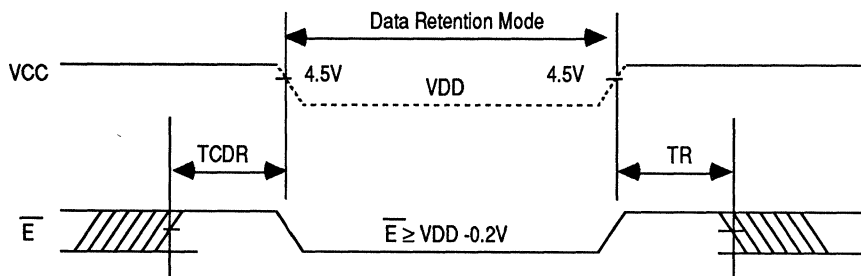
Data Retention Characteristics

(TA = 0°C to +70°C or -55°C to +125°C)

Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	--	--	V
Data Retention Quiescent Current	ICCDR	$\bar{E} \geq VDD - 0.2V$; $S \leq 0.2V$	--	900	2500	μA
Chip Disable to Data Retention Time	TCDR	VIN $\geq$ VDD - 0.2V	0	--	--	ns
Operation Recovery Time	TR	or VIN $\leq$ 0.2V	TAVAV*	--	--	ns

*Read Cycle Time

Data Retention $\bar{E}$ Controlled



Data Retention S Controlled

