256Kx8 Static RAM CMOS, Module

PRELIMINARY

The EDI8M8256C is a 2048K bit CMOS Static RAM module.

It is based on eight 32Kx8 Static RAMs in plastic VSOP packages mounted on a multi-layered ceramic substrate. The EDI8M8256C has an on-board decoder circuit that interprets the higher order address to select one of the 32Kx8 Static RAMs.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous, the EDI8M8256C requires no clocks or refreshing for operation.

Features

256Kx8 bit CMOS Static Random Access Memory Module

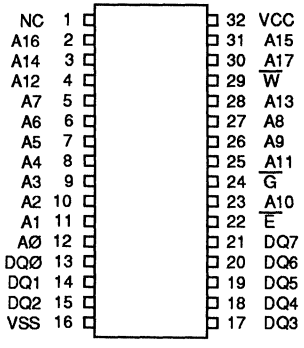
- Access Times 70, 100, and 120ns
- Fully Static, No Clocks
- TTL Compatible Inputs and Outputs

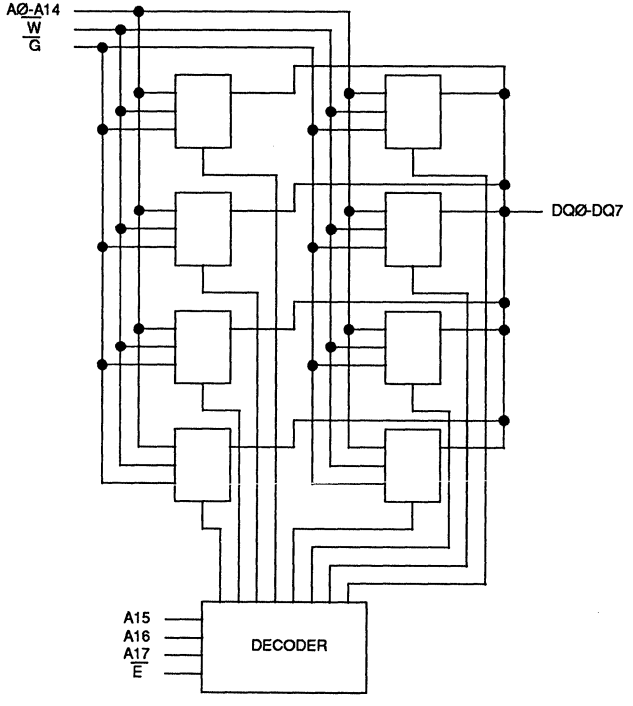
32 Pin Dual-in-line Package (P)

- JEDEC Approved Pinout

Single +5V (±10%) Supply Operation

Pin Configuration and Block Diagram





Pin Names

AØ-A17	Address Inputs
E	Chip Enable
W	Write Enable
G	Output Enable
DQØ-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground

Absolute Maximum Ratings*

Voltage on any pin relative to VSS .....-0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial.....0°C to +70°C
Storage Temperature (Ambient/Ceramic). -65°C to +150°C
Power Dissipation..... 1 Watt
Output Current..... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels..... VSS to 3.0V
Input Rise and Fall Times..... 5ns
Input and Output Timing Levels..... 1.5V
Output Load..... 1TTL, CL = 100pF
(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

(TA = 0°C to +70°C; VCC = 5.0V ±10%)

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle	--	80	100	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$≥ VIH	--		65	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$≥ VCC-0.2V VIN ≥VCC-0.2V or VIN≤0.2V	--		20	mA
Input Leakage Current	IIL	VIN = 0V to VCC	--	--	10	µA
Output Leakage Current	IOL	V I/O = 0V to VCC	--	--	10	µA
Output High Voltage	VOH	IOH = -1.0mA	2.4	--	--	V
Output Low Voltage	VOL	IOL = 2.1mA	--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	CI	55	pF
Capacitance Control (DQ Pins)	CD/Q	42	pF
Input Capacitance Control Lines	CC	16	pF
Input Capacitance $\overline{W}$ Line	CW	48	pF

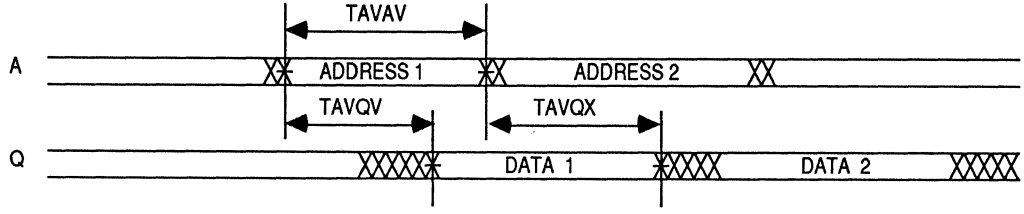
These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle
(TA = 0°C to +70°C; VCC = 5.0V ±10%)

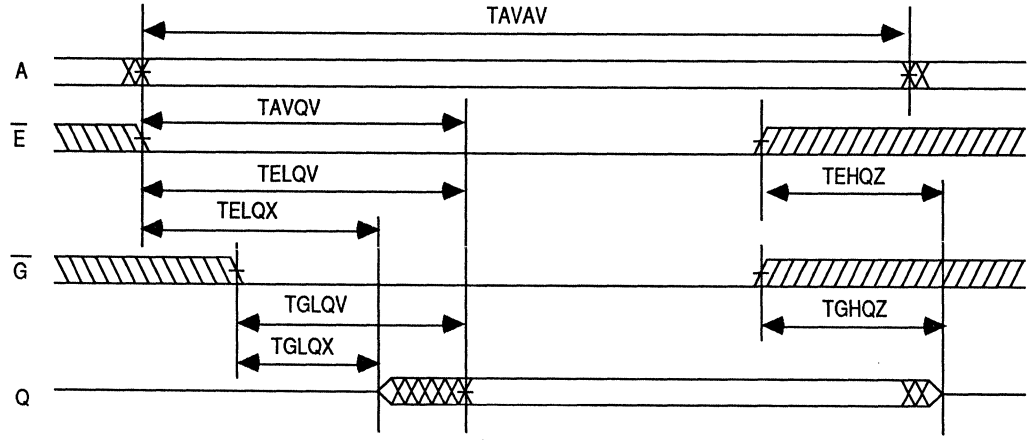
Parameter	Symbol		70ns		100ns		120ns		Units
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV		70		100		120		ns
Address Access Time	TAVQV			70		100		120	ns
Chip Enable Access Time	TELQV			70		100		120	ns
Chip Enable to Output in Low Z (1)	TELQX		30		30		30		ns
Output Enable to Output Valid	TGLQV			35		50		60	ns
Output Enable to Output in Low Z (1)	TGLQX		10		10		10		ns
Chip Enable to Output in High Z (1)	TEHQZ		0	30	0	30	0	40	ns
Output Enable to Output in High Z (1)	TGHQZ		0	30	0	30	0	40	ns
Output Hold from Address Change	TAVQX		10		10		10		ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
$\overline{W}$ High; $\overline{G}$, $\overline{E}$ Low



Read Cycle 2
$\overline{W}$ High



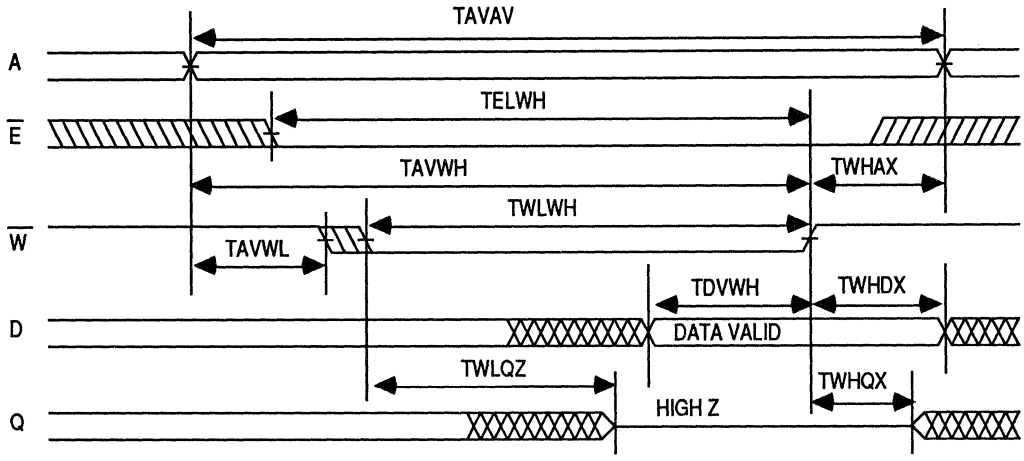
AC Characteristics
Write Cycle

(TA = 0°C to +70°C; VCC = 5.0V ±10%)

Parameter	Symbol		70ns		100ns		120ns		Units
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		70		100		120		ns
Chip Enable to	TELWH	$\overline{W}$	65		80		90		ns
End of Write	TWLEH	$\overline{E}$	65		80		90		ns
Address Setup Time	TAVWL	$\overline{W}$	20		20		20		ns
	TAVEL	$\overline{E}$	0		0		0		ns
Address Valid to	TAVWH	$\overline{W}$	60		80		90		ns
End of Write	TAVEH	$\overline{E}$	60		80		90		ns
Write Pulse Width	TWLWH	$\overline{W}$	55		60		70		ns
	TELEH	$\overline{E}$	55		60		70		ns
Write Recovery Time	TWHAX	$\overline{W}$	5		5		5		ns
	TEHAX	$\overline{E}$	5		5		5		ns
Data Hold Time	TWHDX	$\overline{W}$	5		5		5		ns
	TEHDX	$\overline{E}$	5		5		5		ns
Write to Output in High Z (1)	TWLQZ		0	30	0	35	0	40	ns
Data to Write Time	TDVWH	$\overline{W}$	30		35		40		ns
	TDVEH	$\overline{E}$	30		35		40		ns
Output Active from End of Write (1)	TWHQX		0		0		0		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled