

64Kx8 Static RAM CMOS, Module

The EDI8M864C is a 512K bit CMOS Static RAM based on two 32Kx8 Static RAMs in leadless chip carriers mounted on a multi-layered ceramic substrate.

The EDI8M864C has an on-board decoder circuit that interprets the higher order address to select one of the 32Kx8 Static RAMs.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous, the EDI8M864C requires no clocks or refreshing for operation.

EDI's military modules are built with RAMs that are compliant to MIL-STD-883, Paragraph 1.2.1.

Features

64Kx8 bit CMOS Static

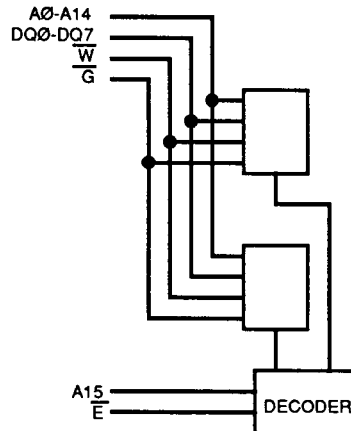
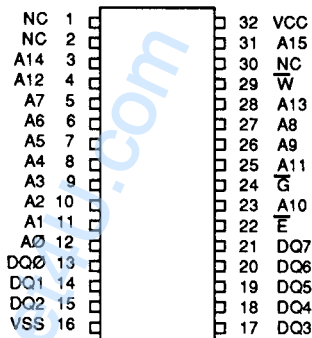
Random Access Memory

- Access Times 45, 55, 70, 80, 90, 100, 120, and 150ns
- Data Retention Function
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

Jedec Approved Pinout

- 32 Pin Dual-in-line Package, No. 50
- Single +5V ($\pm 10\%$) Supply Operation

Pin Configuration and Block Diagram



Pin Names

A0-A15	Address Inputs
\bar{E}	Chip Enable
\bar{W}	Write Enable
\bar{G}	Output Enable
DQ0-DQ7	Common Data Input/Output
VCC	Power (+5V $\pm 10\%$)
VSS	Ground
NC	No Connection

Absolute Maximum Ratings*

Voltage on any pin relative to VSS -0.5V to 7.0V
 Operating Temperature TA (Ambient)
 Commercial 0°C to +70°C
 Industrial -40°C to +85°C
 Military -55°C to +125°C
 Storage Temperature, Ceramic -65°C to +150°C
 Power Dissipation 1 Watt
 Output Current 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels VSS to 3.0V
 Input Rise and Fall Times 5ns
 Input and Output Timing Levels 1.5V
 Output Load 45-70ns 1TTL, CL = 30pF
 80-150ns 1TTL, CL = 100pF
 (note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Typ*	Max		Units
					45-70	80-150	
Operating Power Supply Current	ICC1	W, E = VIL, I/O = 0mA, Min Cycle		--	160	95	mA
Standby (TTL) Power Supply Current	ICC2	E ≥ VIH, VIN ≤ VIL or ≥ VIH		--	80	40	mA
Full Standby Power Supply Current	ICC3	E ≥ VCC-0.2V VIN ≥ VCC-0.2V or VIN ≤ 0.2V		--	20	1.5	mA
Input Leakage Current	ILI	VIN = 0V to VCC		--	10	10	μA
Output Leakage Current	ILO	V I/O = 0V to VCC		--	10	10	μA
Output High Voltage	VOH	IOH = -1.0mA	2.4	--	--	--	V
Output Low Voltage	VOL	IOL = 2.1mA		--	0.4	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

\bar{G}	\bar{E}	\bar{W}	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	CI	50	pF
Capacitance Control (DQ Pins)	CD/Q	43	pF
Input Capacitance Control Lines (\bar{E})	CC	10	pF
Input Capacitance \bar{W} Line	CW	50	pF

These parameters are sampled, not 100% tested.

AC Characteristics Read Cycle

Parameter	Symbol	45ns		55ns		70ns		80ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	45		55		70		80		ns
Address Access Time	TAVQV		45		55		70		80	ns
Chip Enable Access Time	TELQV		45		55		70		80	ns
Chip Enable to Output in Low Z (1)	TELQX	5		5		5		5		ns
Output Enable to Output Valid	TGLQV		20		25		35		35	ns
Output Enable to Output in Low Z (1)	TGLQX	3		3		3		0		ns
Chip Disable to Output in High Z (1)	TEHQZ		20		25		35		35	ns
Output Disable to Output in High Z(1)	TGHQZ		20		25		35		35	ns
Output Hold from Address Change	TAVQX	3		3		3		3		ns

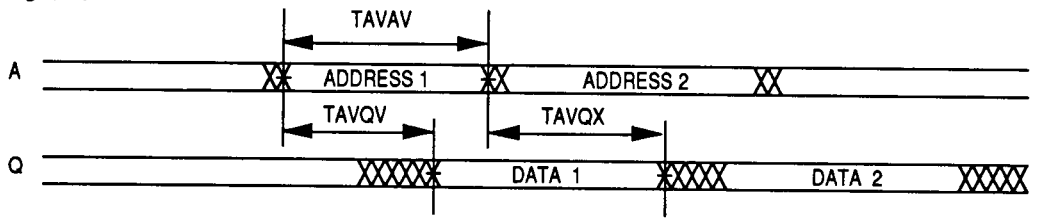
Note 1: Parameter guaranteed, but not tested.

AC Characteristics Read Cycle

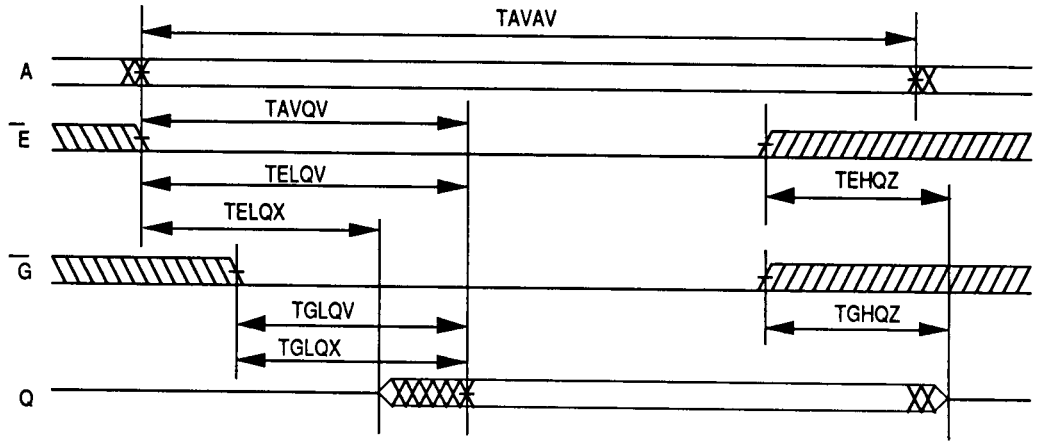
Parameter	Symbol	90ns		100ns		120ns		150ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	90		100		120		150		ns
Address Access Time	TAVQV		90		100		120		150	ns
Chip Enable Access Time	TELQV		90		100		120		150	ns
Chip Enable to Output in Low Z (1)	TELQX	5		5		5		5		ns
Output Enable to Output Valid	TGLQV		40		50		60		70	ns
Output Enable to Output in Low Z (1)	TGLQX	0		0		0		0		ns
Chip Disable to Output in High Z (1)	TEHQZ		35		35		40		45	ns
Output Disable to Output in High Z(1)	TGHQZ		35		35		40		45	ns
Output Hold from Address Change	TAVQX	3		3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
W High; G, E Low



Read Cycle 2
W High



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AC Characteristics

Write Cycle

Parameter	Symbol		45ns		55ns		70ns		80ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		45		55		70		80		ns
Chip Enable to	TELWH	\overline{W}	40		50		60		70		ns
End of Write	TWLEH	\overline{E}	40		50		60		70		ns
Address Setup Time	TAVWL	\overline{W}	0		0		0		0		ns
	TAVEL	\overline{E}	0		0		0		0		ns
Address Valid to	TAVWH	\overline{W}	40		50		60		70		ns
	TAVEH	\overline{E}	40		50		60		70		ns
Write Pulse Width	TWLWH	\overline{W}	25		25		45		55		ns
	TELEH	\overline{E}	25		25		45		55		ns
Write Recovery Time	TWHAX	\overline{W}	0		0		0		0		ns
	TEHAX	\overline{E}	0		0		0		0		ns
Data Hold Time	TWHDX	\overline{W}	0		0		3		3		ns
	TEHDX	\overline{E}	0		0		3		3		ns
Write to Output in High Z (1)	TWLQZ		0	20	0	25	0	40	0	45	ns
Data to Write Time	TDVWH	\overline{W}	20		25		30		35		ns
	TDVEH	\overline{E}	20		25		30		35		ns
Output Active from End of Write (1)	TWHQX		0		0		3		3		ns

Note 1: Parameter guaranteed, but not tested.

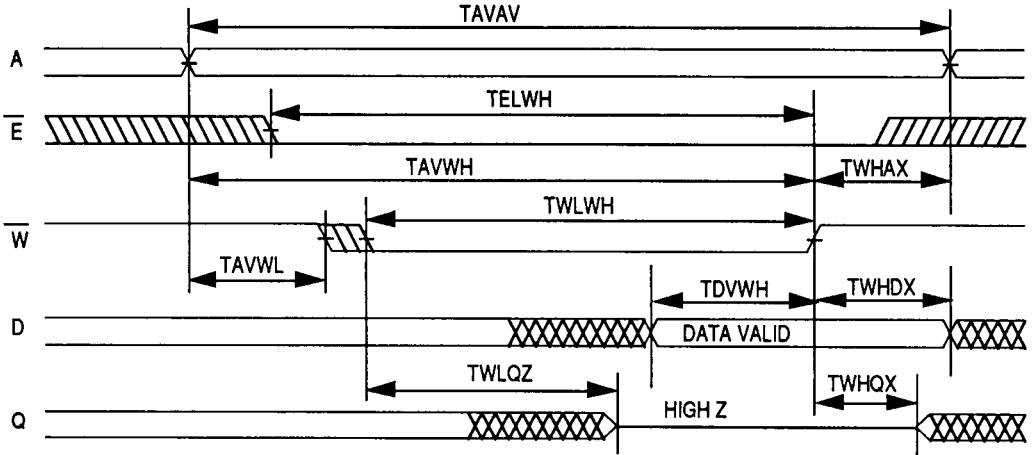
AC Characteristics

Write Cycle

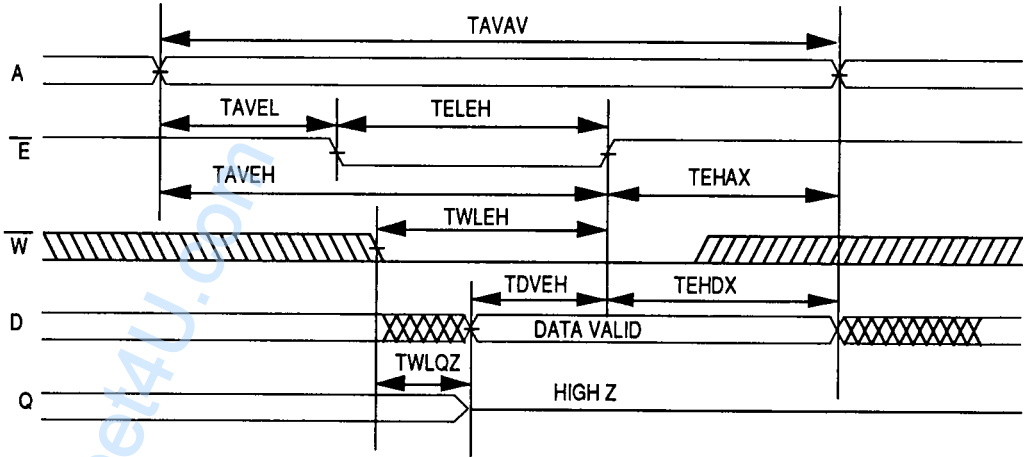
Parameter	Symbol		90ns		100ns		120ns		150ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		90		100		120		150		ns
Chip Enable to	TELWH	\overline{W}	80		80		85		90		ns
End of Write	TWLEH	\overline{E}	80		80		85		90		ns
Address Setup Time	TAVWL	\overline{W}	0		0		0		0		ns
	TAVEL	\overline{E}	0		0		0		0		ns
Address Valid to	TAVWH	\overline{W}	70		80		85		90		ns
End of Write	TAVEH	\overline{E}	70		80		85		90		ns
Write Pulse Width	TWLWH	\overline{W}	55		70		70		80		ns
	TELEH	\overline{E}	55		70		70		80		ns
Write Recovery Time	TWHAX	\overline{W}	0		0		0		0		ns
	TEHAX	\overline{E}	0		0		0		0		ns
Data Hold Time	TWHDX	\overline{W}	3		3		3		3		ns
	TEHDX	\overline{E}	3		3		3		3		ns
Write to Output in High Z (1)	TWLQZ		0	45	0	50	0	50	0	50	ns
Data to Write Time	TDVWH	\overline{W}	35		35		40		50		ns
	TDVEH	\overline{E}	35		35		40		50		ns
Output Active from End of Write (1)	TWHQX		3		3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
W Controlled



Write Cycle 2
E Controlled



Data Retention Characteristics

Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	--	--	V
Data Retention Quiescent Current	ICDDR	$\bar{E} \geq VDD - 0.2V$	--	300	750	μA
Chip Disable to Data Retention Time	TCDR	$V_{IN} \geq VDD - 0.2V$	0	--	--	ns
Operation Recovery Time	TR	or $V_{IN} \leq 0.2V$	TAVAV*	--	--	ns

*Read Cycle Time

Data Retention \bar{E} Controlled

