



512Kx37 Static RAM CMOS, High Speed Module

FEATURES

- 512Kx37 bit CMOS Static RAM
 - Access Times: 45 and 55ns
 - Individual Byte Selects
 - Fully Static, No Clocks
 - TTL Compatible I/O
- High Density Package
 - 72 lead SIMM, No. 418
 - Common Data Inputs and Outputs
- Single +5V (±10%) Supply Operation

DESCRIPTION

The EDI9F37512C is a high speed 20 megabit Static RAM module organized as 512K words x 37 bits. This module is constructed from five 512Kx8 Static RAMs in TSOP packages on an epoxy laminate (FR4) board.

Four write selects (W0-W3) are used to independently enable the four bytes. Reading and writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

The EDI9F37512C is offered in a 72 lead SIMM which allows 20 megabits of memory to be placed in less than 1.5 square inch of board space.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

The SIMM module contains two Presence Detect pins which are used to identify module memory density in applications where alternate modules can be interchanged.

FIG. 1

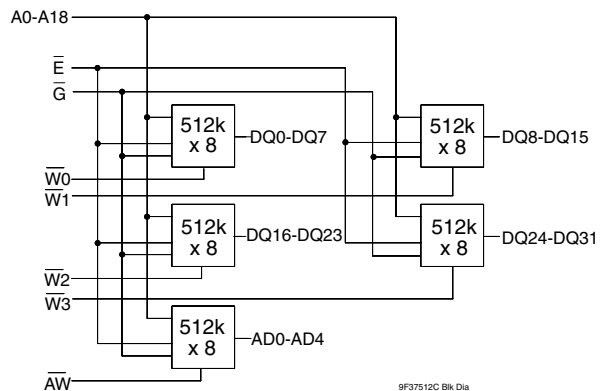
PIN CONFIGURATIONS AND BLOCK DIAGRAM

AD3	1	W3	37
AD4	2	W2	38
AD1	3	A18	39
AD2	4	A17	40
VSS	5	G	41
AD0	6	VSS	42
AW	7	DQ24	43
DQ0	8	DQ16	44
DQ8	9	DQ25	45
DQ1	10	DQ17	46
DQ9	11	DQ26	47
DQ2	12	DQ18	48
DQ10	13	DQ27	49
DQ3	14	DQ19	50
DQ11	15	A8	51
VCC	16	A9	52
A0	17	A10	53
A1	18	A11	54
A2	19	A12	55
A3	20	A13	56
A4	21	VCC	57
A5	22	A14	58
DQ12	23	A15	59
DQ4	24	DQ20	60
DQ13	25	DQ28	61
DQ5	26	DQ21	62
DQ14	27	DQ29	63
DQ6	28	DQ22	64
DQ15	29	DQ30	65
DQ7	30	DQ23	66
VSS	31	DQ31	67
E	32	VSS	68
A6	33	A16	69
A7	34	PD1	70
W1	35	NC	71
W0	36	PD0	72

9F37512C Pin Config

PIN NAMES

A0-A18	Address Inputs
\bar{E}	Chip Enables
$\bar{W}0-\bar{W}3$	Write Enable
$\bar{A}W$	Parity Write Enable
\bar{G}	Output Enable
DQ0-DQ31	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
PD0-PD1	Presence Detect



9F37512C Blk Dia



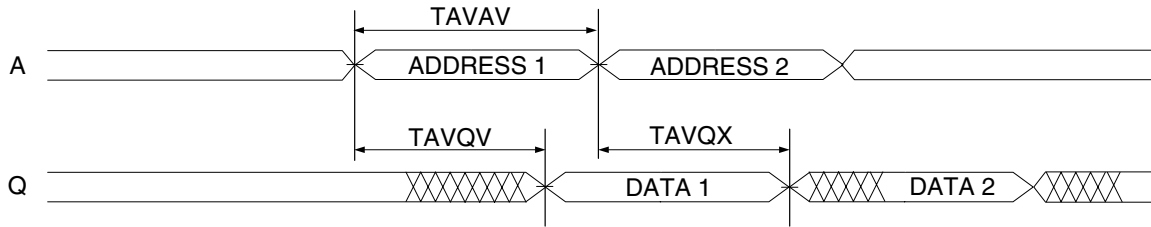
AC CHARACTERISTICS READ CYCLE

Parameter	Symbol		45ns		55ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC	45		55		ns
Address Access Time	TAVQV	TAA		45		55	ns
Chip Enable Access	TELQV	TACS		45		55	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		18		25	ns
Output Hold from Address Change	TAVQX	TOH	3		3		ns
Output Enable to Output Valid	TGLQV	TOE		15		25	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		15		15	ns

Notes: 1. Parameter guaranteed, but not tested.

FIG. 2

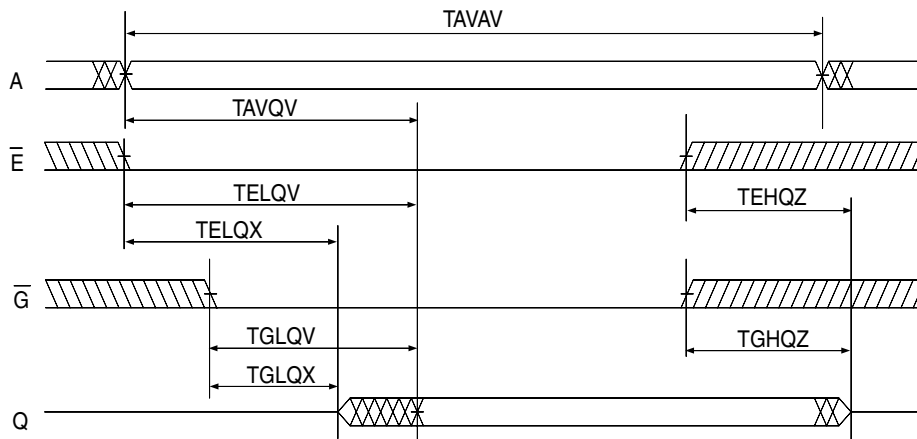
READ CYCLE 1 - \bar{W} HIGH, \bar{G} , \bar{E} LOW



9F37512C Rd Cyc1

FIG. 3

READ CYCLE 2 - \bar{W} HIGH



9F37512C Rd Cyc2



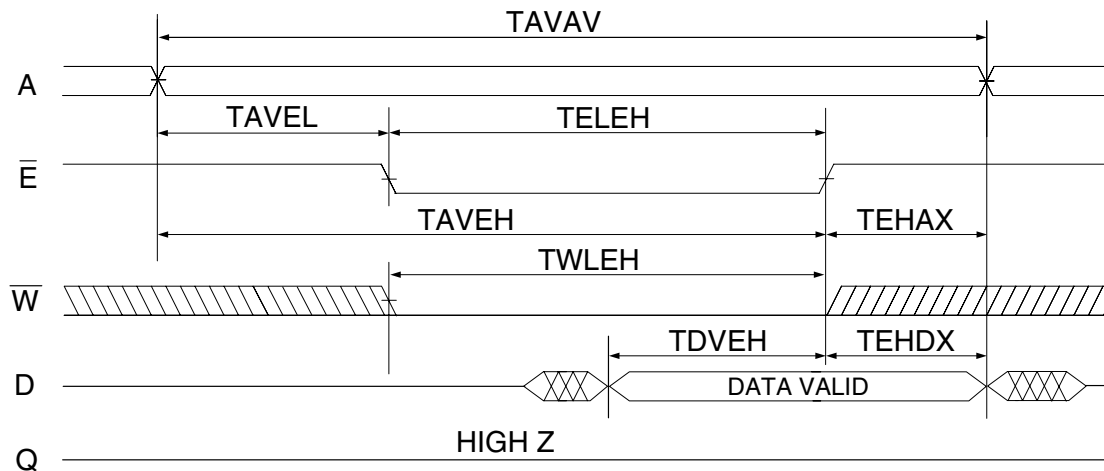
AC CHARACTERISTICS WRITE CYCLE

Parameter	Symbol		45ns		55ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	
Write Cycle Time	TAVAV	TWC	45		55		ns
Chip Enable to End of Write	TELWH	TCW	25		45		ns
	TWLEH	TCW	25		45		ns
Address Setup Time	TAVWL	TAS	0		0		ns
	TAVEL	TAS	0		0		ns
Address Valid to End of Write	TAVWH	TAW	25		45		ns
	TAVEH	TAW	25		45		ns
Write Pulse Width	TWLWH	TWP	25		40		ns
	TELEH	TWP	25		40		ns
Write Recovery Time	TWHAX	TWR	0		0		ns
	TEHAX	TWR	0		0		ns
Data Hold Time	TWHDX	TDH	0		0		ns
	TEHDX	TDH	0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	6	0	28	ns
Data to Write Time	TDVWH	TDW	20		30		ns
	TDVEH	TDW	20		30		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		3		ns

Notes: 1. Parameter guaranteed, but not tested.

FIG. 4

WRITE CYCLE 2 - \bar{E} CONTROLLED



9F37512C Write Cyc2

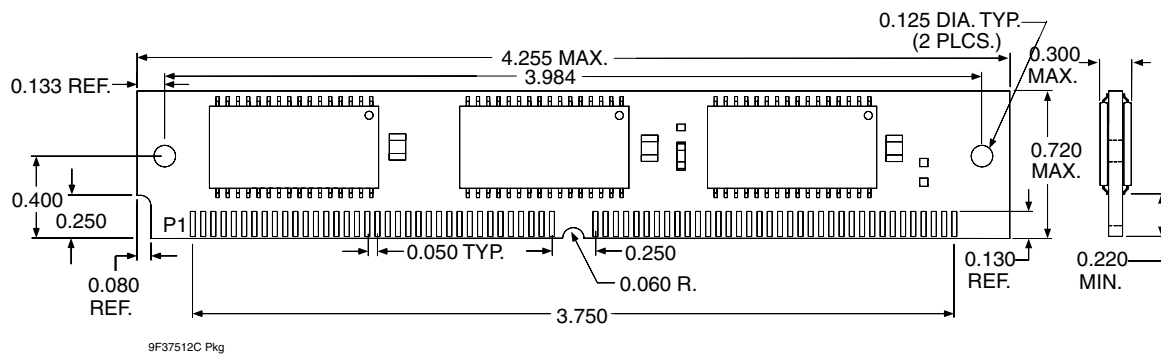


ORDERING INFORMATION

Part Number	Speed (ns)	Package No.
EDI9F37512C45MMC	45	418
EDI9F37512C55MMC	55	418

PACKAGE DESCRIPTION

PACKAGE NO. 418: 72 PIN ZIP



ALL DIMENSIONS ARE IN INCHES

