EDI9F81025C

High Speed Eight Megabit SRAM Module

2x512Kx8 Static RAM CMOS, Module

The EDI9F81025C is an 8 megabit CMOS Static RAM based on two 512Kx8 Static RAMs mounted on a multi-layered epoxy laminate (FR4) substrate.

The EDI9F81025C is organized as two separate banks of 512Kx8 Random Access Memory, with common address and data pins to minimize module size. It is offered with access times of 70, 85, and 100ns.

It is also available as EDI9F81025LP, which features Low Power and Battery Back-up Data Retention.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous, the EDI9F81025C requires no clocks or refreshing for operation.

Features

2x512Kx8 bit CMOS Static Random Access Memory

- Access Times: 70, 85, and 100ns
- Common Address and Data Pins
- Data Retention Function (EDI9F81025LP)
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

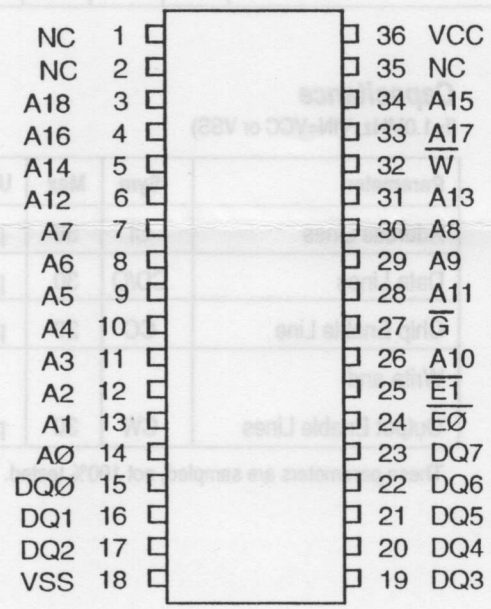
36 Lead SOIC Module, No. 198

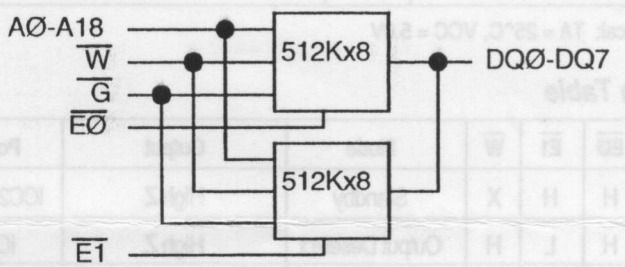
Single +5V (±10%) Supply Operation

Pin Names

AØ-A18	Address Inputs
$\overline{E}$Ø-$\overline{E}$1	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

Pin Configuration and Block Diagram





Absolute Maximum Ratings*

Voltage on any pin relative to VSS ..... -0.5V to 7.0V
Operating Temperature TA (Ambient)
Commercial ..... 0°C to +70°C
Industrial ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Power Dissipation ..... 2 Watts
Output Current. ..... 20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels ..... VSS to 3.0V
Input Rise and Fall Times 5ns
Input and Output Timing Levels 1.5V
Output Load ..... 1TTL, CL =100pF
(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions		Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, II/O = 0mA, $\overline{E\O}$ or $\overline{E1}$= VIL, Min Cycle (Operating Current per Bank of 512K bits)		--	60	85	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E} \geq$ VIH, VIN $\leq$ VIL VIN $\geq$ VIH		--	1	2	mA
Full Standby Power Supply Current	ICC3	$\overline{E} \geq$ VCC-0.2V	C			1	mA
		VIN $\geq$ VCC-0.2V or VIN $\leq$ 0.2V	LP		10	100	µA
Input Leakage Current	ILI	VIN = 0V to VCC		-10		10	µA
Output Leakage Current	ILO	V I/O = 0V to VCC		-10		10	µA
Output High Voltage	VOH	IOH =-1.0mA		2.4	--	--	V
Output Low Voltage	VOL	IOL = 2.1mA		--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{G}$	$\overline{E\O}$	$\overline{E1}$	$\overline{W}$	Mode	Output	Power
X	H	H	X	Standby	High Z	ICC2, ICC3
H	H	L	H	Output Deselect	High Z	ICC1
H	L	H	H	Output Deselect	High Z	ICC1
H	L	L	H	Output Deselect	High Z	ICC1, ICC2
L	L	H	H	Read	DOUT (1st 512K)	ICC1
L	H	L	H	Read	DOUT (2nd 512K)	ICC1
L	L	L	X	Not Allowed	–	–
X	L	H	L	Write	DIN (1st 512K)	ICC1
X	H	L	L	Write	DIN (2nd 512K)	ICC1
X	L	L	L	Write	DIN (1st & 2nd 512K)	ICC1, ICC2

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	30	pF
Data Lines	CD/Q	30	pF
Chip Enable Line	CC	20	pF
Write and Output Enable Lines	CW	30	pF

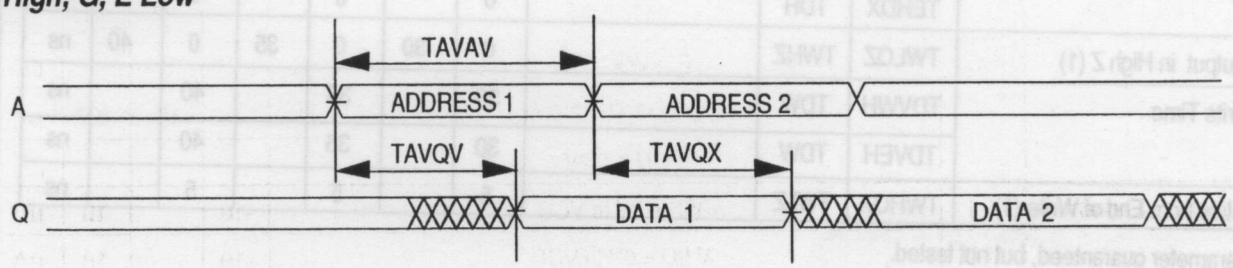
These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle

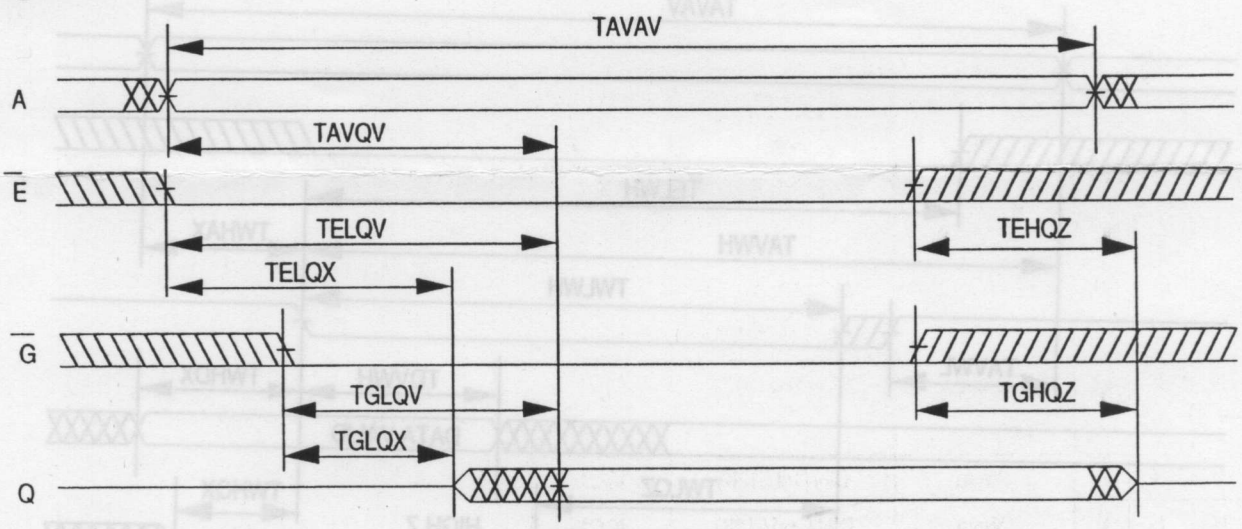
Parameter	Symbol JEDEC	Symbol Alt.		70ns Min	70ns Max	85ns Min	85ns Max	100ns Min	100ns Max	Units
Read Cycle Time	TAVAV	TRC		70		85		100		ns
Address Access Time	TAVQV	TAA			70		85		100	ns
Chip Enable Access Time	TELQV	TACS			70		85		100	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ		5		5		5		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ			30		35		40	ns
Output Hold from Address Change	TAVQX	TOH		5		5		5		ns
Output Enable to Output Valid	TGLQV	TOE			40		45		50	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ		5		5		5		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ			30		35		40	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
$\overline{W}$ High; $\overline{G}$, $\overline{E}$ Low



Read Cycle 2
$\overline{W}$ High

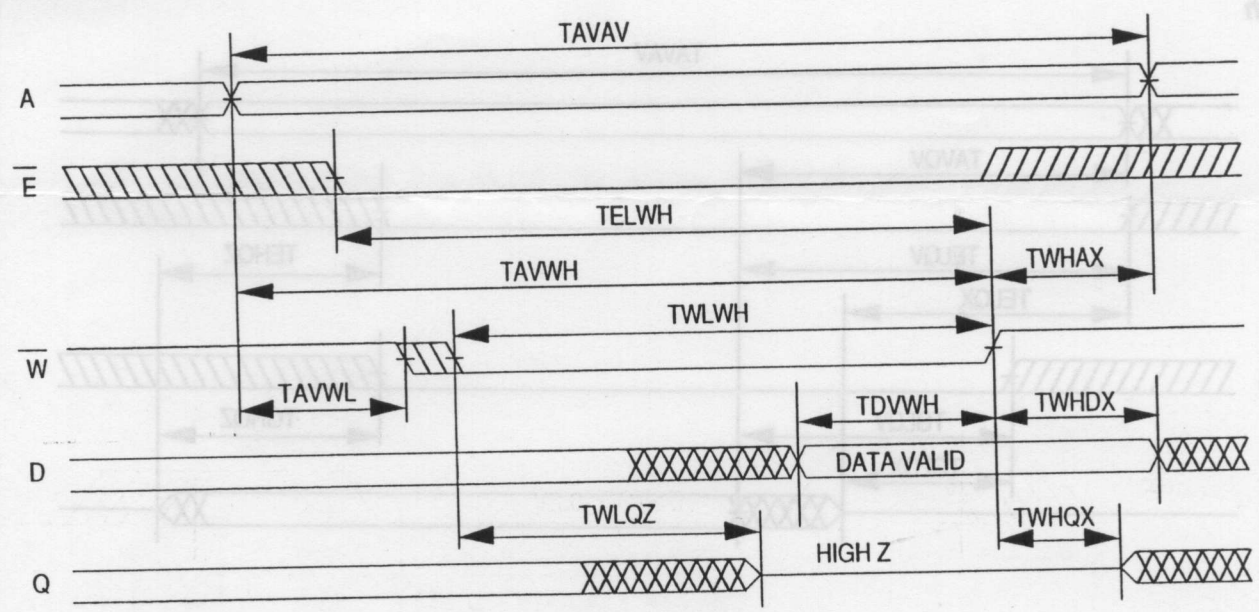


AC Characteristics
Write Cycle

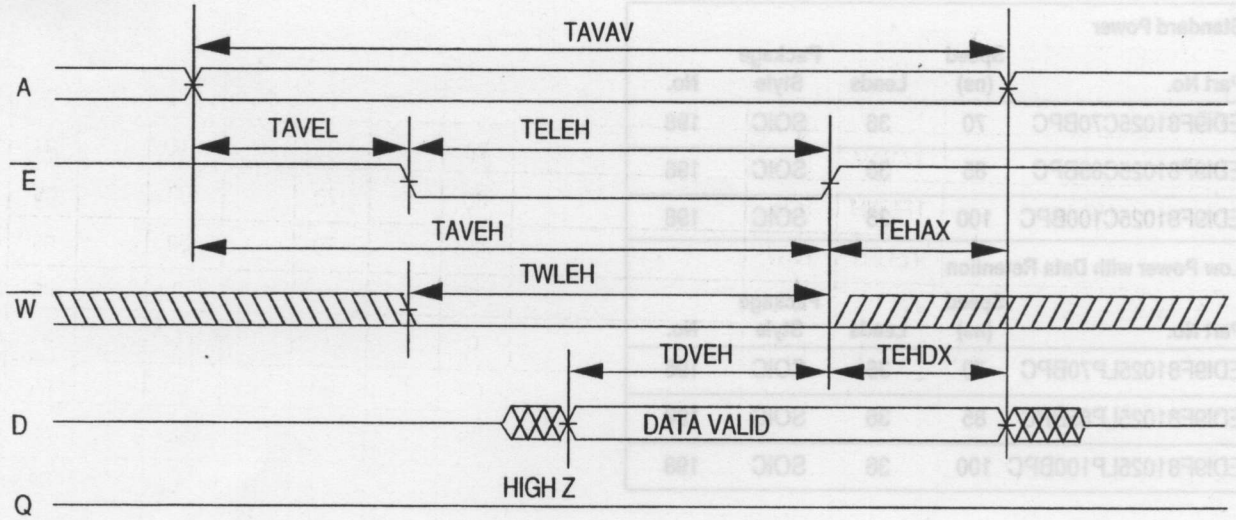
Parameter	Symbol JEDEC	Symbol Alt		70ns Min	70ns Max	85ns Min	85ns Max	100ns Min	100ns Max	Units
Write Cycle Time	TAVAV	TWC		70		85		100		ns
Chip Enable to End of Write	TELWH	TCW		65		70		80		ns
	TELEH	TCW		65		70		80		ns
Address Setup Time	TAVWL	TAS		0		0		0		ns
	TAVEL	TAS		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW		65		70		80		ns
	TAVEH	TAW		65		70		80		ns
Write Pulse Width	TWLWH	TWP		65		70		80		ns
	TWLEH	TWP		65		70		80		ns
Write Recovery Time	TWHAX	TWR		5		5		5		ns
	TEHAX	TWR		5		5		5		ns
Data Hold Time	TWHDX	TDH		0		0		0		ns
	TEHDX	TDH		0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ		0	30	0	35	0	40	ns
Data to Write Time	TDVWH	TDW		30		35		40		ns
	TDVEH	TDW		30		35		40		ns
Output Active from End of Write (1)	TWHQX	TWLZ		5		5		5		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1
$\overline{W}$ Controlled



Write Cycle 2
$\overline{E}$ Controlled

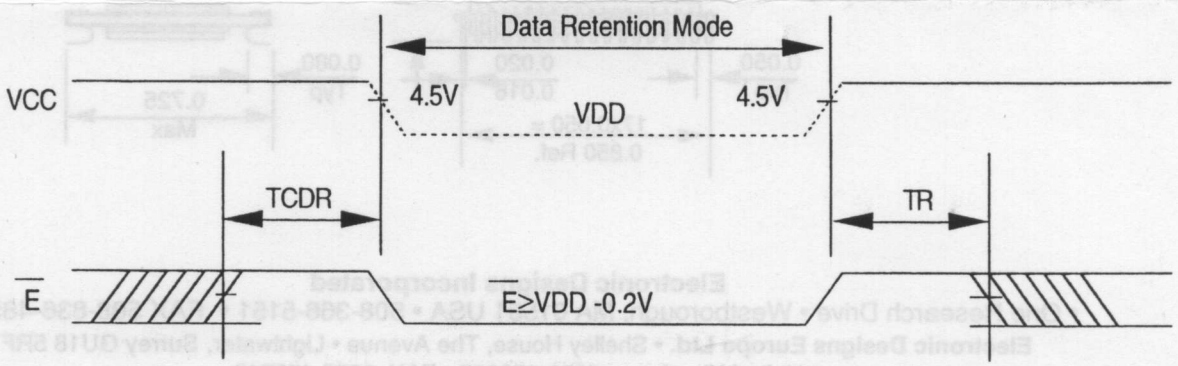


Data Retention Characteristics — *EDI9F81025LP*

Characteristic	Sym	Test Conditions	VDD	Min	Typ	Max		Unit
						70°C	85°C	
Data Retention Voltage	VDD	VDD= 0.2V		2	--	--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E}$≥ VDD -0.2V	2V	--	10	60	100	µA
		VIN ≥VDD -0.2V	3V	--	20	90	150	µA
Chip Disable to Data Retention Time(1)	TCDR	or VIN ≤0.2V		0		--	--	ns
Operation Recovery Time (1)	TR			5		--	--	ms

*Read Cycle Time Note 1: Parameter guaranteed, but not tested.

Data Retention
$\overline{E}$ Controlled



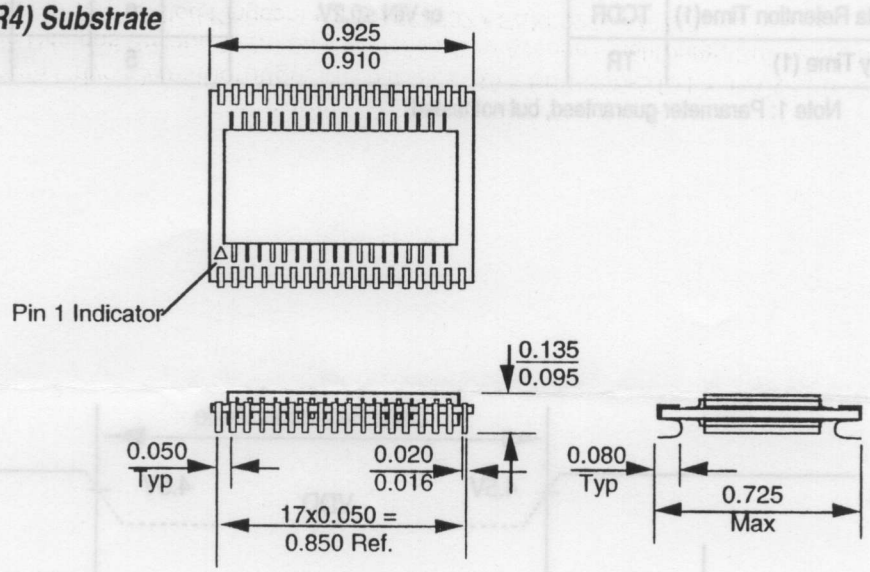
Ordering Information

Standard Power Part No.	Speed (ns)	Leads	Package Style	No.
EDI9F81025C70BPC	70	36	SOIC	198
EDI9F81025C85BPC	85	36	SOIC	198
EDI9F81025C100BPC	100	36	SOIC	198
Low Power with Data Retention **Part No.**	**Speed (ns)**	**Leads**	**Package Style**	**No.**
EDI9F81025LP70BPC	70	36	SOIC	198
EDI9F81025LP85BPC	85	36	SOIC	198
EDI9F81025LP100BPC	100	36	SOIC	198

Note: Performance grade/temperature range of part is designated by the last letter in the suffix to the part number.
To order an Industrial version of parts listed above, change EDI9F81025C85BPC to EDI9F81025C85BPI.

Package Description

Package No. 198
36 Lead SOIC Package
Plastic TSOP Chip Carriers on an Epoxy Laminate (FR4) Substrate



Electronic Designs Incorporated
• One Research Drive • Westborough, MA 01581 USA • 508-366-5151 • FAX 508-836-4850 •
Electronic Designs Europe Ltd. • Shelley House, The Avenue • Lightwater, Surrey GU18 5RF
United Kingdom • 0276 472637 • FAX: 0276 473748

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