

# MOSFET – Power, Dual, N-Channel, for 1-Cell Lithium-ion Battery Protection

12 V, 3.55 mΩ, 18 A

## EFC2J022NUZ

This Power MOSFET features a low on-state resistance. This device is suitable for applications such as power switches of portable machines. Best suited for 1-cell lithium-ion battery applications.

### Features

- 2.5 V Drive
- Common-Drain Type
- ESD Diode-Protected Gate
- Pb-Free, Halide Free and RoHS Compliant

### Applications

- 1-Cell Lithium-ion Battery Charging and Discharging Switch

### Specifications

#### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C)

Parameter	Symbol	Value	Unit
Source to Source Voltage	V <sub>SSS</sub>	12	V
Gate to Source Voltage	V <sub>GSS</sub>	±8	V
Source Current (DC)	I <sub>S</sub>	18	A
Source Current (Pulse) PW ≤ 100 μs, duty cycle ≤ 1%	I <sub>SP</sub>	76	A
Total Dissipation (Note 1)	P <sub>T</sub>	1.8	W
Junction Temperature	T <sub>j</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE RATINGS

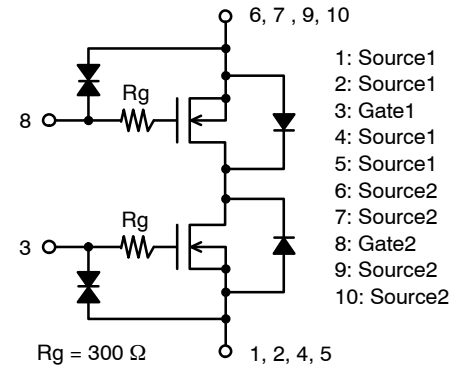
Parameter	Symbol	Value	Unit
Junction to Ambient (Note 1)	R <sub>θJA</sub>	69	°C/W

1. Surface mounted on ceramic substrate (5000 mm<sup>2</sup> × 0.8 mm).

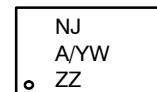
V <sub>SSS</sub>	R <sub>SS(on)</sub> Max	I <sub>S</sub> Max
12 V	3.55 mΩ @ 4.5 V	18 A
	3.75 mΩ @ 3.8 V	
	4.8 mΩ @ 3.1 V	
	6.9 mΩ @ 2.5 V	

### ELECTRICAL CONNECTION

#### N-Channel



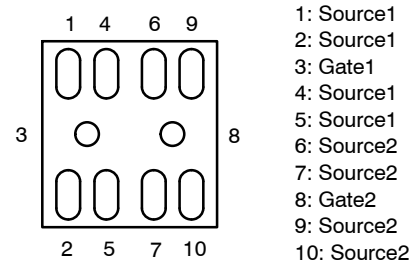
### MARKING DIAGRAM



WLCSP10  
1.84x1.96x0.10  
CASE 567PH

NJ = Specific Device Code  
A = Assembly Site  
YW = Assembly Start Week  
ZZ = Assembly Lot Number

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

# EFC2J022NUZ

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source to Source Breakdown Voltage	V <sub>(BR)SSS</sub>	I <sub>S</sub> = 1 mA, V <sub>GS</sub> = 0 V (Figure 1)	12	–	–	V
Zero-Gate Voltage Source Current	I <sub>SSS</sub>	V <sub>SS</sub> = 10 V, V <sub>GS</sub> = 0 V (Figure 1)	–	–	1	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±8 V, V <sub>SS</sub> = 0 V (Figure 2)	–	–	±10	μA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>SS</sub> = 6 V, I <sub>S</sub> = 1 mA (Figure 3)	0.3	–	1.3	V
Static Source to Source On-State Resistance	R <sub>SS(on)</sub>	I <sub>S</sub> = 5 A, V <sub>GS</sub> = 4.5 V (Figure 4)	1.9	2.75	3.55	mΩ
		I <sub>S</sub> = 5 A, V <sub>GS</sub> = 3.8 V (Figure 4)	2.0	2.9	3.75	mΩ
		I <sub>S</sub> = 5 A, V <sub>GS</sub> = 3.1 V (Figure 4)	2.25	3.1	4.8	mΩ
		I <sub>S</sub> = 5 A, V <sub>GS</sub> = 2.5 V (Figure 4)	2.5	3.5	6.9	mΩ
Turn-ON Delay Time	t <sub>d(on)</sub>	V <sub>SS</sub> = 6 V, V <sub>GS</sub> = 4.5 V, I <sub>S</sub> = 3 A, R <sub>g</sub> = 10 kΩ (Figure 5)	–	10	–	μs
Rise Time	t <sub>r</sub>		–	26	–	μs
Turn-OFF Delay Time	t <sub>d(off)</sub>		–	195	–	μs
Fall Time	t <sub>f</sub>		–	111	–	μs
Total Gate Charge	Q <sub>g</sub>	V <sub>SS</sub> = 6 V, V <sub>GS</sub> = 4.5 V, I <sub>S</sub> = 18 A (Figure 6)	–	46	–	nC
Forward Source to Source Voltage	V <sub>F(S-S)</sub>	I <sub>S</sub> = 3 A, V <sub>GS</sub> = 0 V (Figure 7)	–	0.75	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Test Circuits are Example of Measuring FET1 Side

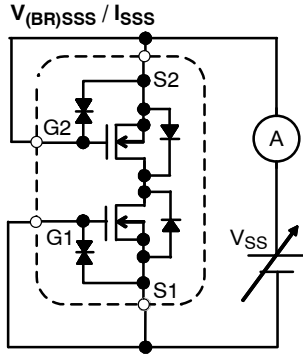


Figure 1. Test Circuit 1

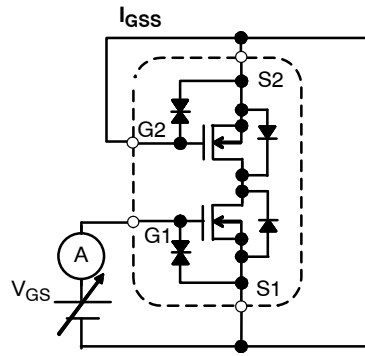
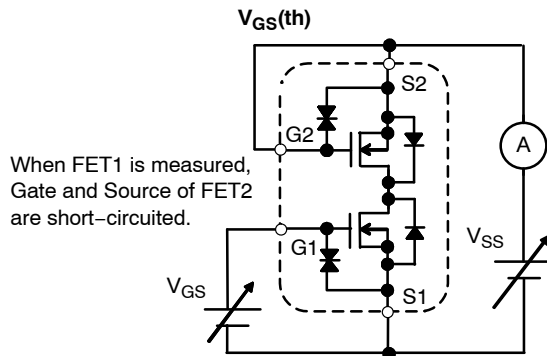


Figure 2. Test Circuit 2

When FET1 is measured, Gate and Source of FET2 are short-circuited.



When FET1 is measured, Gate and Source of FET2 are short-circuited.

Figure 3. Test Circuit 3

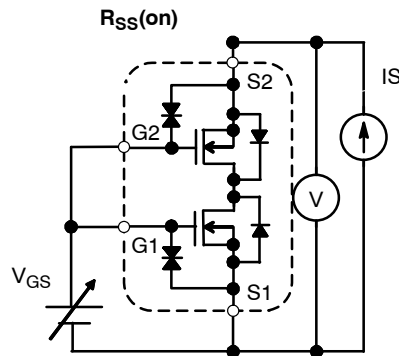
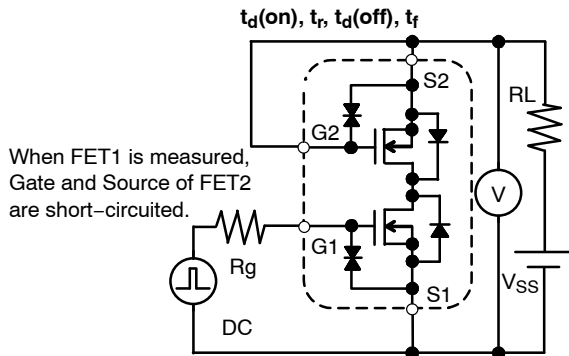
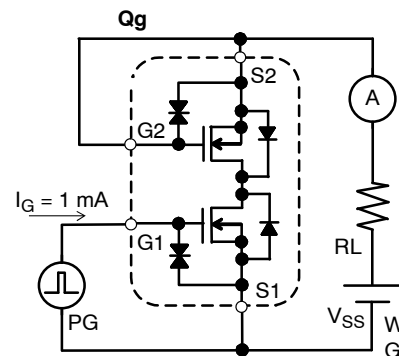


Figure 4. Test Circuit 4



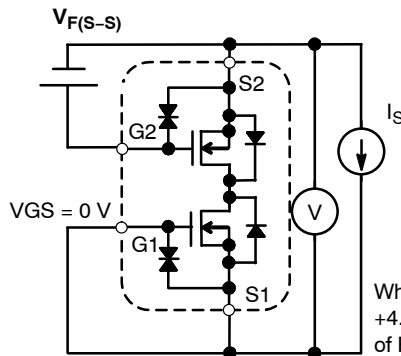
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Figure 5. Test Circuit 5



When FET1 is measured, Gate and Source of FET2 are short-circuited.

Figure 6. Test Circuit 6



When FET1 is measured, +4.5 V is added to VGS of FET2.

Figure 7. Test Circuit 7

NOTE: When FET2 is measured, the position of FET1 and FET2 is switched.

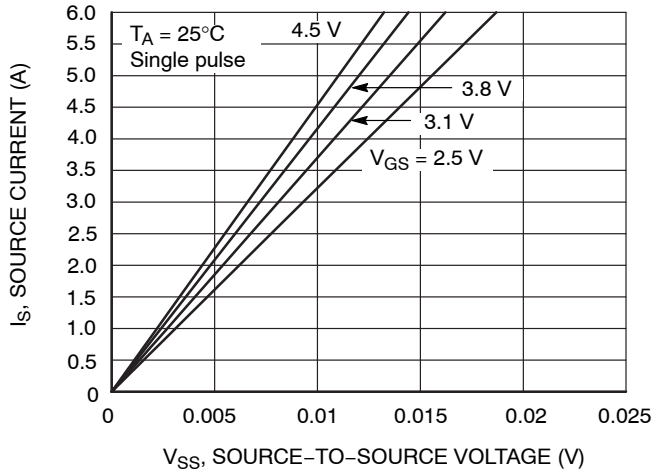


Figure 8. On-Region Characteristics

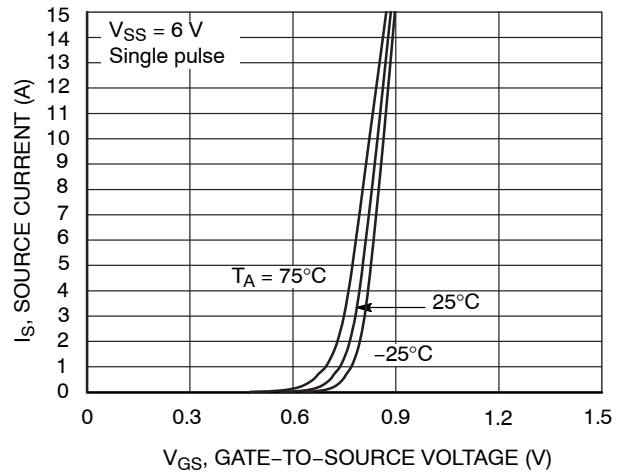


Figure 9. Transfer Characteristics

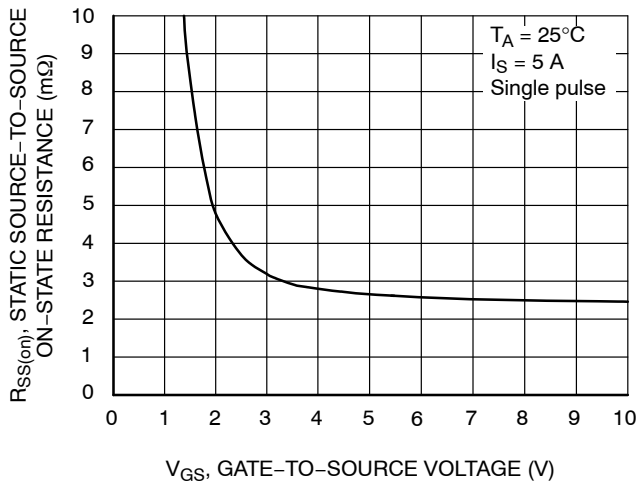


Figure 10. On-Resistance vs. Gate-to-Source Voltage

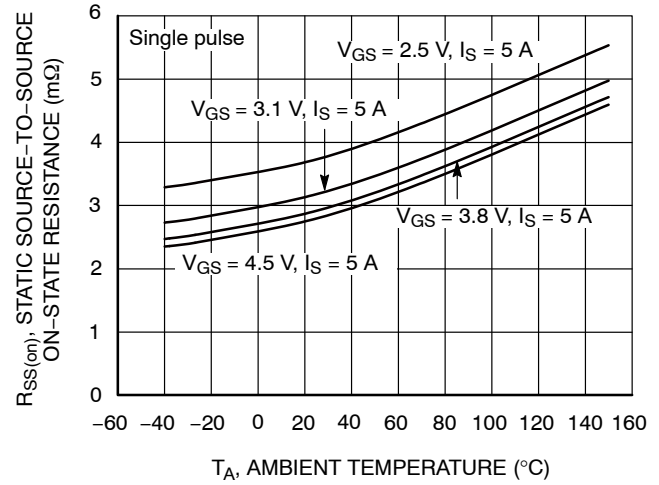


Figure 11. On-Resistance vs. Temperature

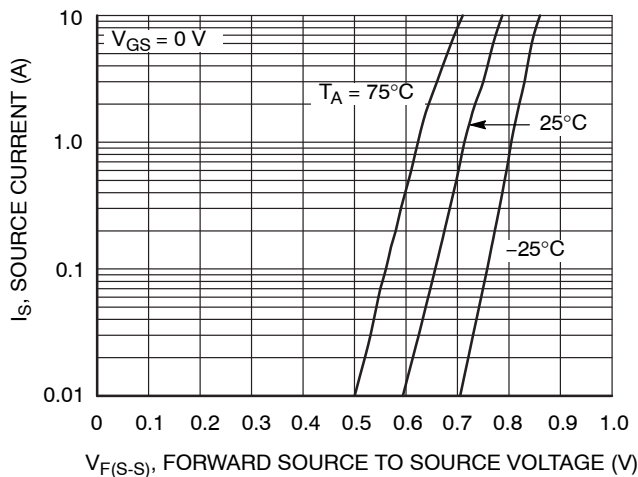


Figure 12. Forward Source-to-Source Voltage vs. Current

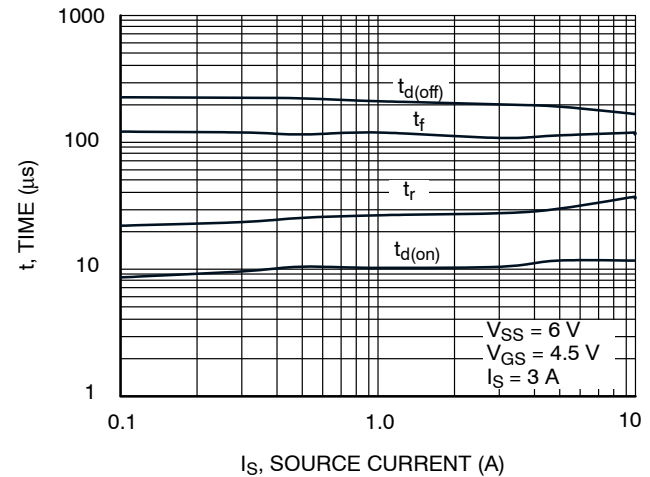


Figure 13. Switching Time vs. Source Current

# EFC2J022NUZ

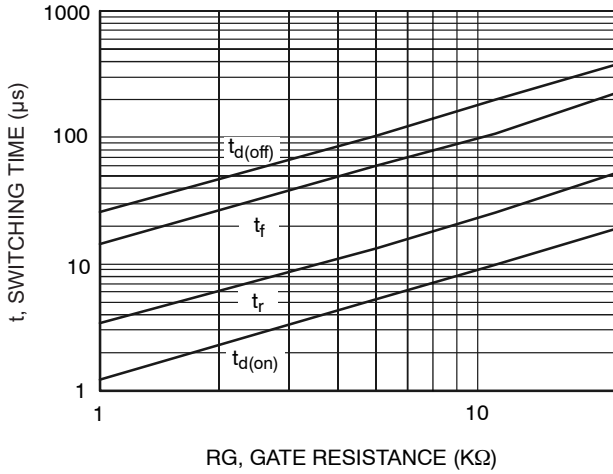


Figure 14. Switching Time vs. Gate Resistance

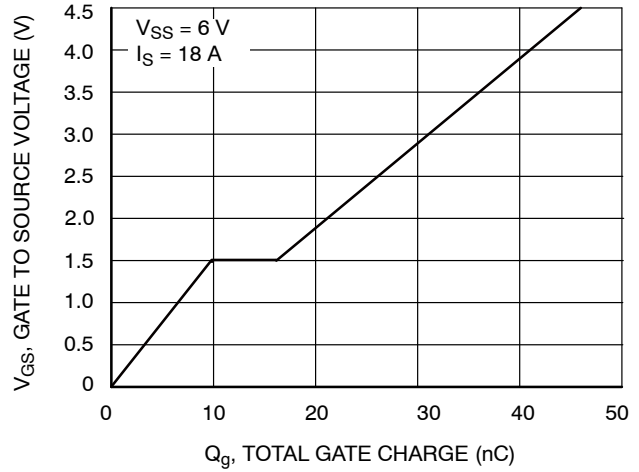


Figure 15. Gate-To-Source Voltage vs. Total Charge

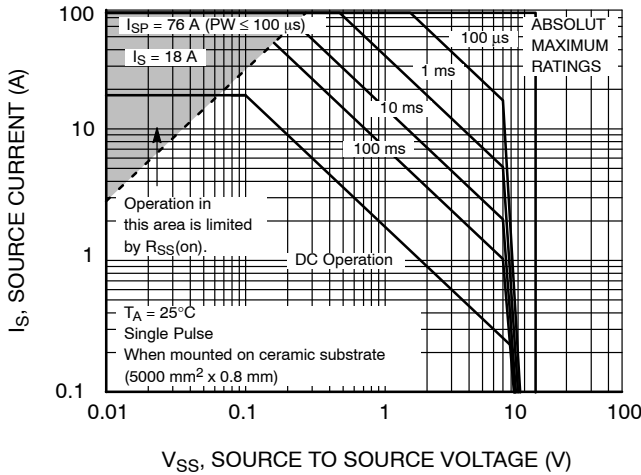


Figure 16. Safe Operating Area

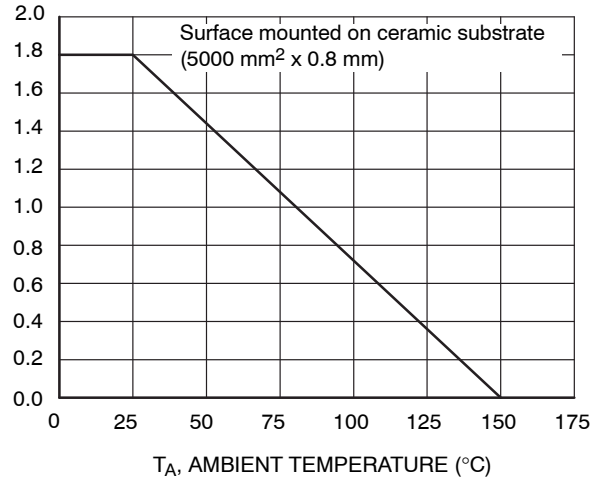


Figure 17. Total Dissipation vs. Temperature

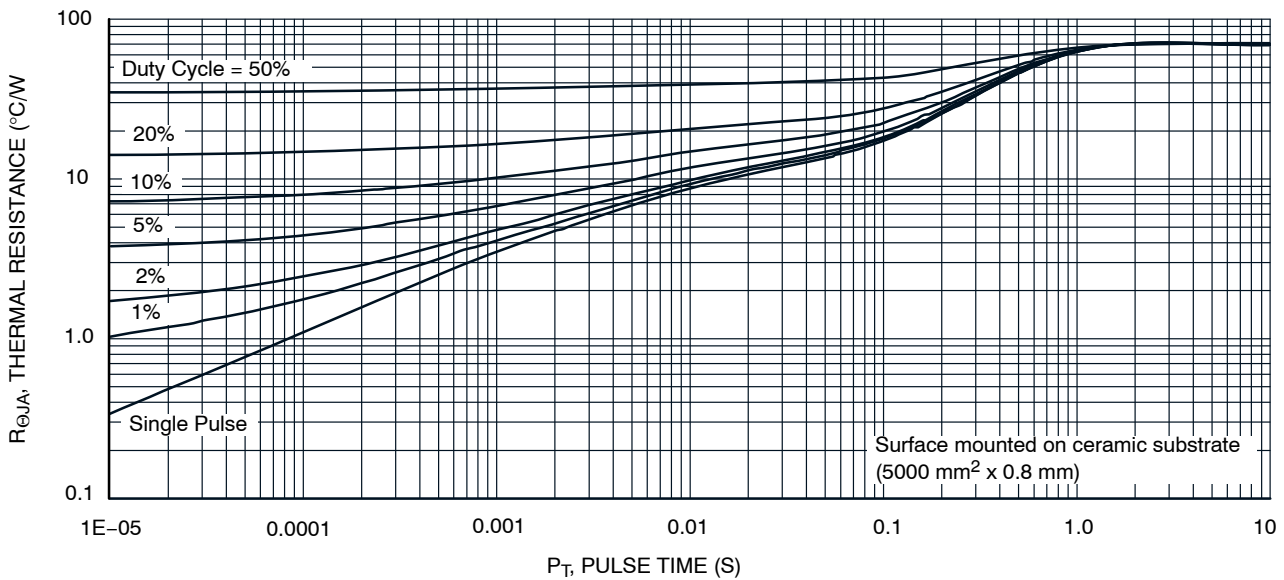


Figure 18. Thermal Response

# EFC2J022NUZ

## ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup> (Qty / Packing)
EFC2J022NUZTCG	NJ	WLCSP10 1.84x1.96x0.10 (Pb-Free / Halogen Free)	5000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

Note on usage: Since the EFC2J022NUZ is a MOSFET product, please avoid using this device in the vicinity of highly charged objects. Please contact sales for use except the designated application.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

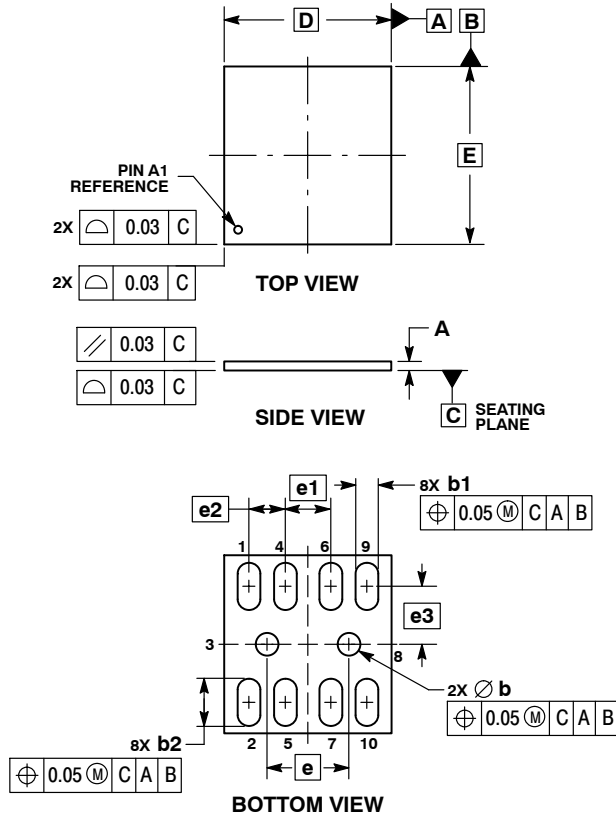
ON Semiconductor®



SCALE 4:1

WLCSP10 1.84x1.96x0.10  
CASE 567PH  
ISSUE A

DATE 06 APR 2017

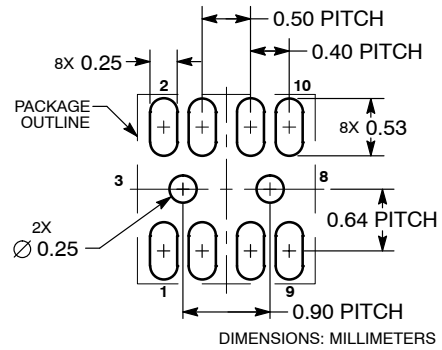


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.08	0.10	0.12
b	0.22	0.25	0.28
b1	0.22	0.25	0.28
b2	0.50	0.53	0.56
D	1.84 BSC		
E	1.96 BSC		
e	0.90 BSC		
e1	0.50 BSC		
e2	0.40 BSC		
e3	0.64 BSC		

### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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