ELECTRONIC CIRCUIT

EG2113D Datasheet

High-power MOS transistor, IGBT transistor gate driver chip

 REV 1.0

Version Change record

Version №	Date	Description
V1.0	May 18, 2019	First draft of the EG2113D Datasheet

Contents

EG2113D D a t a s h e e t V1.0

1. Features

- High-end suspension bootstrap power supply design, withstand voltage up to 600V
- Integrated internal bootstrap diode,fewer peripheral devices
- Maximum frequency support 500KHZ
- Low-side VDD voltage range 3.3 V-5V
- Low-side VCC voltage range 10V-20V
- Output current capability IO+/- 2A/2A
- Built-in dead zone control circuit
- Comes with locking function, completely eliminate the upper and lower tube output is turned on at the same time
- HIN input channel is active high to control the high-side HO output
- LIN input channel is active high to control the low-side LO output
- Quiescent current less than 50uA
- Package form: SOW16 and SOP16

2. Description

EG2113D is a cost-effective high-power MOS transistor, IGBT transistor Gate Drive dedicated chip, integrated logic signal input processing circuit, dead zone control circuit, latch circuit, level displacement circuit, pulse filter circuit, bootstrap diode and output drive circuit, dedicated to brushless motor controller drive circuit.

EG2113D high-end operating voltage up to 600V, low-end VCC supply voltage range is wide 10V ~ 20V, static power consumption is less than 50uA.The chip has a latching function to prevent the output power tube is turned on at the same time,the input channel HIN and LIN built - in a 200k pull-down resistor, when the input floating so that the upper and lower power MOS transistor is turned off, the output current capability IO+/ - 2A/2A, using SOP16 and SOW16 package.

3. Application Areas

- Sine wave inverter
- Variable frequency pump controller
- Square wave inverter
- Electric vehicle controller
- Brushless motor driver
- High voltage Class-D power amplifier

4. Pin

4.1. Pin definition

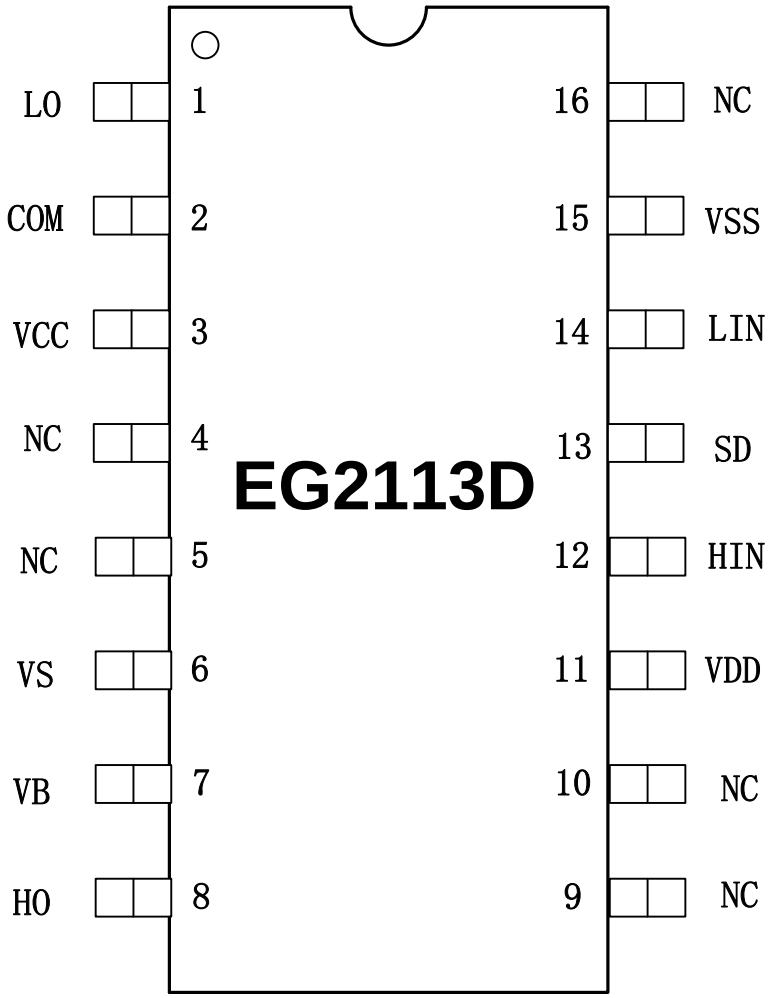


Figure 4-1. SOW16 and SOP16L

Note: SOW16 and SOP16 two packages, but the pin is exactly the same.

4.2. Pin description

Pin serial №	Pin name	I/O	Description
1	LO	O	The output controls the conduction and shutdown of the low-side MOS transistor
2	COM	GND	Power ground
3	VCC	Power	Chip power input, voltage range 10V-20V,an external high frequency 0.1 uF bypass capacitor
4	NC	-	Empty feet
5	NC	-	Empty feet
6	VS	O	High-end suspended Ground end
7	VB	Power	High-end suspended power supply
8	HO	O	The output controls the on and off of the high-side MOS transistor
9	NC	-	Empty feet
10	NC	-	Empty feet
11	VDD	Power	Logic circuit power supply terminal, voltage range 3.3 V-5V,an external high frequency 0.1 uF bypass capacitor
12	HIN	I	Logic input signal active high to control the high-side power MOS transistor is turned on and off "0" is the off power MOS transistor "1" is the open power MOS transistor
13	SD	I	Logic input, Active High, used to turn off the outputs of HO and LO
14	LIN	I	Logic input signal active low, control the low-side power MOS transistor is turned on and off "0" is the off power MOS transistor "1" is the open power MOS transistor
15	VSS	GND	Ground end of the chip
16	NC		Empty feet

5. Block diagram

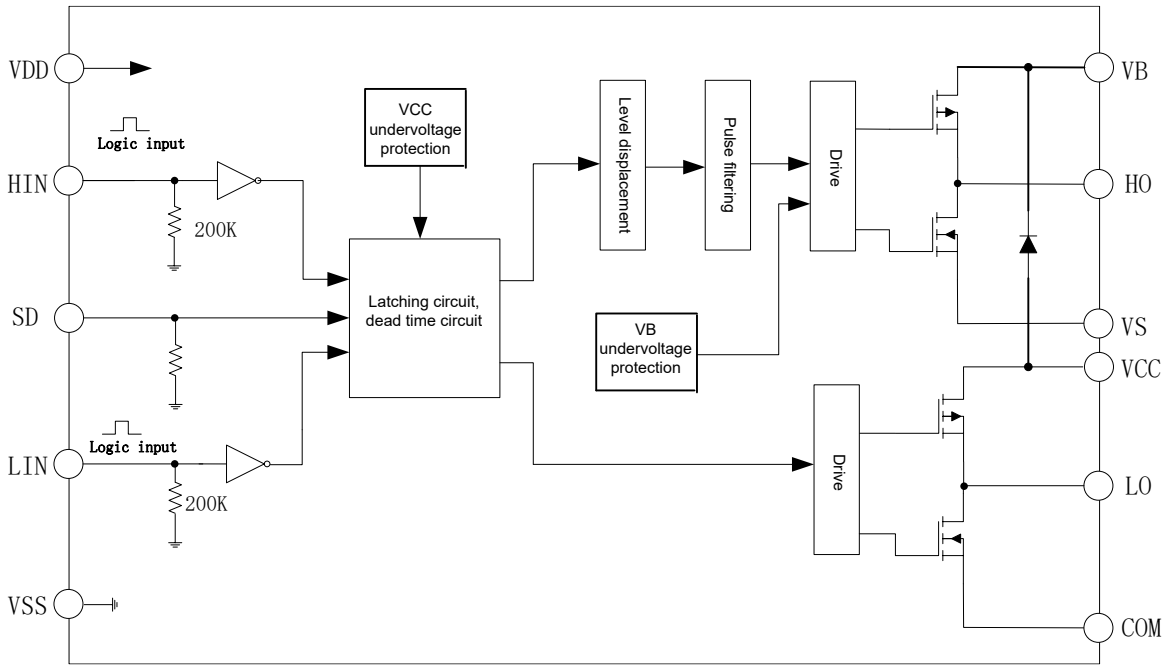


Figure 5-1. EG2113D block diagram

6. Typical application circuit

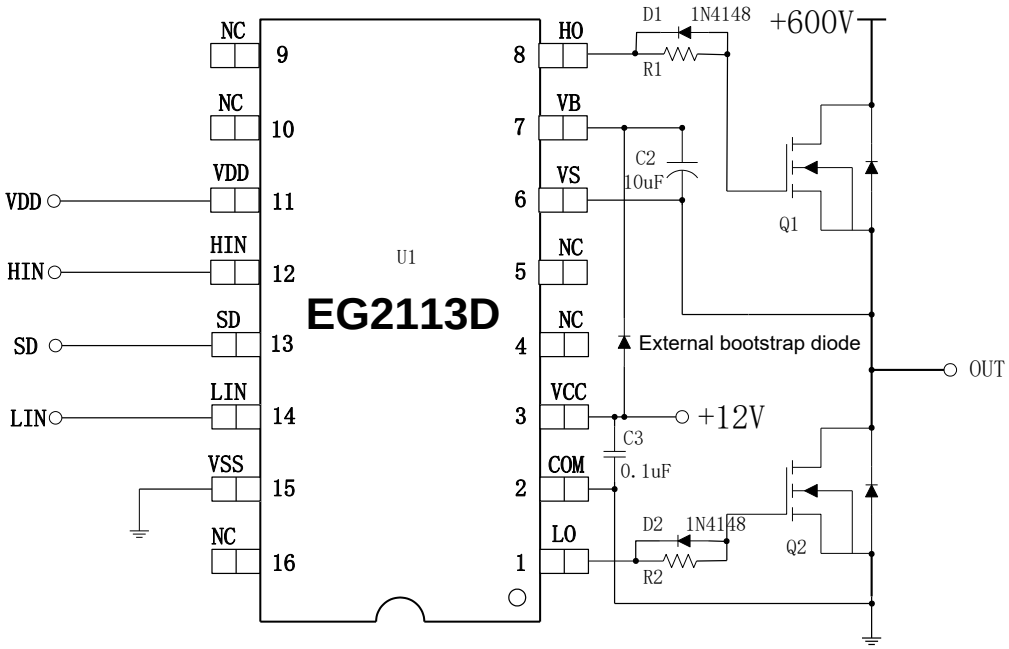


Figure 6-1. EG2113D typical application circuit diagram

7. Electrical characteristics

7.1 Limit parameters

Without further explanation, at TA=25℃ conditions

Symbols	Parameter name	Test conditions	Min.	Max.	Units
High side floating absolute voltage	VB	-	-0.3	600	V
High side floating supply offset voltage	VS	-	VB-20	VB+0.3	V
High side floating supply offset voltage	HO	-	VS-0.3	VB+0.3	V
Low side output voltage	LO	-	-0.3	VCC+0.3	V
Low side and logic fixed supply voltage	VCC	-	-0.3	20	V
Power supply	VDD	-	-0.3	5	V
Logic input voltage (HIN)	HIN	-	-0.3	VDD+0.3	V
Logic input voltage (LIN)	LIN	-	-0.3	VDD+0.3	V
TA	Ambient temperature	-	-45	105	℃
Tstr	Storage temperature	-	-55	150	℃
TL	Lead temperature (soldering, 10 seconds)	T=10S	-	300	℃

Note: exceeding the listed limit parameters may cause permanent damage to the chip, operating in extreme conditions for a long time will affect the reliability of the chip.

7.2 Typical parameters

Without further explanation, at TA=25℃, Vcc=15v, load capacitance CL=1NF conditions

Parameter name	Symbols	Test conditions	Min.	Typical	Max.	Units
Power supply	Vcc	-	10	15	20	V
Quiescent current	Icc	Input dangling，VCC=15V	-	50	100	uA
Input logic signal high potential	Vin(H)	All input control signals	2.5	-	-	V
Input logic signal low potential	Vin(L)	All input control signals	-0.3	0	1.0	V
Current at the high level of the input logic signal	Iin(H)	Vin=5V	-	-	20	uA
Input logic signal low current	Iin(L)	Vin=0V	-20	-	-	uA
VCC supply undervoltage shutdown feature						
VCC turn-on voltage	Vcc(on)	-	7.4	8.4	9.4	V
Vcc shutdown voltage	Vcc（off）	-	7.0	8.0	9.0	V
VB supply undervoltage shutdown feature						
VB turn-on voltage	VB(on)	-	7.6	8.6	9.6	V
VB shutdown voltage	VB（off）	-	7.2	8.2	9.2	V
Low-side output LO switching time characteristics						
On delay	Ton	SeeFigure7-1	-	350	450	ns
Off delay	Toff	See Figure 7-1	-	200	300	ns
Rise Time	Tr	See Figure 7-1	-	20	25	ns
Fall time	Tf	See Figure 7-1	-	15	20	ns
High-side output HO switching time characteristics						
On delay	Ton	See Figure 7-2	-	350	400	ns
Off delay	Toff	See Figure 7-2	-	200	400	ns
Rise Time	Tr	See Figure 7-2	-	20	25	ns
Fall time	Tf	See Figure 7-2	-	15	20	ns
Dead time characteristics						
Dead time	DT	See Figure 7-3	50	150	250	ns
IO output maximum drive capability						
IO output pull current	IO+	Vo=0V,VIN=VIH		+2	-	A

		PW≤10uS				
IO Output sink current	IO-	Vo=12V,VIN=VIL PW≤10uS		-2	-	A

7.3 Switching time characteristics and dead time waveform diagram

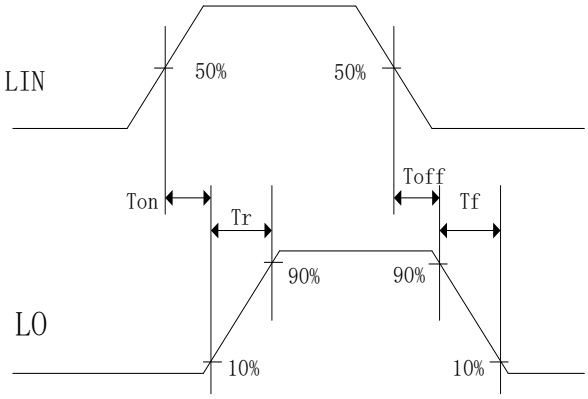


Figure 7-1. Low-side output LO switching time waveform diagram

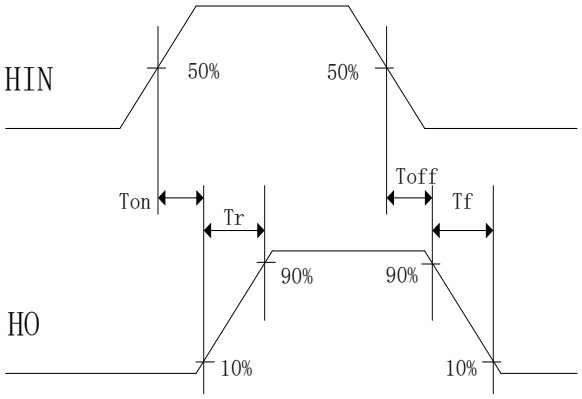


Figure 7-2. High-side output HO switching time waveform diagram

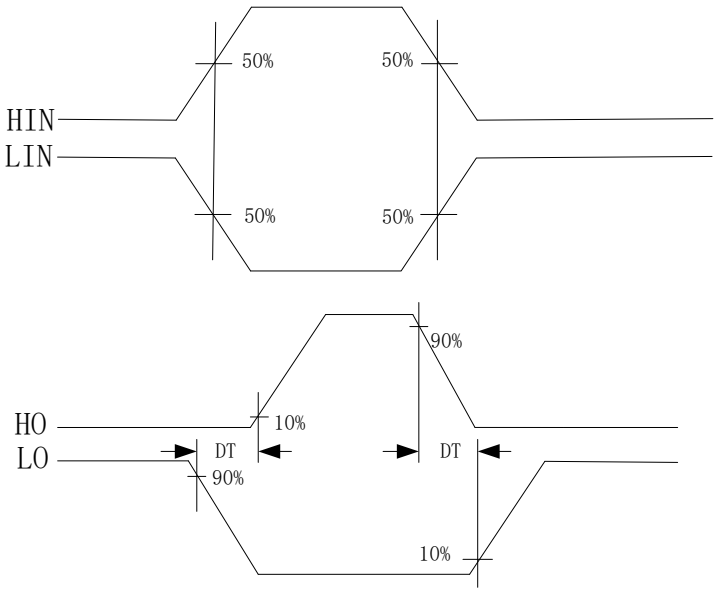


Figure 7-3. Dead time waveform diagram

8. Application design

8.1 VCC terminal supply voltage

For different MOS transistor, select a different driving voltage,high voltage to open the MOS transistor recommended power supply Vcc operating voltage is typically 10V-15V; low voltage to open the MOS transistor recommended power supply VDD operating voltage 3.3 V-5V.

8.2 Input logic signal requirements and output driver characteristics

The main functions of the EG2113D are logic signal input processing,dead time control, level translation function, floating bootstrap power structure and upper and Lower Bridge totem pole output.Logic signal input high threshold of 2.5 V or more, low threshold of 1.0 V or less, the requirements of the output current of the logic signal is small,you can make the MCU output logic signal is directly connected to the EG2113D input channel.

Up to 2A and the maximum output current up to 2A, the high-end arm channel can withstand 600V voltage, the input logic signal and the output control signal between the conduction delay is small,the low-end output opening conduction delay of 350ns, turn-off conduction delay of 200ns, high-end output opening conduction delay of 350ns, turn-off conduction delay of 200ns.The rise time of the low-side output is 25ns, the fall time of the shutdown is 15ns, the rise time of the high-side output is 25ns, the fall time of the shutdown is 15ns.

Input signal and output signal logic function diagram shown in Figure 8-2：

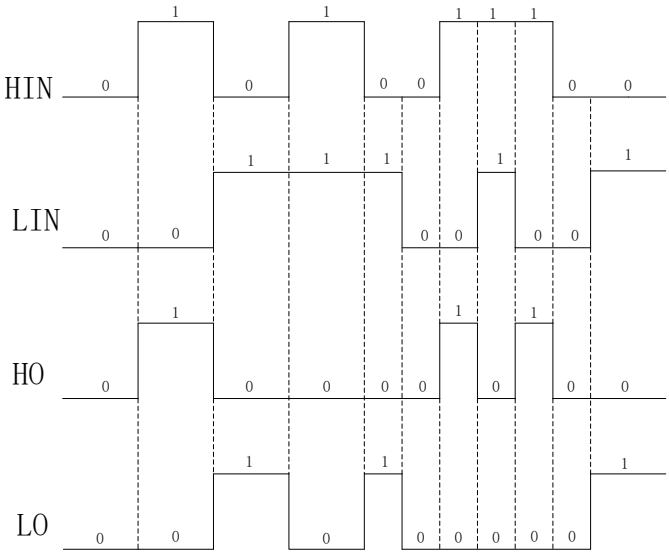


Figure 8-2. Input signal and output signal logic function diagram

Logic truth table for input and output signals：

Input		Output	
Input and output logic			
HIN	LIN	HO	LO
0	**0**	0	**0**
0	1	0	1
1	0	1	0
1	**1**	**0**	0

From the truth table, when the input logic signal HIN is “1” and LIN is “0”, The Drive control output HO is “1” on the tube is opened, LO is “0” under the tube is turned off; when the input logic signal HIN is “0” and LIN is “1”, the drive control output HO is “0” on the tube is turned off, LO is “1” under the tube is opened; 0 “the upper and lower power tube is turned off at the same time; internal logic processor to prevent the controller output, the lower power tube is turned on at the same time, with mutual locking function.

8.3 Bootstrap circuit

The EG2113D adopts a bootstrap floating drive power structure to greatly simplify the design of the drive power supply. Only one power supply voltage VCC can complete the drive of the two power switching devices of the high-end N-channel MOS transistor and the low-end N-channel MOS transistor, which brings practical application. It's a great convenience. EG2113D can use an internal bootstrap diode as shown in Figure 8-3 and a bootstrap capacitor to automatically complete the bootstrap boost function. It is assumed that the C bootstrap capacitor has been charged to a sufficient voltage during the period when the lower tube is turned on and the upper tube is turned off (Vc=VCC)), when the HO output high level, when the upper tube is turned on and the lower tube is turned off, the voltage on the VC bootstrap capacitor will be equivalent to a voltage source as the power supply for the internal drivers VB and VS to complete the drive of the high-side N-channel MOS tube.

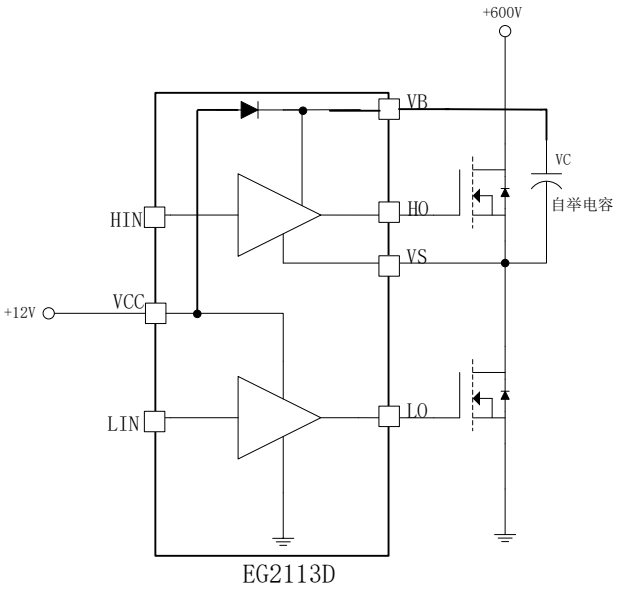
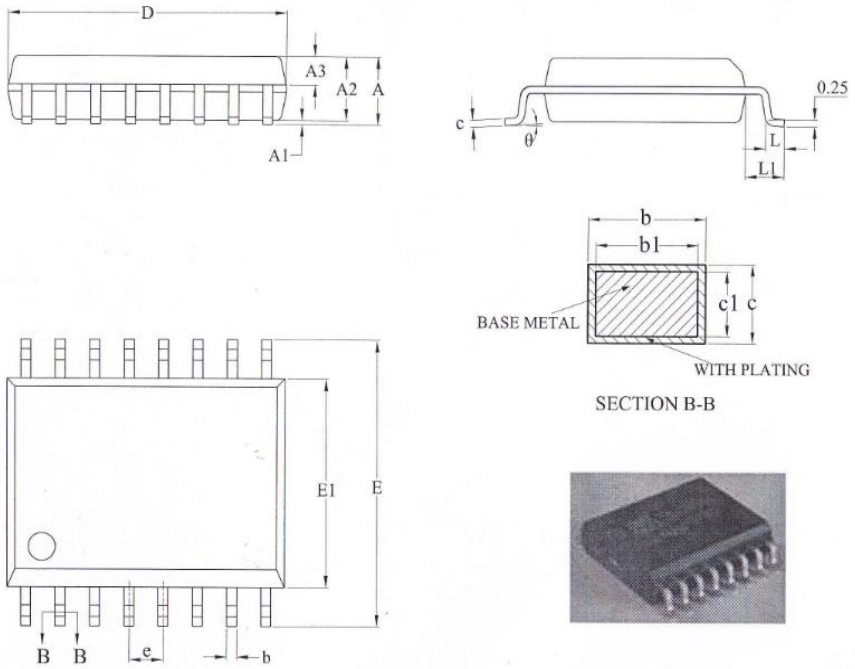


Figure 8-3. EG2113D bootstrap circuit structure

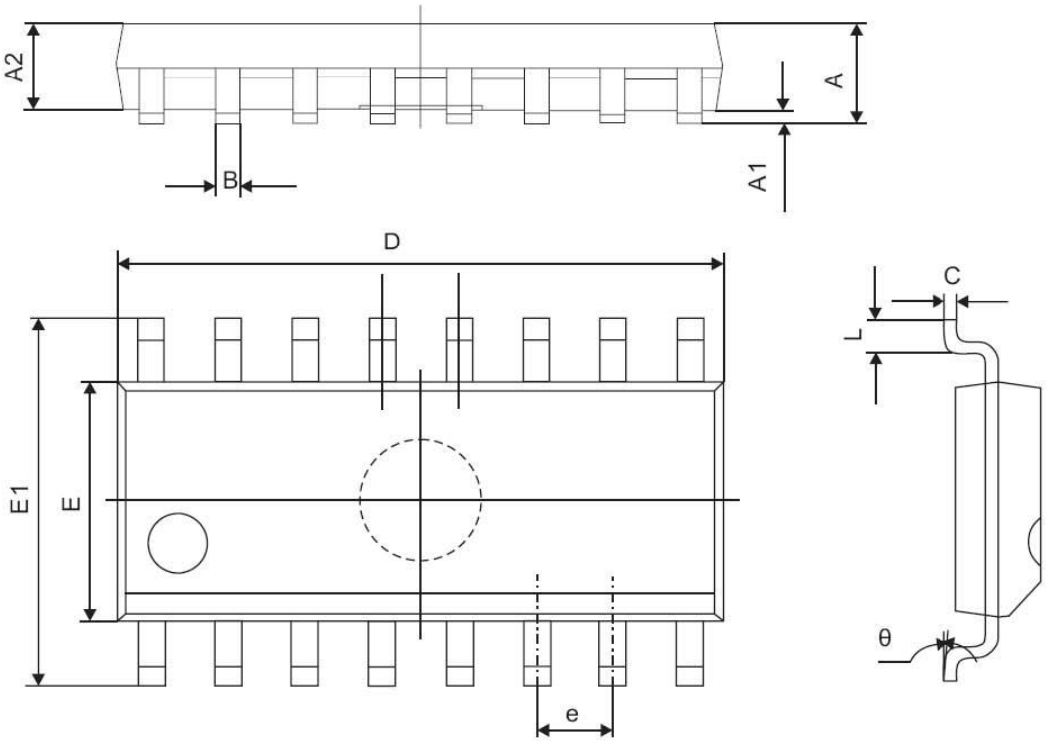
9. Package size

9.1 SOW16 package size



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.65
A1	0.10	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	—	0.43
b1	0.34	0.37	0.40
c	0.25	—	0.29
c1	0.24	0.25	0.26
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.55	—	0.85
L1	1.40REF		
θ	0	—	8°

9.2 SOP16 package size



Symbols	Size (mm)	
	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
B	0.330	0.510
C	0.190	0.250
D	9.800	10.000
E	3.800	4.000
E1	5.800	6.300
e	1.270（TYP）	
L	0.400	1.270
Θ	0°	8°