

UPDATED 07/12/2007

14.00-14.50 GHz 5-Watt Internally-Matched Power FET

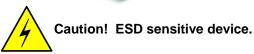
FEATURES

- 14.00-14.50 GHz Bandwidth
- Input/Output Impedance Matched to 50 Ohms
- +37.5 dBm Output Power at 1dB Compression
- 7.5 dB Power Gain at 1dB Compression
- 35% Power Added Efficiency
- **Hermetic Metal Flange Package**
- 100% Tested for DC, RF, and R_{TH}



The EID1414A1-5 is a high power, highly linear, single stage MFET amplifier in a flange mount package. This amplifier features Excelics' unique PHEMT transistor technology.





ELECTRICAL CHARACTERISTICS (Ta = 25°C)

SYMBOL	PARAMETERS/TEST CONDITIONS ¹	MIN	TYP	MAX	UNITS
P _{1dB}	Output Power at 1dB Compression $f = 14.00-14.50GHz$ $V_{DS} = 10 \text{ V}, I_{DSQ} = 1200\text{mA}$	37.0	37.5		dBm
G _{1dB}	Gain at 1dB Compression $f = 14.00-14.50GHz$ $V_{DS} = 10 \text{ V}, I_{DSQ} = 1200\text{mA}$	6.5	7.5		dB
ΔG	Gain Flatness $f = 14.00-14.50GHz$ $V_{DS} = 10 \text{ V}, I_{DSQ} = 1200\text{mA}$			±0.6	dB
PAE	Power Added Efficiency at 1dB Compression $V_{DS} = 10 \text{ V}, I_{DSQ} = 1200\text{mA}$ f = 14.00-14.50GHz		35		%
Id _{1dB}	Drain Current at 1dB Compression f = 14.00-14.50GHz		1400	1800	mA
I _{DSS}	Saturated Drain Current $V_{DS} = 3 \text{ V}, V_{GS} = 0 \text{ V}$		2080	2880	mA
V_P	Pinch-off Voltage $V_{DS} = 3 \text{ V}, I_{DS} = 20 \text{ mA}$		-2.5	-4.0	V
R _{TH}	Thermal Resistance ²		5.5	6.0	°C/W

Notes:

- Tested with 100 Ohm gate resistor.
- Overall Rth depends on case mounting.



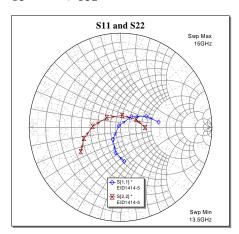
UPDATED 07/12/2007 14.00-14.50 GHz 5-Watt Internally-Matched Power FET ABSOLUTE MAXIMUM RATINGS FOR CONTINUOUS OPERATION^{1,2}

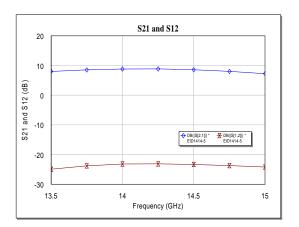
SYMBOL	CHARACTERISTIC	VALUE		
V_{DS}	Drain to Source Voltage	10 V		
V_{GS}	Gate to Source Voltage	-4.5 V		
I _{DS}	Drain Current	IDSS		
I_{GSF}	Forward Gate Current	40 mA		
P _{IN}	Input Power	@ 3dB compression		
P_T	Total Power Dissipation	23 W		
T_CH	Channel Temperature	150°C		
T_{STG}	Storage Temperature	-65/+150°C		

- Operating the device beyond any of the above ratings may result in permanent damage or reduction of MTTF. Bias conditions must also satisfy the following equation $P_T < (T_{CH} T_{PKG})/R_{TH}$; where $T_{PKG} = T_{PKG}$ temperature of package, and $P_T = (V_{DS} * I_{DS}) - (P_{OUT} - P_{IN}).$

PERFORMANCE DATA

Typical S-Parameters (T= 25°C, 50Ω system, de-embedded to edge of package) $V_{DS} = 10 \text{ V}, I_{DSO} = 1200 \text{mA}$





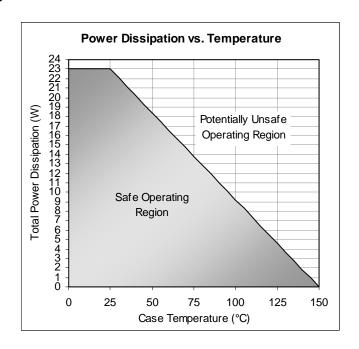
FREQ	S1	11	S2	21	S ^r	12	Si	22
(GHz)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
13.60	0.3380	-90.79	2.5944	-176.44	0.0603	170.24	0.4755	-153.89
13.70	0.2971	-97.44	2.6490	175.75	0.0609	161.63	0.4390	-160.10
13.80	0.2552	-105.20	2.6962	167.96	0.0630	153.33	0.3950	-166.55
13.90	0.2045	-112.85	2.7481	159.02	0.0655	145.93	0.3527	-173.84
14.00	0.1524	-122.48	2.7628	151.12	0.0694	136.76	0.3036	177.97
14.10	0.0956	-135.11	2.7767	142.28	0.0683	128.89	0.2507	166.52
14.20	0.0411	-169.43	2.7844	133.47	0.0703	119.55	0.2036	152.97
14.30	0.0435	81.13	2.7578	124.71	0.0701	111.32	0.1626	134.59
14.40	0.1025	54.46	2.7359	115.60	0.0691	101.22	0.1352	109.08
14.50	0.1651	42.41	2.6853	106.41	0.0682	91.51	0.1272	81.88
14.60	0.2214	33.93	2.6150	98.28	0.0693	84.19	0.1428	53.54
14.70	0.2802	26.00	2.5646	89.44	0.0673	75.38	0.1711	33.11
14.80	0.3322	20.00	2.4814	81.16	0.0659	66.29	0.2059	19.24
14.90	0.3800	13.06	2.3964	72.99	0.0653	58.58	0.2374	7.89



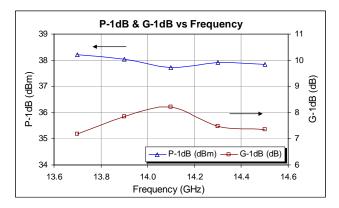
UPDATED 07/12/2007

14.00-14.50 GHz 5-Watt Internally-Matched Power FET

Power De-rating Curve



Typical Power Data ($V_{DS} = 10 \text{ V}$, $I_{DSQ} = 1200 \text{ mA}$)



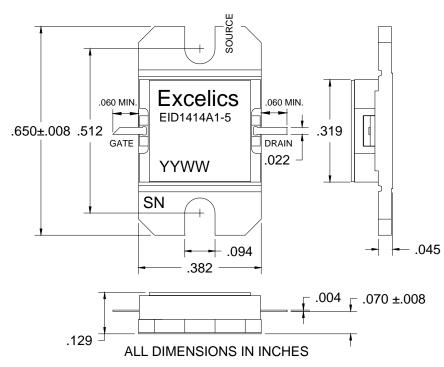


UPDATED 07/12/2007

14.00-14.50 GHz 5-Watt Internally-Matched Power FET

PACKAGE OUTLINE

Dimensions in inches, Tolerance ± .005 unless otherwise specified



ORDERING INFORMATION

Part Number	Grade ¹	f _{Test} (GHz)	P _{1dB} (min)
EID1414A1-5	Industrial	14.00-14.50 GHz	37.0

Notes:

- 1. Contact factory for military and hi-rel grades.
- 2. Exact test conditions are specified in "Electrical Characteristics" table.

DISCLAIMER

EXCELICS SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. EXCELICS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN.

LIFE SUPPORT POLICY

EXCELICS SEMICONDUCTOR PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF EXCELICS SEMICONDUCTOR, INC. AS HERE IN:

- 1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
- 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness