EK6703

Rev. 1.1

DATA SHEET

TFT LCD Timing Controller

fitipower integrated technology inc.

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TFT LCD Timing Controller

1. GENERAL DESCRIPTION

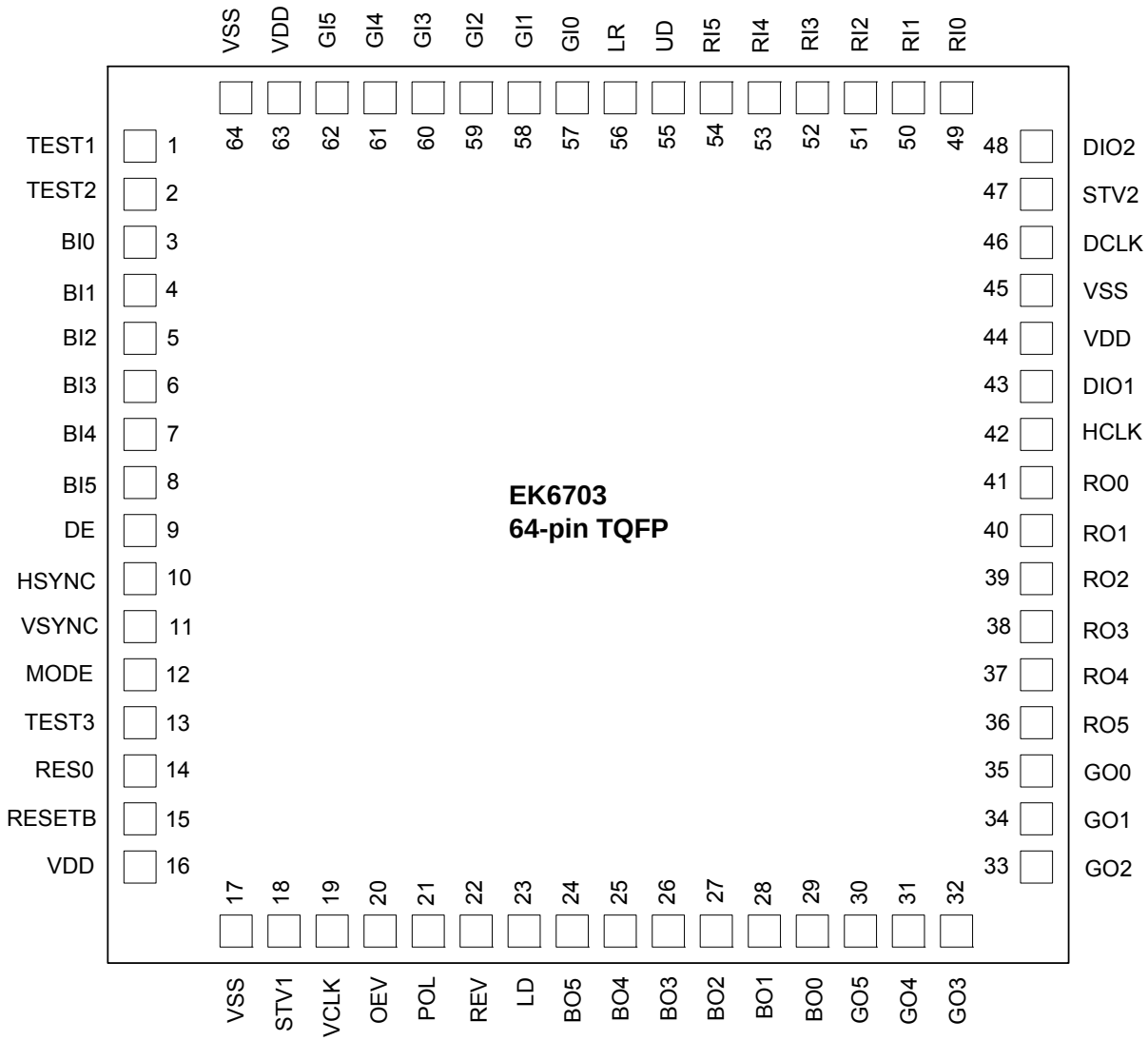
The EK6703 is a TFT LCD timing controller. It resides on the flat panel display and provides the interface signal and timing control between graphics and a TFT-LCD system.

The EK6703 chip links the panel's system interface to the display via the input data bus. The data is then routed to the source and gate display drivers.

2. FEATURES

- Wide supply voltage: 2.7V to 3.6V.
- 6 bit data single port input and single port output.
- Support Up/Down and Left/Right image rotation.
- Support 3 display resolutions that are 640 x 480, 800 x 480, 800 x 600.
- Support both DE and Sync mode.
- Support Flicker Free Type 2.
- Built-in Power on Reset.
- Green-64 pin TQFP.

3. PIN ASSIGNMENT



4. PIN DESCRIPTION

Pin Name	Pin No.	Pin Type	Description		
DCLK	46	Input	Clock signal; latching data at the falling edge.		
RI5 - RI0	54 - 49	Input	Data input.		
GI5 - GI0	62 - 57	Input	6-bit data.		
BI5 - BI0	8 - 3	Input	-		
DE	9	Input	Data enable signal.		
HSYNC	10	Input	Horizontal sync input. Negative polarity.		
VSYNC	11	Input	Vertical sync input. Negative polarity.		
MODE	12	Input	DE/HV MODE select. Normally pulled high. 1: DE mode. 0:HV mode		
RES0	14	Input	Resolution Selection 1:800*600 and 800*480 0:640*480		
RESETB	15	Input	Reset pin, active low. Normally pulled high.		
STV1, STV2	18, 47	Output	Gate Start Pulse.		
VCLK	19	Output	Gate driver shift clock.		
OEV	20	Output	Gate output off signal.		
POL	21	Output	Polarity invert signal of Source Driver IC.		
REV	22	Output	Data polarity invert control signal output.		
LD	23	Output	Latch Pulse of Source Driver IC.		
RO5 - RO0	36 - 41	Output	Data Output		
GO5 - GO0	30 - 35	Output	Data Output		
BO5 - BO0	24 - 29	Output	Data Output		
HCLK	42	Output	Source driver shift clock.		
DIO1, DIO2	43, 48	Output	Source Start Pulse.		
UD	55	Input	UD = 1	STV1 Output	STV2 Tristate
			UD = 0	STV2 Output	STV1 Tristate
LR	56	Input	LR = 1	DIO1 Output	DIO2 Tristate
			LR = 0	DIO2 Output	DIO1 Output
TEST1, TEST2	1, 2	Input	Test Pin, Please pull high or NC.		
TEST3	13	Input	Please pull high in normal operation.		
VDD	16, 44, 63	Power	Power supply for digital circuits.		
VSS	17, 45, 64	Power	Ground pins for digital circuits.		

5. INPUT TIMING

640 × 480

SYNC MODE	640 × 480			
Parameter	Min.	Typ.	Max.	Unit
Clock Freq.	23	25	30	MHZ
H-sync Total	750	800	900	CLK
H-sync Pulse Width	1	1	1	CLK
H-sync Pulse Width + Back Porch	46	46	46	CLK
H-sync Front poach	64	114	214	CLK
H-Active	640	640	640	CLK
V-sync Total	515	525	560	LINE
V-sync Pulse Width	1	1	1	LINE
V-sync Pulse Width + Back Porch	34	34	34	LINE
V-sync Front poach	1	11	46	LINE
V-Active	480	480	480	LINE
DE MODE	**640 × 480**			
H-sync Total	750	800	900	CLK
H-Active	640	640	640	CLK
H-Blanking	110	160	260	CLK
V-sync Total	515	525	560	LINE
V-Active	480	480	480	LINE
V-Blanking	35	45	80	LINE

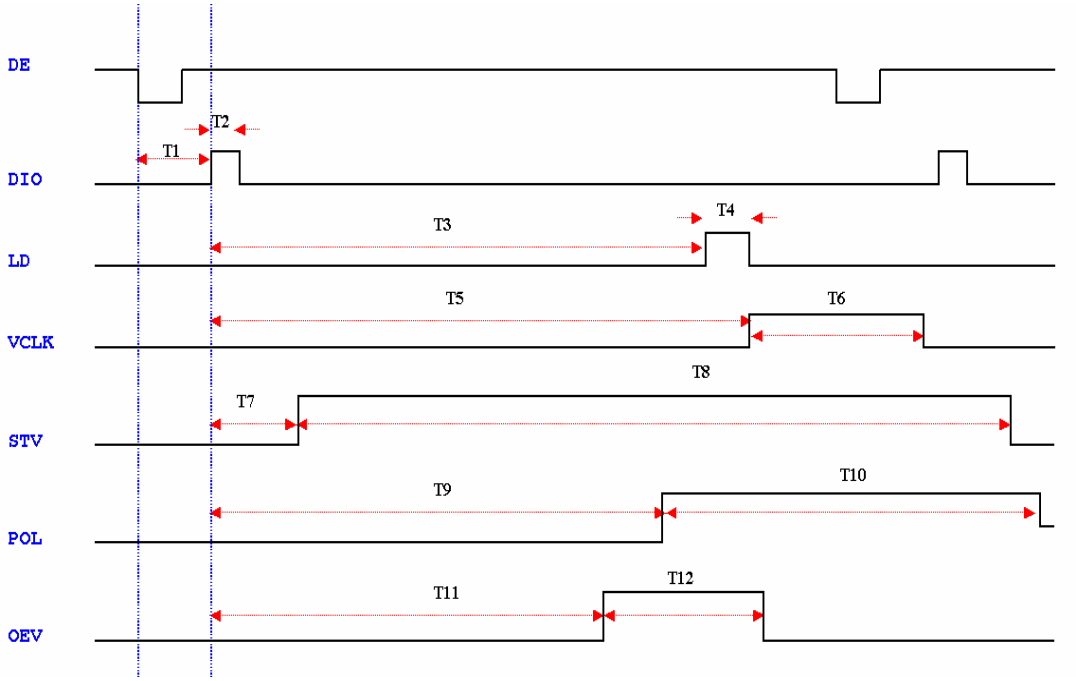
800 × 600

SYNC MODE	800 × 600			
Parameter	Min.	Typ.	Max.	Unit
Clock Freq.	32	40.2	42.9	MHZ
H-sync Total	850	1056	1100	CLK
H-sync Pulse Width	1	1	1	CLK
H-sync Pulse Width + Back Porch	46	46	46	CLK
H-sync Front poach	4	210	254	CLK
H-Active	800	800	800	CLK
V-sync Total	628	635	650	LINE
V-sync Pulse Width	1	1	1	LINE
V-sync Pulse Width + Back Porch	23	23	23	LINE
V-sync Front poach	5	12	27	LINE
V-Active	600	600	600	LINE
DE MODE	**800 × 600**			
H-sync Total	850	1056	1100	CLK
H-Active	800	800	800	CLK
H-Blanking	50	256	300	CLK
V-sync Total	628	635	650	LINE
V-Active	600	600	600	LINE
V-Blanking	28	35	50	LINE

800 × 480

SYNC MODE	800 × 480			
Parameter	Min.	Typ.	Max.	Unit
Clock Freq.	25.7	29.7	39.6	MHZ
H-sync Total	850	900	1100	CLK
H-sync Pulse Width	1	1	1	CLK
H-sync Pulse Width + Back Porch	46	46	46	CLK
H-sync Front poach	4	54	254	CLK
H-Active	800	800	800	CLK
V-sync Total	505	550	600	LINE
V-sync Pulse Width	1	1	1	LINE
V-sync Pulse Width + Back Porch	23	23	23	LINE
V-sync Front poach	2	47	97	LINE
V-Active	480	480	480	LINE
DE MODE	**800 × 480**			
H-sync Total	850	900	1100	CLK
H-Active	800	800	800	CLK
H-Blanking	50	100	300	CLK
V-sync Total	505	550	600	LINE
V-Active	480	480	480	LINE
V-Blanking	25	70	120	LINE

6. OUTPUT TIMING



	Symbol	640 × 480	800 × 600 800 × 480	Unit
DE-rising to DIO-rising	t1	TBD	TBD	CLK
DIO high duration	t2	1	1	CLK
DIO-rising to LD-rising	t3	653	813	CLK
LD high duration	t4	4	4	CLK
DIO-rising to VCLK-rising	t5	647	817	CLK
VCLK high duration	t6	318	398	CLK
DIO-rising to STV-rising	t7	9	9	CLK
STV high duration	t8	898	898	CLK
DIO-rising to POL-rising	t9	658	820	CLK
POL high duration	t10	1L	1L	CLK
DIO-rising to OEV-rising	t11	571	709	CLK
OEV high duration	t12	96	120	CLK

Absolute Maximum Ratings (Note1)

Item	Symbol	Conditions	Range	Units
Supply Voltage	VDD	-	-0.3 to + 6	V
Input Voltage	VI	TTL 5V tolerant Buffer	-0.3 and VI< +0.3	V
Output Voltage	VO	TTL Buffer	-0.3 and VI< +0.3	V
Storage temperature	Tstg	-	-45 to +125	Deg.c
Junction temperature	Tj	-	+150	Deg.c

Note1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed

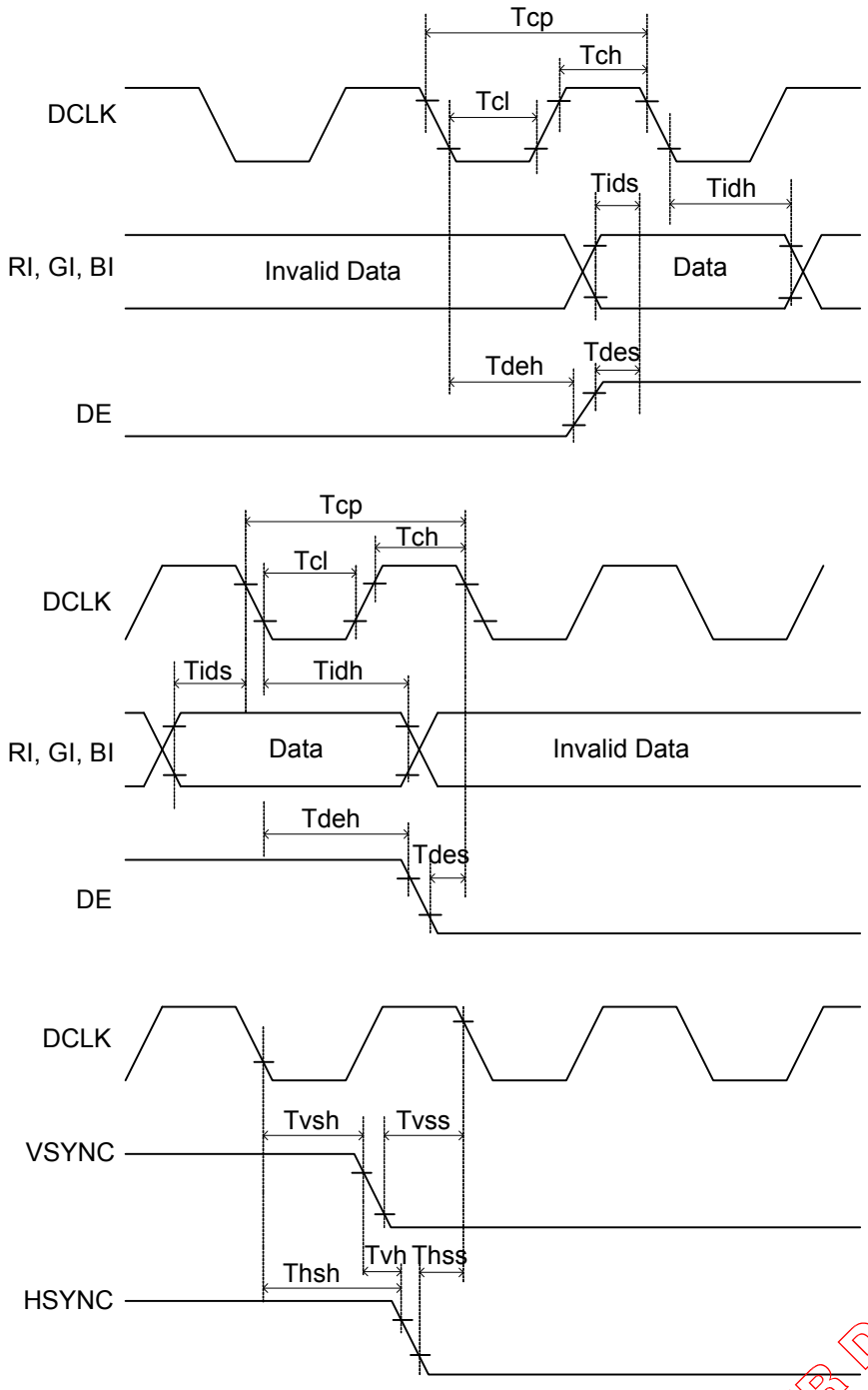
7. DC ELECTRICAL CHARACTERISTICS

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
TTL Input Characteristic						
Supply Voltage	VDD	-	2.7	-	5.5	V
Minimum High Level Input Voltage	VIH	TTL Buffer	2.0	-	-	V
Maximum Low Level Input Voltage	VIL	TTL Buffer	0	-	0.8	V
Minimum High Level Input Voltage	VIH	TTL 5V Tolerant Buffer	2.0	-	5.5	V
Maximum Low Level Input Voltage	VIL	TTL 5V Tolerant Buffer	0	-	0.8	V
Positive Trigger Voltage	VP	TTL SCHMITTER Buffer	1.4	-	2.4	V
Negative Trigger Voltage	VN	TTL SCHMITTER Buffer	0.8	-	1.6	V
Hysteresis Voltage	VH	TTL SCHMITTER Buffer	0.3		1.5	V
Output Sink/Source current	IO	VOL = 0.4V/VOH = 2.4V (Type 2 for 8Ma)	8	-	-	mA

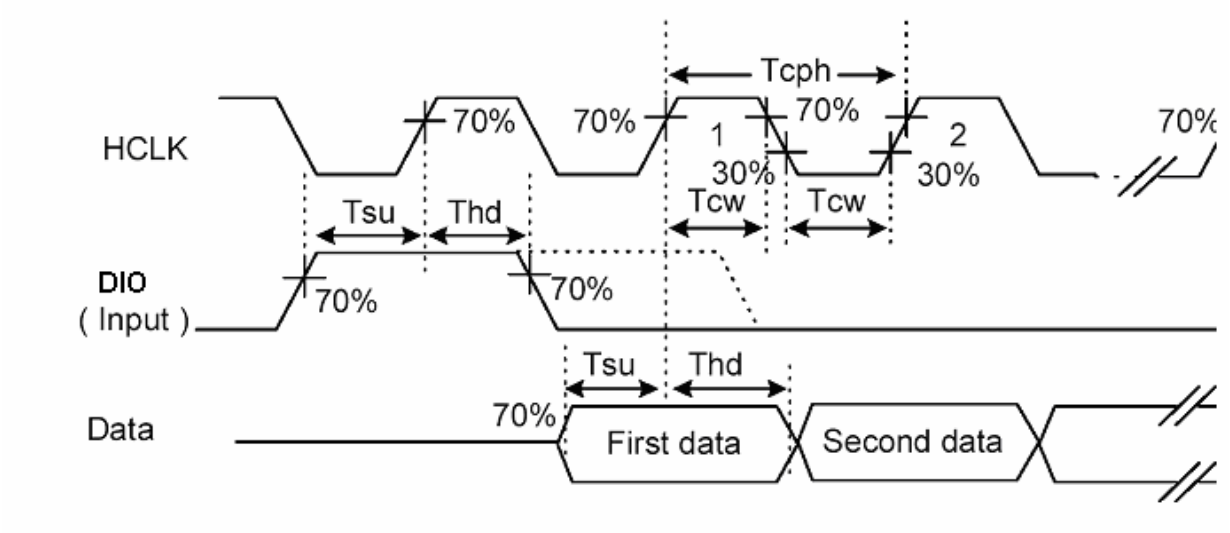
8. AC ELECTRICAL CHARACTERISTICS

Symbol	Item	Specification			Unit
		Min.	Typ.	Max.	
Fdclk	DCLK frequency	5	-	40	MHZ
Tduty	DCLK	-	-	-	-
Tcp	DCLK period	16.67	-	-	ns
Tch	DCLK High time	0.3	-	-	Tcp
Tcl	DCLK Low time	0.3	-	-	Tcp
Tids	RGB Input Data Setup time	5	-	-	ns
Tidh	RGB Input Data Hold time	10	-	-	ns
Tdes	DE Setup time	5	-	-	ns
Tdeh	DE Hold time	10	-	-	ns
Thss	HSYNC Setup time	5	-	-	ns
Thsh	HSYNC Hold time	10	-	-	ns
Tvss	VSYNC Setup time	5	-	-	ns
Tvsh	VSYNC Hold time	10	-	-	ns
Tvh	VSYNC↓ to HSYNC↓ Delay	0	-	-	ns
Tsu	Data hold time	8	-	-	ns
Thd	Data set-up time	4	-	-	ns
Tcw	HCLK pulse width	3	-	-	ns

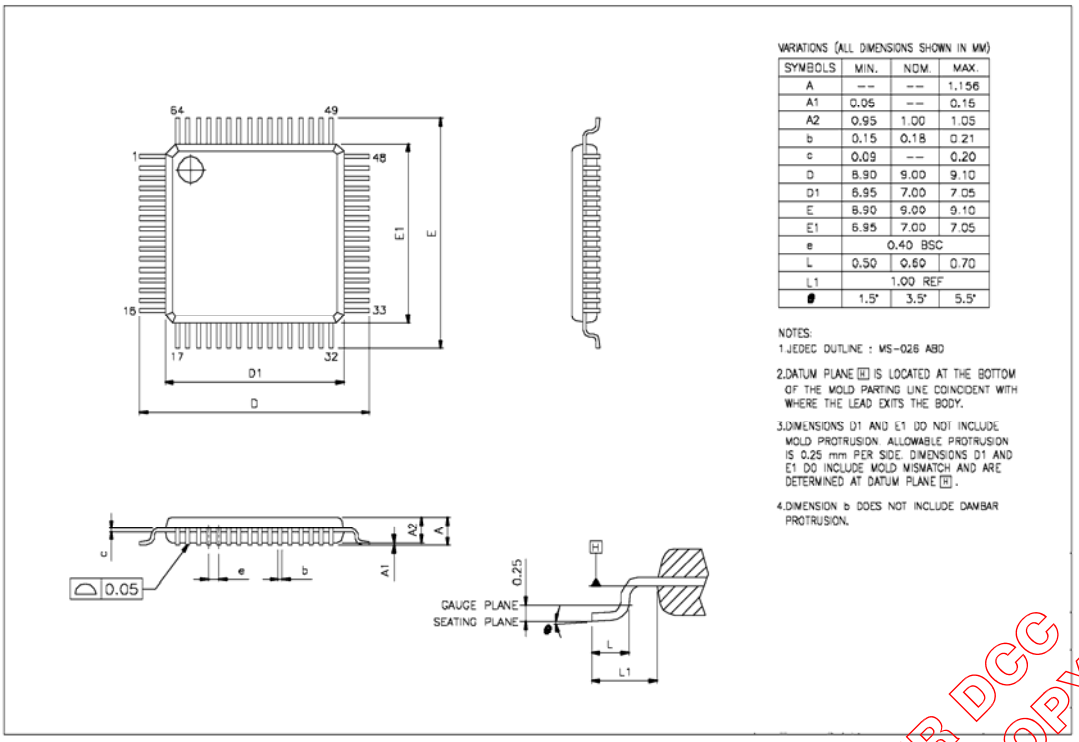
Input Signal Timing Chart



Output Signal Timing Chart



9. PACKAGE INFORMATION



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.156
A1	0.05	--	0.15
A2	0.95	1.00	1.05
b	0.15	0.18	0.21
c	0.09	--	0.20
D	8.90	9.00	9.10
D1	6.95	7.00	7.05
E	8.90	9.00	9.10
E1	6.95	7.00	7.05
e	0.40 BSC		
L	0.50	0.60	0.70
L1	1.00 REF		
θ	1.5°	3.5°	5.5°

NOTES:
1.JEDEC OUTLINE : MS-026 ABD
2.DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

10. REVISION HISTORY

0. 99

- ✧ New issue

1.0

- ✧ Page 6 / page 7 Separate 800*600/800*480 into two tables.

1.1

- ✧ Page 6 / page 7 modify the numbers of clock frequency.
- ✧ Page 9 modify the unit of Tcl
- ✧ Page 10 modify Tcp period at “DE to low” chart.