天鈺科技股份有限公司
Eureka Microelectronics,Inc.

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Eureka Microelectronics, Inc.

EK7601

DATA SHEET

240-Channel Analogue Source Driver for colour TFT LCDs

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240-Channel Analogue Source Driver for colour TFT LCDs

OVERVIEW

The EM7601 is an analogue, fully colour, source driver for TFT LCD panels designed for camera, TV etc. Analogue R, G and B signal are applied directly on the chip. For each of the 240 outputs, the voltage is sampled and buffered to the panel. With a double sample and hold circuit a new voltage can be sample whereas the previous sample voltage is applied to the panel.

According to different modes, the 3 input voltages (VA, VB, VC) can be applied on different output to support various pixel array types.

The 3 input voltages (VA, VB, VC) can be sampled simultaneously or sequentially to have a better flexibility with the input voltage. Using enable signal (STHx), several chips can be cascaded for large panel.

FEATURE

- LCD outputs: 240
- Bi-directional shift (L/$\overline{R}$)
- Simultaneous or Sequential RGB acquisition mode
- X1 or X3 clock mode
- High frequency Sampling 10MHz (x1)
- Automatic low power consumption mode after data capture (gated clock)
- RGB colour selection (automatic or manual)
- Applicable to COG / COF
- Logic power supply voltage V_{DD}: 2.7V – 5.25V
- LCD power supply voltage AV_{DD}: 4.5V – 5.5V
- Output dynamic range AV_{SS}+0.2V to AV_{DD}-0.2V
- Applicable to COG/COF

1. INTERNAL BLOCK DIAGRAM

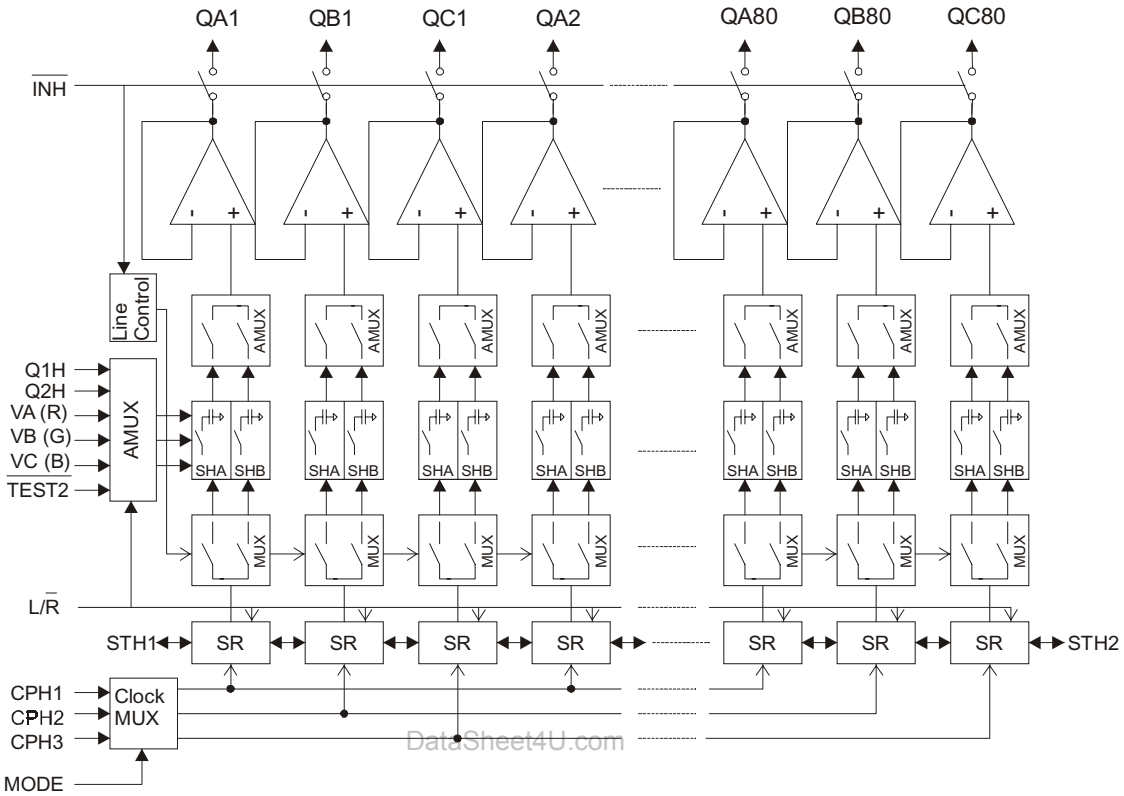


Figure 1.1: Block diagram

1. **Clock MUX**
   Selects if the sampling is simultaneous or sequential and the clocks are divided by three or not. Also gates the clock.
2. **3 x 80-bit bi-directional shift register**
   Generates enable signals for sequential sampling 80 groups of 3 input colours.
3. **Line control**
   Select sample circuit SHA or SHB and the high impedance output state
4. **SH control MUX**
   Select which sample and hold circuit samples the analogue input value.
5. **RGB MUX**
   According to the controls signals, selects which input colour goes to which group of outputs.
6. **Sample and hold Circuit (SHA, SHB)**
   Sample the input voltage when the enable signal of the shift register is generated and hold this value until it is stored on the panel.
7. **Buffers**
   Drive the sample greyscale voltage on the panel.

2. PIN CONFIGURATION (COF PACKAGE)

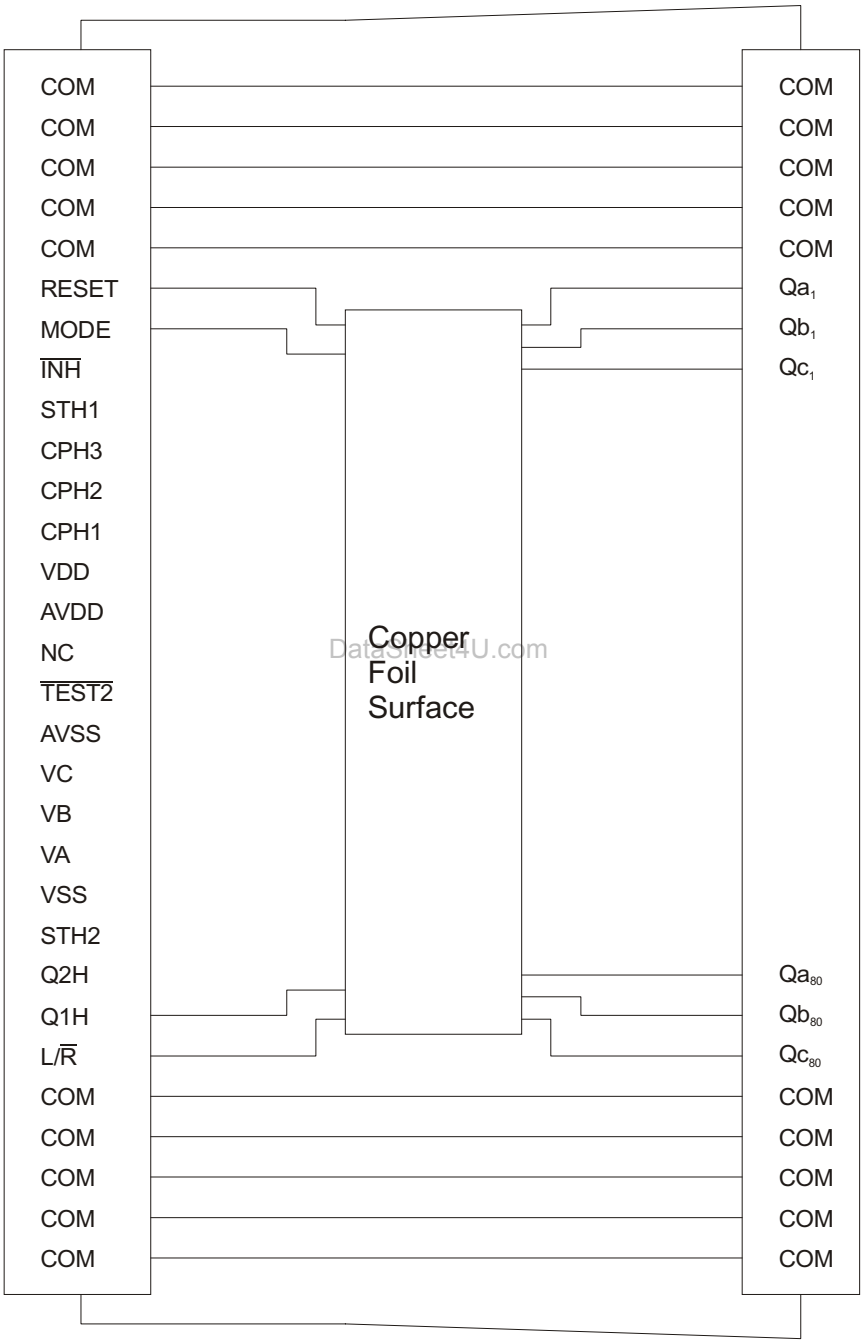


Figure 2.1: Pin Arrangement

3. PIN FUNCTION DESCRIPTION

Signal Name	Pin Type	Function
Qa1 to Qa80 Qb1 to Qb80 Qc1 to Qc80	Output	Liquid-crystal application voltages *Each QaX, QbX or QcX correspond to one of the analogue sample input signal VA, VB or VC.*
VA VB VC	Input	Video input signal *Analogue video input signal that is sampled internally and applied to the panel.*
L/$\overline{R}$	Input	Controls the display data shift direction *L/$\overline{R}$ = H : STH1 input, Qa1→Qc80, STH2 output.* *L/$\overline{R}$ = L : STH2 input, Qc80→Qa1, STH1 output.*
STH1	Bidir	Right shift start pulse *L/$\overline{R}$ = H : Becomes the start pulse input pin* *L/$\overline{R}$ = L : Becomes the start pulse output pin*
STH2	Bidir	Left shift start pulse *L/$\overline{R}$ = H : Becomes the start pulse output pin* *L/$\overline{R}$ = L : Becomes the start pulse input pin*
CPH1 CPH2 CPH3	Input (Pull-down CPH2 & CPH3 @ $\overline{TEST2}$ = L And MODE=H)	Sampling clock input *Refers to the analogue data-sampling clock. The sampling starts at the first rising edge of CPH1 when STH1 (L/$\overline{R}$=H) is activated.* *CPH1 can be internally divided (x3 mode) to generate internal clock signal CPH1'.* *The sampling can be simultaneous or sequential.* *In simultaneous mode, the sampling is made during CPH1 (CPH1') period for all output.* *In sequential mode, the sampling is made according the table below:* *CPH1 (CPH1') control the sampling for Qa1→Qa80* *CPH2 (CPH2') control the sampling for Qb1→Qb80* *CPH3 (CPH3)' control the sampling for Qc1→Qc80* *When clock mode x1 and sequential is selected, the three inputs CPH1, CPH2 and CPH3 must have an input clock signal applied. Otherwise only CPH1 must have input clock applied.* *The clock selection table was described on the page 8.*
$\overline{INH}$	Input	Load line *The sampled voltages are connecting to the panel at the rising edge of $\overline{INH}$. The outputs of SHA(B) that was in sample mode are applied to the panel, whereas the SHB(A) becomes ready to sample new values.* *During $\overline{INH}$ = L, output level is HiZ state and this signal initialise the internal circuits.*

$\overline{TEST2}$	Input (Pull-up)	Input signal colour rotation mode selector *$\overline{TEST2}$ = L: No data rotation mode.* *Input voltage of each output QaX, QbX and QcX are selected from VA, VB and VC according to the control signal Q1H and Q2H.* *Simultaneous or sequential clock mode is selected by MODE.* *$\overline{TEST2}$= H or open: Automatic rotation mode.* *Input voltage of each output QaX, QbX and QcX are selected automatically from VA, VB and VC according to the filter arrays, selected by the control signal Q1H and Q2H.* *Simultaneous or sequential clock mode is selected by Q1H, Q2H.*
MODE	Input (Pull-down @ $\overline{TEST2}$ = L)	Sampling mode selection *MODE = L or open: Sequentially sampling* *MODE = H: Simultaneous sampling* *This signal is only usable when TEST2= L.*
Q1H Q2H	Input (Pull-down @ $\overline{TEST2}$ = L)	Colour selection input *When $\overline{TEST2}$ = L: Q1H and Q2H select which input voltage (VA, VB, VC) correspond to QaX, QbX, QcX outputs.* *When $\overline{TEST2}$ =H: Q1H and Q2H select the filters array colours sequence. Q1H and Q2H select also simultaneous/sequential mode according to the equation below.* *Q1H = Q2H = 0: Simultaneous sampling* *Q1H =1 OR Q2H = 1: Sequential sampling* *The colour selection table and filter array are describe on page 12.*
RESET	Input (Pull-down @ $\overline{TEST2}$ = L)	Automatic colour selection Initialisation *Reset the system of the automatic rotation mode. To initialise the module a pulse on INH must be applied after reset.* *This function is only usable when $\overline{TEST2}$=H. When not used should be L or open.*
V_{DD}	Power	Logic part power supply
V_{SS}	Power	Logic part ground
AV_{DD}	Power	Analogue part power supply
AV_{SS}	Power	Analogue part ground

4. OPERATION TIMING

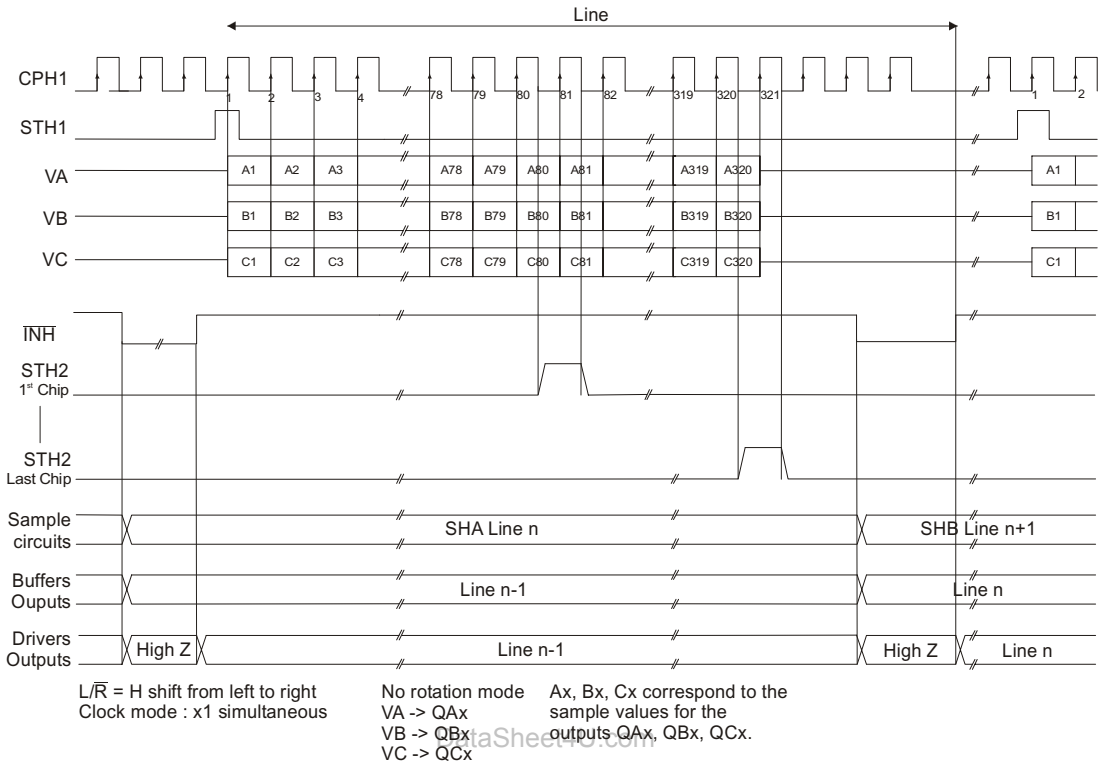


Figure 4.1: Operation timing diagram

The start condition is initiated by applying a start pulse to the enable input pin (STH1 when L/$\overline{R}$=VDD) at the beginning of each line on the first chip. During the next 80 CPH1 rising edges, this source driver sample 80 times 3 display input voltage (3 RGB dot x 80 pixels). After sampling the 80th group of input voltages, it activates the enable output signal (STH2 when L/$\overline{R}$=VDD) to enable the following chip.
As soon as the loading of the input voltage is achieved for a complete line, the controller activates the $\overline{INH}$ signal to force the 240 output buffers in a high impedance state. Then the outputs of SHA(B) that were in sample mode are applied to the output buffers , whereas the SHB(A) becomes ready to sample new values. Finally, at the rising edge of $\overline{INH}$, the 240 output buffers drive the sample voltages to the panel.

5. SAMPLING MODES

Simultaneous/Sequential and x1/x3 sampling modes provide 4 different ways to sample input voltages.
Simultaneous/Sequential selection mode is described on the table below.

When $\overline{TEST2}$ =L	When $\overline{TEST2}$ =H	Sampling Mode
Mode=H	Q1H=Q2H=L	Simultaneous
Mode=L	Q1H=H OR Q2H =H	Sequential

Table 5.1: Simultaneous Sequential selection table

Sampling Mode	CPH1	CPH2	CPH3	Clock division
Simultaneous	Clock IN	L	L	x1
Sequential	Clock IN	Clock IN	Clock IN	
Simultaneous	Clock IN	L	H	x3
Sequential	Clock IN	L	H	

Table 5.2: x1 x3 clock selection table

All diagram below describe the 4 clock modes, voltage correspondence are: VA -> QAX, VB -> QBX, VC -> QCX.
Ax, Bx, Cx correspond to the sample values for the outputs QAx, QBx, QCx.

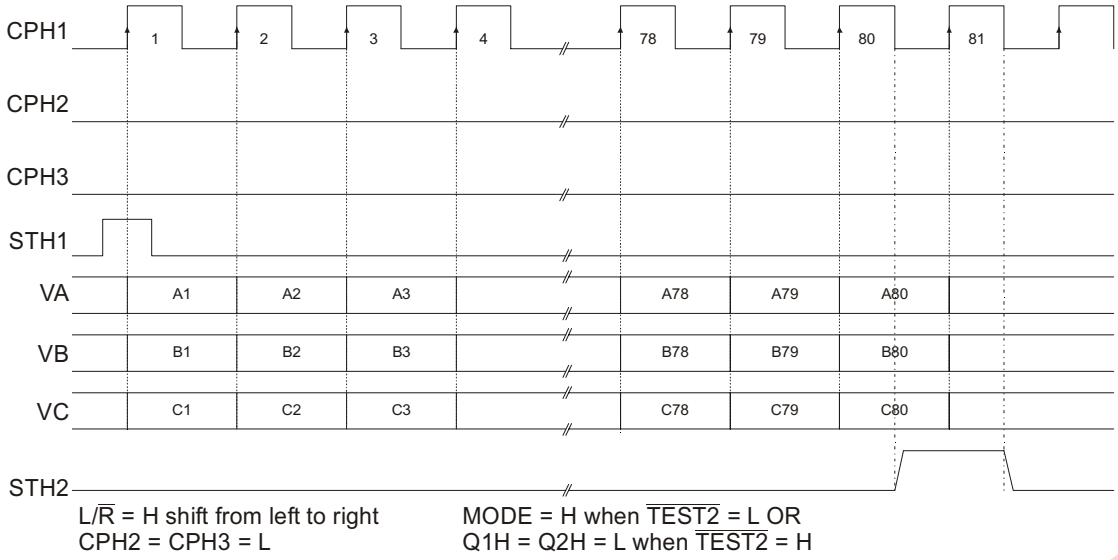


Figure 5.1: x1 simultaneous sampling mode

Each input is sampled simultaneously synchronised with CPH1 rising edge.
Output enable signal is generated at the falling edge of the 80th period of CPH1 since the start pulse.

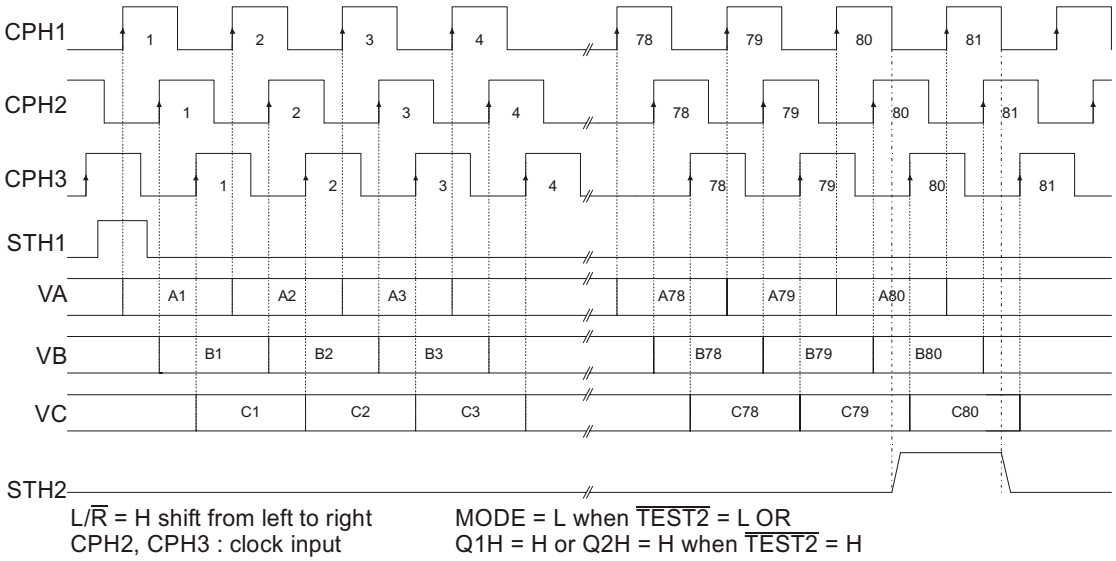


Figure 5.2: x1 sequential sampling mode

Each input is sampled sequentially synchronised with the associated rising edge of the corresponding clock. CPH1 controls the sample for QAx outputs, CPH2 controls the sample for QBx outputs and CPH3 controls the sample for QCx outputs.
Output enable signal is generated at the falling edge of the 80th period of CPH1 since the start pulse.

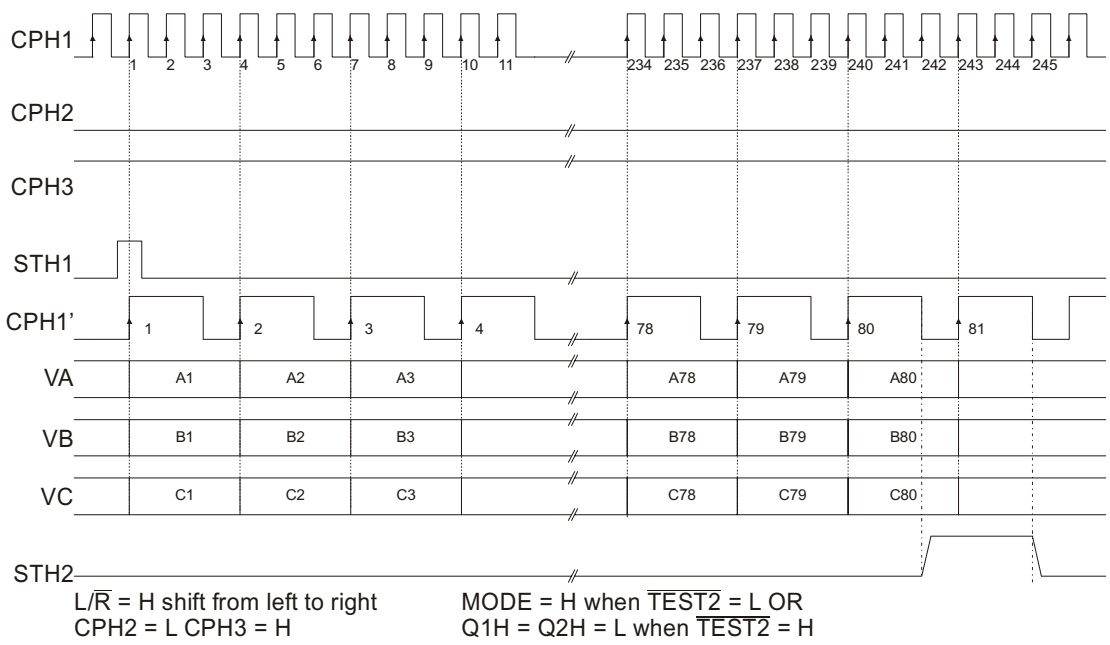


Figure 5.3: x3 simultaneous sampling mode

Each input is sampled simultaneously synchronised with CPH1' rising edge. CPH1' is generated from CPH1 (Frequency divided by 3).
Output enable signal is generated at the falling edge of the 80th period of CPH1' since the start pulse.

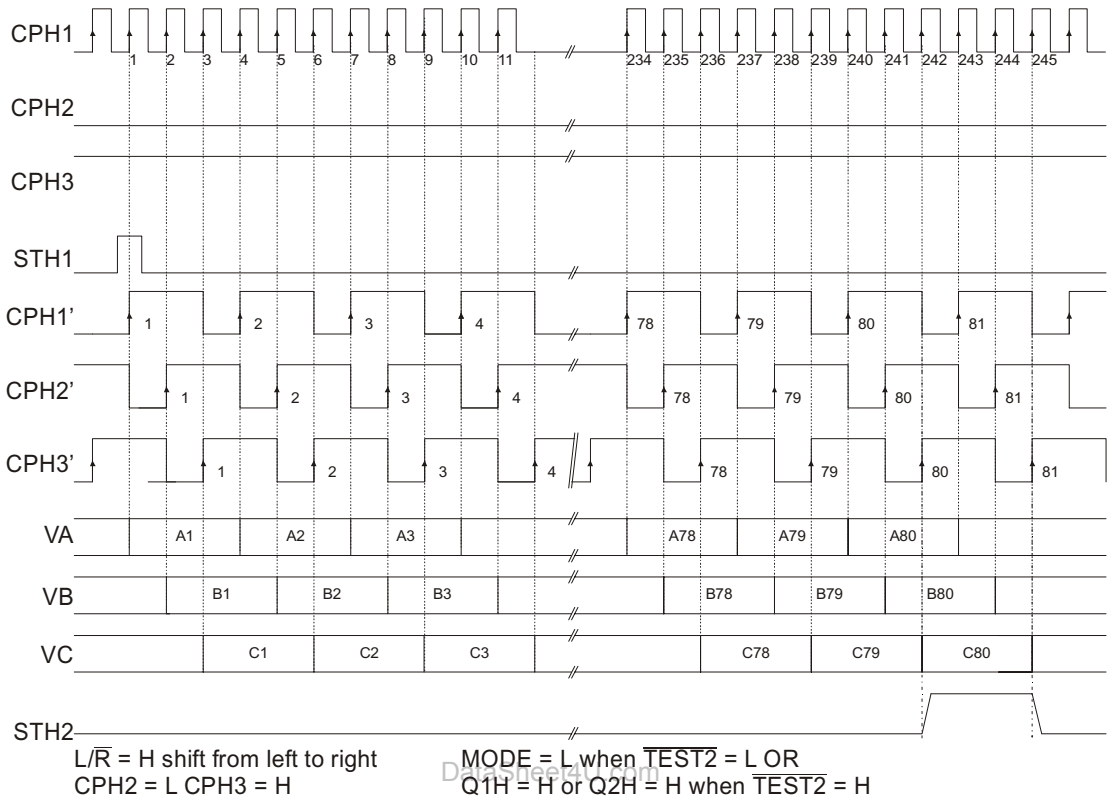


Figure 5.4: x3 sequential sampling mode

Each input is sampled sequentially synchronised with the associated rising edge of the corresponding clock. CPH1' controls the sample for QAx outputs, CPH2' controls the sample for QBx outputs and CPH3' controls the sample for QCx outputs.
CPH1', CPH2' and CPH3' are generated from CPH1 (Frequency divided by 3). The three clocks have one CPH1 period phase shift between them.
Output enable signal is generated at the falling edge of the 80th period of CPH1' since the start pulse.

6. COLOUR MODE SELECTION

According to the signal description table, the colour mode selection is separated in two modes. No rotation mode and automatics rotation mode.

NO ROTATION MODE

This mode is selected by $\overline{TEST2}$ = L. When no rotation mode is selected, Q1H and Q2H control the colour selection in order to the table below.

Q1H	Q2H	QA	QB	QC
L	L	VA	VB	VC
L	H	VC	VA	VB
H	X	VB	VC	VA

Table 6.1: No rotation mode colour selection table

The sample circuit SHA(B) get the value according to the table above.
For example, when Q1H = Q2H = L, the sample circuit SHA(B) for the outputs Qax sample VA and the next $\overline{INH}$ pulse this sample voltage is put to the panel.

AUTOMATIC ROTATION MODE

This mode is selected by $\overline{TEST2}$ = H. It allows the chip to select automatically the colour in function of the panel colour filter and the chips location on the panel (single bank or dual bank). Single bank mean that all the source drivers are on one side of the panel. Dual bank means that one group of source drivers is in the top of the panel and one at the bottom of the panel and they drive columns alternatively.

Q1H	Q2H	Colour array	Chip location
L	L	Vertical Stripe	Single bank
L	H	Delta	Single bank
H	X	Delta	Dual bank

Table 6.2: Automatic rotation mode panel selection table

In this mode, the colour selection has a cycle of two lines. A pulse on RESET and after an activation of $\overline{INH}$ initialises this sequence (figure below).

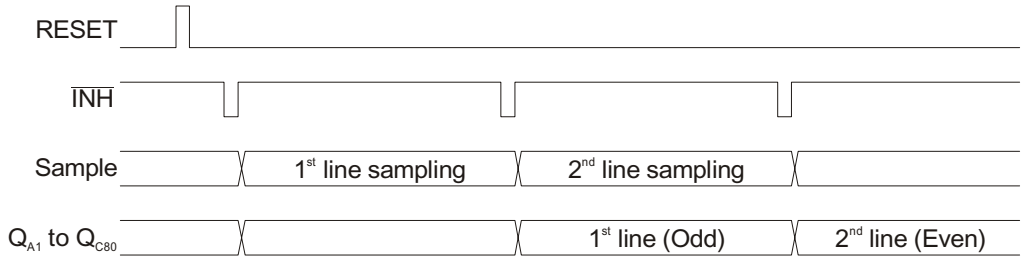


Figure 6.1: Automatic rotation mode initialisation sequence

In automatic rotation mode, the colour is selected automatically for Odd and Even line.

Vertical stripe array

This mode is selected by Q1H = Q2H = L and $\overline{\text{TEST2}}$=H.

The characteristics of this panel configuration are:

- Each column is associated with one colour.
- One bank of source driver.

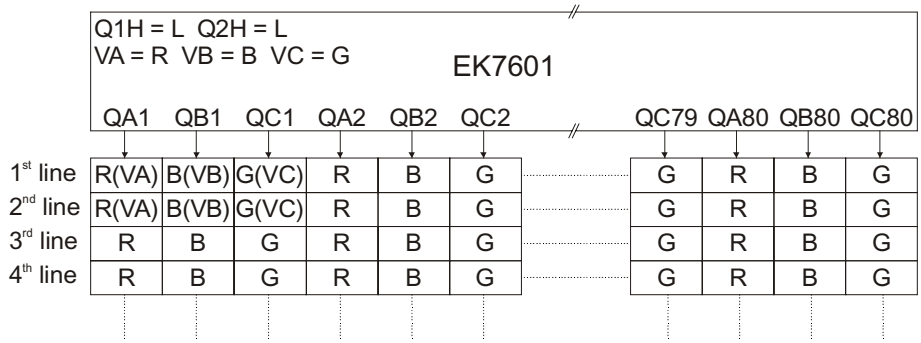


Figure 6.2: Vertical stripe array panel configuration

The figure shows, for this mode, that there is only one case of colour:

Line	QA	QB	QC
Odd	VA	VB	VC
Even	VA	VB	VC

Table 6.3: Vertical stripe array colour selection table

Single bank delta array

This mode is selected by Q1H = L, Q2H = H and $\overline{TEST2}$ = H.

The characteristics of this panel configuration are:

- Each column is share between two colours.
- One bank of source driver.

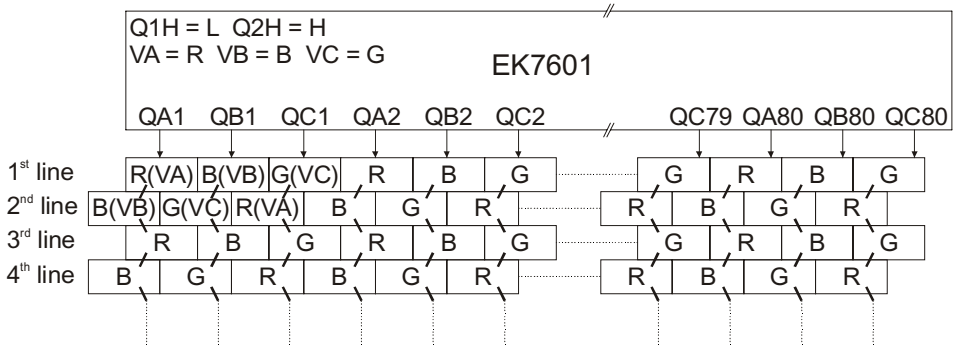


Figure 6.3: Single bank delta array panel configuration

The colours are switched between Odd and Even line:

Line	QA	QB	QC
Odd	VA	VB	VC
Even	VB	VC	VA

Table 6.4: Single bank delta array colour selection table

Dual bank delta array

This mode is selected by Q1H = H, Q2H = H and $\overline{TEST2}$ = H.

The characteristics of this panel configuration are:

- Each column is share between two colours.
- Two bank of source driver (top and bottom of the panel).

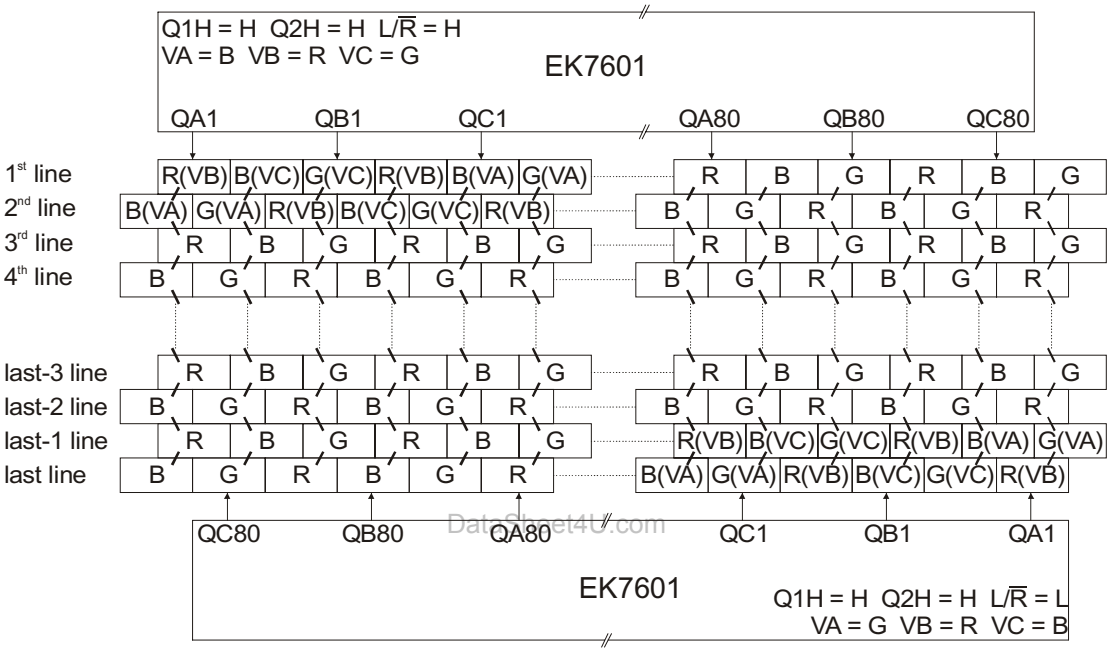


Figure 6.4: **Dual bank delta array panel configuration**

The colours are switched between Odd and Even line and depend also on L/$\overline{R}$:

L/$\overline{R}$	Line	QA	QB	QC
H	Odd	VB	VC	VA
	Even	VA	VB	VC
L	Odd	VA	VB	VC
	Even	VB	VC	VA

Table 6.5: Dual bank delta array colour selection table

COLOURS SELECTION RESUMING TABLE

The table below resume 3 different colour cases:

Case	QA	QB	QC
1	VA	VB	VC
2	VC	VA	VB
3	VB	VC	VA

Table 6.6: RGB Colour selection case

The table below resume all colour selection modes:

Q1H	Q2H	LR	When $\overline{TEST2}$ =L	When $\overline{TEST2}$ =H	
				Odd line	Even line
L	L	X	1	1	1
L	H	X	2	1	3
H	H	L	3	1	3
H	H	H	3	3	1

Table 6.7: Colours selection resuming table

The numbers represent the different colour cases are listed on Table 6.6.

7. RELATIONSHIP BETWEEN $\overline{INH}$ AND OUTPUT WAVEFORM

At $\overline{INH}$ rising edge, the sample voltages are output on the panel. As long as $\overline{INH}$ is active, the 240 output buffers are forced in a high impedance state.

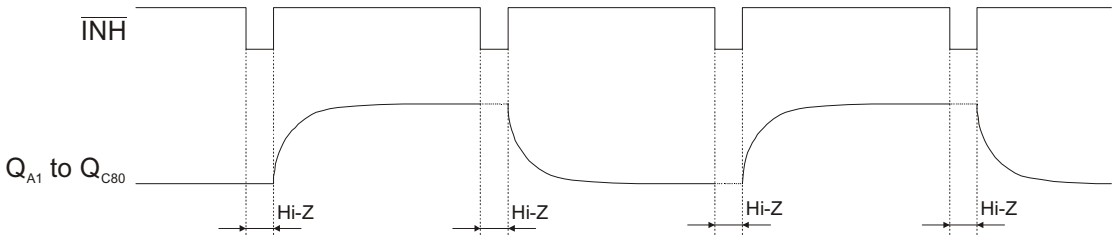


Figure 7.1: $\overline{INH}$ timing diagram

8. ELECTRICAL SPECIFICATION

Absolute Maximum Rating (V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD}	-0.5 to +7.0V	V
Analogue Part Supply Voltage	AV_{DD}	-0.5 to +7.0V	V
Logic Part Input Voltage	V_{I1}	-0.5 to VDD + 0.5	V
Video Input Voltage	V_{I2}	-0.5 to AVDD + 0.5	V
Logic Part Output Voltage	V_{O1}	-0.5 to VDD + 0.5	V
Driver Part Output Voltage	V_{O2}	-0.5 to AVDD + 0.5	V
Storage Temperature	T_{STG}	-55 to +125	°C

Caution: If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum rating, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum rating.

Recommended Operating Range (V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Logic Part Supply Voltage	V_{DD}		2.7		5.25	V
Analogue Part Supply Voltage	AV_{DD}		4.5		5.5	V
Video Input Voltage	V_{VIDEO}		AV_{SS} + 0.2		AV_{DD} - 0.2	V
Operating Ambient Temperature	T_A		-30		75	°C
Maximum Clock Frequency	F_{CPH}	X1 Mode			10	MHz
		X3 Mode			25	MHz
$\overline{INH}$ period	T_{INH}			64	200	µs

DC Characteristics

(T_A= -30 to +75°C, V_{DD}= 2.7V to 5.25V, AV_{DD}= 4.5V to 5.5V, V_{SS}=AV_{SS}=0V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Logic High-level Input Voltage	V_{DIH}		0.7*V_{DD}		V_{DD}	V
Logic Low-level Input Voltage	V_{DIL}		0.0		0.3*V_{DD}	V
Logic Input Leakage Current	I_{LIL}				±1.0	μA
Video Input Leakage Current	I_{VIL}				±1.0	μA
Logic High-level Output Voltage	V_{OH}	STH1(STH2), I_{OH}=0mA	V_{DD} - 0.1			V
Logic Low-level Output Voltage	V_{OL}	STH1(STH2), I_{OL}=0mA			0.1	V
Output Voltage Range	V_0		0.2		AV_{DD} - 0.2	V
Output Voltage Deviation	ΔV_0	Note 1			±20	mV
Logic Part Dynamic Current Consumption	I_{DD}	Note 2		TBD	TBD	
Driver Part Dynamic Current Consumption	I_{ADD}	Note 3		0.8	1.2	mA
Logic Input Capacitance	C_{L1}	STH1 (STH2) excluded, T_A=+25°C		5	10	pF
	C_{L2}	STH1 (STH2), T_A=+25°C		8	10	pF
Logic Input Capacitance	C_{L2}			TBD	TBD	pF
Wiring Resistance AV_{DD}	R_{AVDD}	Note 4		6		Ω
Wiring Resistance AV_{SS}	R_{AVSS}	Note 4		5		Ω
Wiring Resistance V_{DD}	R_{VDD}	Note 4		20		Ω
Wiring Resistance V_{DD}	R_{VSS}	Note 4		15		Ω

Note 1: Deviation between input voltage and output value. Voltage on the output pin 30us after the rinsing edge of $\overline{INH}$. V_{VIDEO}= 0.2V to AV_{DD}-0.2V.

Note 2: F_{CPH}=10MHz, X1 Simultaneous Clock Mode, T_{INH}=63μs, T_{IWL} = 5us, No load.

Note 3: Video input = AV_{DD}/2, No Load.

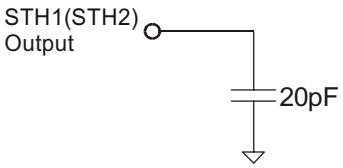
Note 4: Power and control signal are connected between each edge of the chips.

AC Characteristics

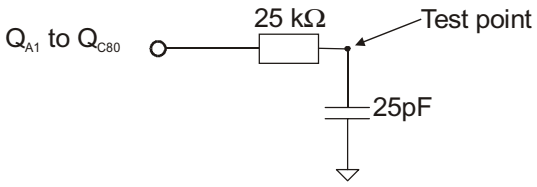
(T_A= -30 to +75°C, V_{DD}= 2.7V to 5.25V, V_{SS}=AV_{SS}=0V, T_R = T_F = 5.0ns)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Period	T_{CP}	x1 Mode	100			ns
		x3 Mode	40			ns
Clock high-level width	T_{CWH}	x1 Mode	40			ns
		x3 Mode	15			ns
Clock low-level width	T_{CWL}	x1 Mode	40			ns
		x3 Mode	15			ns
Delay time Between Clocks	T_{C12}, T_{C23}	x1 Sequential Mode	15		1/2*T_{CP}	ns
STH Setup Time	T_{SS}		10			ns
STH Hold Time	T_{SH}		10			ns
RESET Pulse Width	T_{WR}		100			ns
RESET-$\overline{INH}$ Timing	$T_{RST-INH}$		100			ns
$\overline{INH}$ high-level width	T_{IWH}		30			µs
$\overline{INH}$ low-level width	T_{IWL}		100			ns
$\overline{INH}$-STH Timing	$T_{INH-STH}$		TDB			ns
STH Pulse Delay Time	T_{SD}	C_L =20pF			20	ns
Driver Output Delay Time	T_{DD}	C_L =25pF, R_L=25kΩ		12	20	µs

Load condition: Start pulse delay Time T_{SD} on STH1 (STH2) output pin:



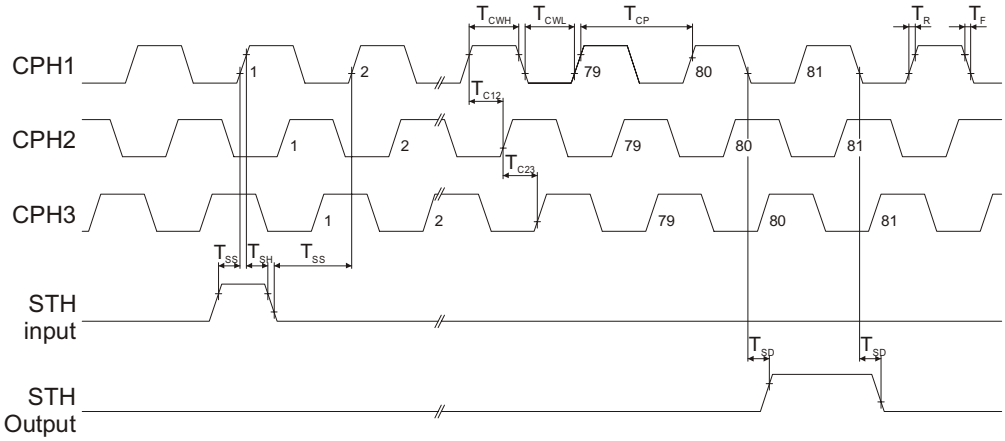
Load condition: Driver Output Delay Time T_{DD} on output buffers:



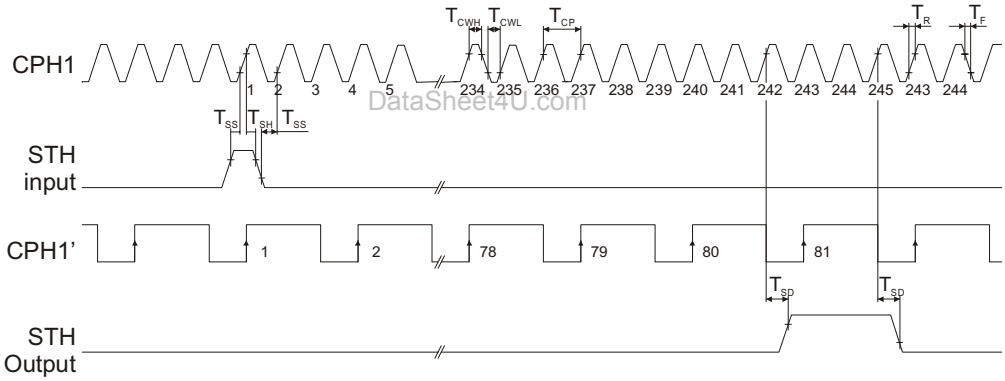
9. AC CHARATERISTICS WAVEFORM

Unless otherwise specified, the input level is defined to V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}

x1 Mode



x3 Mode



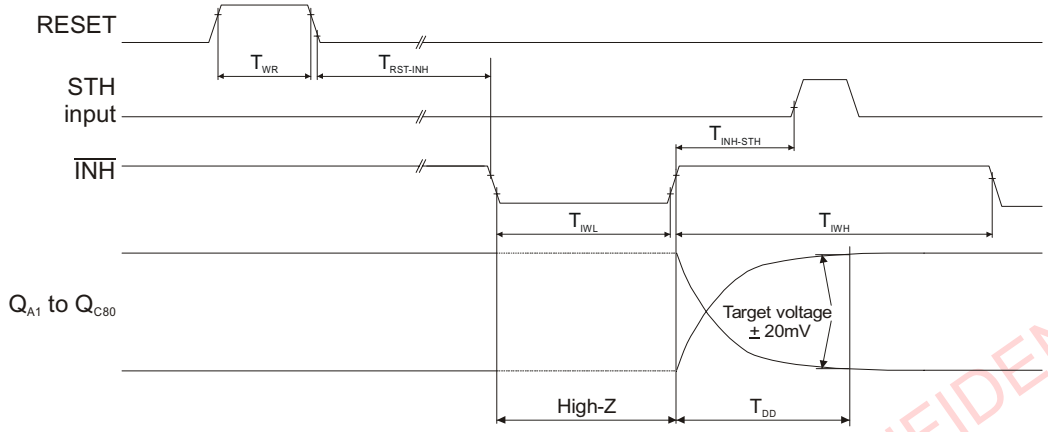


Table 9.1: AC characteristics waveform

10. RECOMMANDED SOLDERING CONDITIONS

The following conditions must be met for soldering conditions of the EK7601.
Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

EK7601: COF (TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C: heating for 2 to 3 Seconds: pressure 100g(per solder)
	ACF (Anisotropic Conductive Film)	Temporary bonding 70 to 100°C: pressure 3 to 8 kg/cm^2: time 3 to 5 seconds. Real bonding 165 to 180°C: pressure 25 to 45 Kg/cm^2: time 30 to 40 seconds.

11. LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Eureka customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Eureka for any damages resulting from such improper use or sale.