Data Sheet | July 1998, Rev C | FN7158

DC Restored Video Amplifier

The EL4089 is an 8-pin complete DC-restored monolithic video amplifier sub-system. It contains a high quality video amplifier and a nulling, sample-and-hold amplifier specifically designed to stabilize video performance.

When the HOLD logic input is set to a TTL/CMOS logic 0, the sample - and - hold amplifier can be used to null the DC offset of the video amplifier.

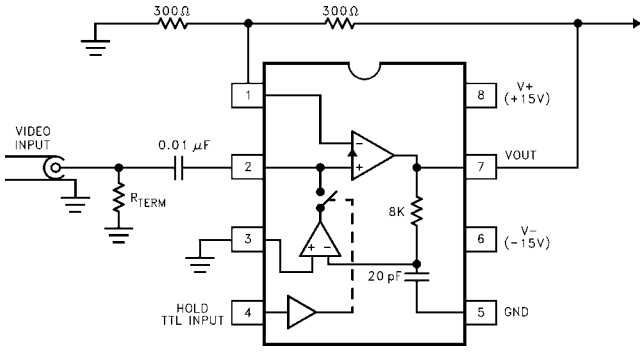
When the HOLD input goes to a TTL/CMOS logic l, the correcting voltage is stored on the video amplifier's input coupling capacitor. The correction voltage can be further corrected as need be, on each video line.

The video amplifier is optimized for video performance and low power. Its current feedback design allows the user to maintain essentially the same bandwidth over a gain range of nearly 10:1. The amplifier drives back-terminated 75Ω lines.

The EL4089 is fabricated in Elantec's proprietary Complementary Bipolar process which produces NPN and PNP transistors with equivalent AC and DC performance. The EL4089 is specified for operation over -40°C to +85°C temperature range.

Pinout

EL4089
(8-PIN PDIP, SO)
TOP VIEW



DC Restoring Amplifier with a gain of 2, restoring to ground

Features

- Complete video level restoration system
- 0.02% differential gain and 0.05° differential phase accuracy at NTSC
- 60MHz bandwidth
- 0.1dB flatness to 10MHz
- V_S = ±5V to ±15V
- TTL/CMOS hold signal

Applications

- Input amplifier in video equipment
- Restoration amplifier in video mixers

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
EL4089CN	-40°C to +85°C	8-Pin PDIP	MDP0031
EL4089CS	-40°C to +85°C	8-Pin SO	MDP0027

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V- 33V
Voltage between V_{IN}+, S/H_{IN}+,and GND pins . . (V+) +0.5V to (V-) -0.5V
V_{OUT} Current. 60mA
Current into V_{IN}- and HOLD Pins 5mA

Internal Power Dissipation . . . . . See Curves
Operating Ambient Temperature Range . . . . . .-40°C to +85°C
Operating Junction Temperature Plastic DIP or SOL. . . . . 150°C
Storage Temperature Range . . . . . .-65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Open-Loop DC Electrical Specifications

Provisional Supplies at ±15V, Load = 1kΩ; T_A = +25°C

PARAMETER	DESCRIPTION	TEMP	MIN	TYP	MAX	UNITS
AMPLIFIER SECTION (HOLD = 5V)						
V_{OS}	Input Offset Voltage	+25°C		12	25	mV
Ib+	IN+ Input Bias Current	+25°C		1	5	µA
Ib-	IN- Input Bias Current	+25°C		18	150	µA
R_{OL}	Transimpedance (Note 1)	+25°C	180	800		kΩ
R_{IN}-	IN- Resistance	+25°C		20		Ω
CMRR	Common Mode Rejection Ratio (Note 2)	+25°C	44	60		dB
V_O	Output Voltage Swing	+25°C	±12	±13		V
I_{SC}	Short Circuit Current (IN+ Only Driven to 0.5V)	+25°C	45	100		mA
RESTORE SECTION						
V_{OS}, Comp	Composite Input Offset Voltage (Note 3)	+25°C		3	7	mV
Ib+, r	Restore In+ Input Bias Current	+25°C		3	12	µA
I_{OUT}	Restoring Current Available	+25°C	180	300		µA
CMRR	Common Mode Rejection Ratio (Note 2)	+25°C	60	70		dB
PSRR	Power Supply Rejection Ratio (Note 4)	+25°C	60	90		dB
$V_{THRESHOLD}$	HOLD Logic Threshold	+25°C	0.8		2.0	V
I_{IH}, Hold	HOLD Input Current @ Logic High	+25°C		1	5	µA
I_{IL}, Hold	HOLD Input Current @ Logic Low	+25°C		5	15	µA
SUPPLY CURRENT						
Isy, Hold	Supply Current (HOLD = 5V)	+25°C	4.8	6.0	9.0	mA
Isy, Sampling	Supply Current (HOLD = 0V)	+25°C	5.0	6.5	11.0	mA

NOTES:

1. For current feedback amplifiers, $A_{VOL} = R_{OL}/R_{IN}$-.
2. V_{CM} = ±10V for V_S = ±15V.
3. Measured from S/H Input to amplifier output, while restoring.
4. V_{OS} is measured at V_S = ±4.5V and V_S = ±16V, both supplies are changed simultaneously.

Closed-Loop AC Electrical Specifications

Provisional Supplies at ±15V, Load = 150Ω and 15pF. R_F and R_G = 300Ω; A_V = 2, T_A = 25°C. (Note 1)

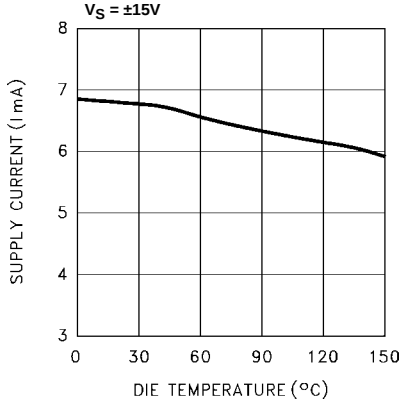
PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNITS
AMPLIFIER SECTION						
SR	Slew Rate (Note 2)			500		V/µs
SR	Slew Rate with ±5V Supplies (Note 2)			275		V/µs
BW	Bandwidth ±5V Supplies	-3dB		60		MHz
		-3dB		55		MHz
BW	Bandwidth ±5V Supplies	±0.1dB		25		MHz
		±0.1dB		23		MHz
dG	Differential Gain at 3.58MHz (Note 3)	V_S = ±15V		0.02		%
		V_S = ±5V		0.03		%
dPh	Differential Phase at 3.58MHz (Note 3)	V_S = ±15V		0.05		°
		V_S = ±5V		0.06		°
RESTORE SECTION						
SR	Restore Amplifier Slew Rate (Test Circuit) 20%--80%			25		V/µs
T_{HE}	Time to Enable Hold			25		ns
T_{HD}	Time to Disable Hold			40		ns

NOTES:

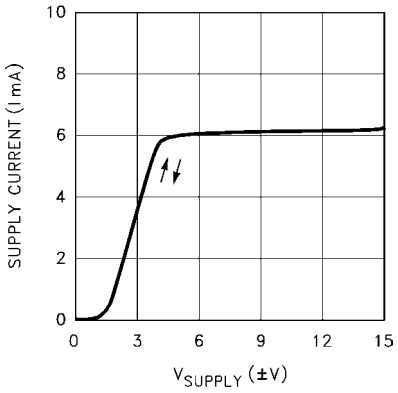
1. Test fixture was designed to minimize capacitance at the IN- input. A “good” fixture should have less than 2pF of stray capacitance to ground at this very sensitive pin. See application notes for further details.
2. SR measured at 20% to 80% of a $4V_{PK-PK}$ square wave.
3. DC offset from -0.714V through +0.714V, ac amplitude is $286mV_{P-P}$, equivalent to 40 IRE.

Typical Performance Curves

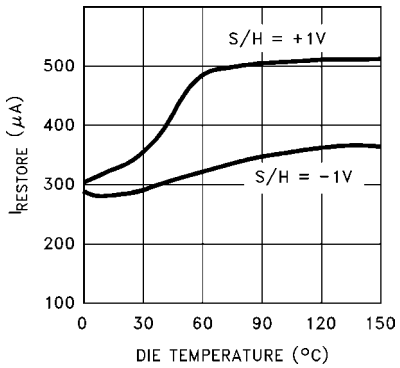
Supply Current vs Temperature
V_S = ±15V



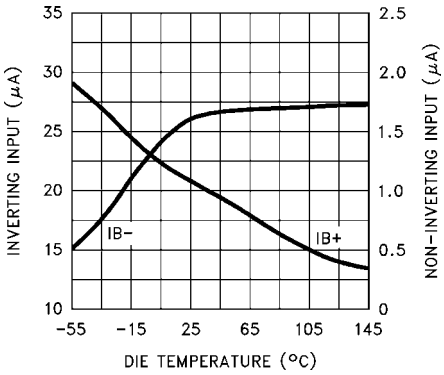
Supply Current vs Supply Voltage



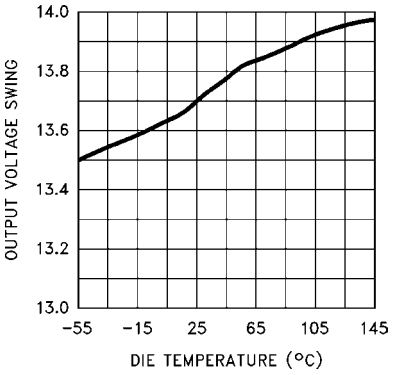
Restoring Current vs Temperature



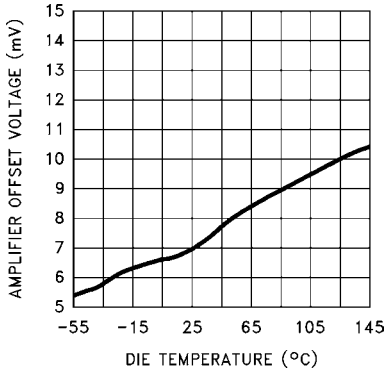
Amplifier Input Current vs Die Temperature



Amplifier Output Voltage vs Die Temperature;
V_S = ±15V

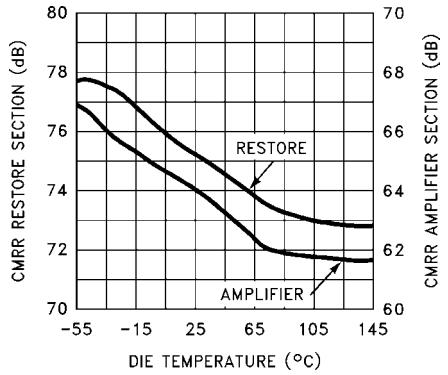


Amplifier Offset Voltage vs Die Temperature

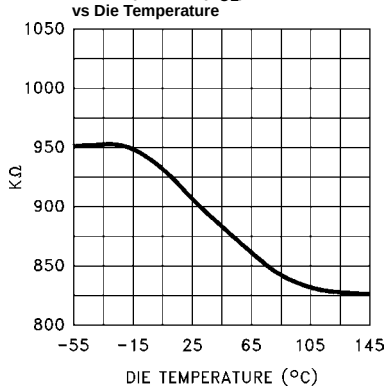


Typical Performance Curves (Continued)

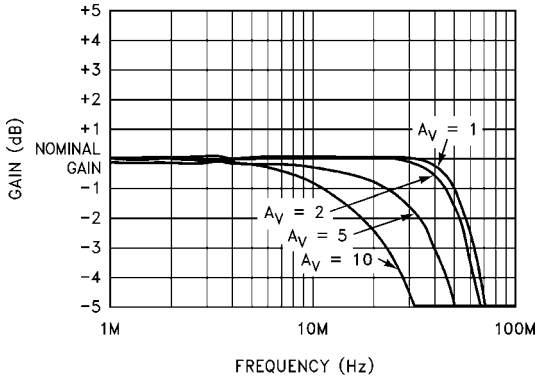
CMRR for Amplifier and Restore Section vs Die Temperature



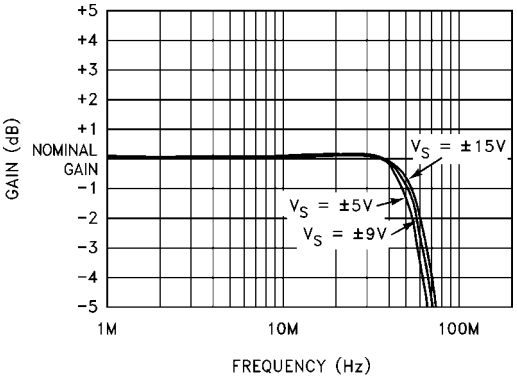
Transimpedance (R_{OL}) vs Die Temperature



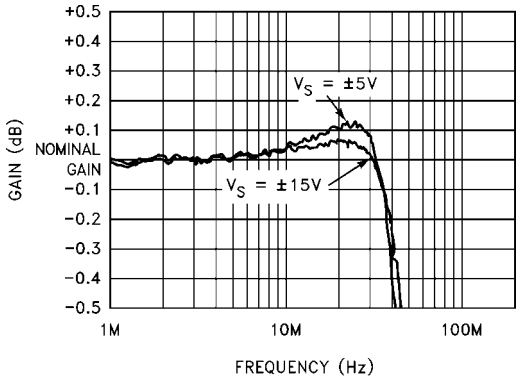
Relative Frequency Response for Various Gains, R_F = 300Ω



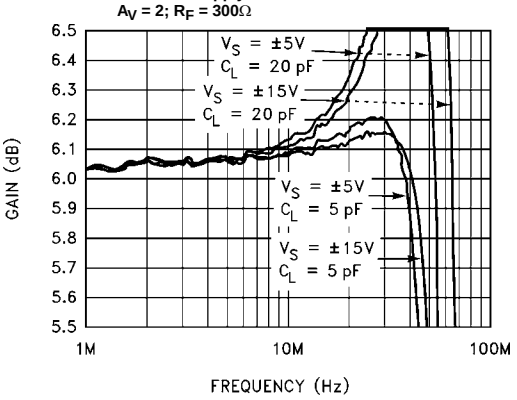
Frequency Response vs Supply A_V = 2; R_F = 300Ω



Frequency Response Flatness vs Supply A_V = 2; R_F = 300Ω

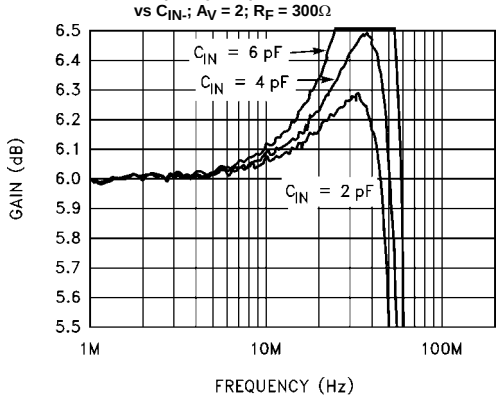


Frequency Response Flatness for Various Load and Supply Conditions A_V = 2; R_F = 300Ω

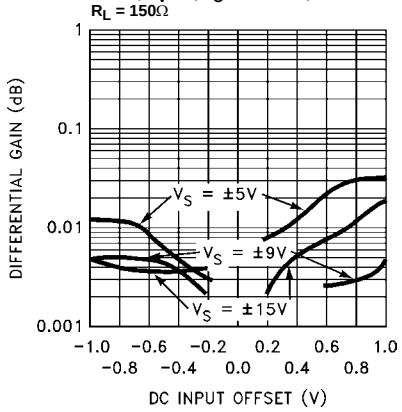


Typical Performance Curves (Continued)

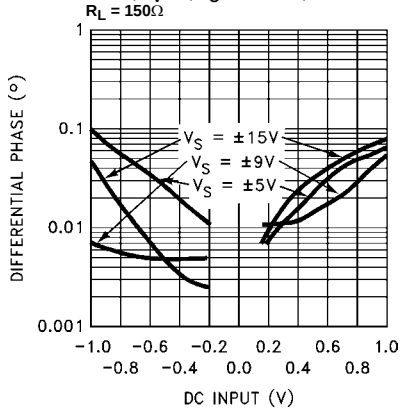
Frequency Response Flatness vs C_{IN}.; A_V = 2; R_F = 300Ω



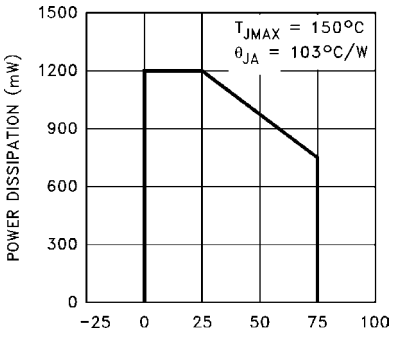
Differential Gain vs DC Input Offset; A_V = 2, F_O = 3.58MHz, R_L = 150Ω



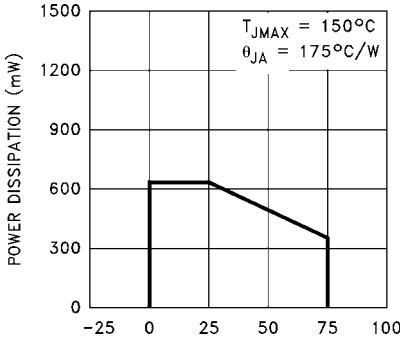
Differential Phase vs DC Input Offset; A_V = 2; F_O = 3.58MHz; R_L = 150Ω



8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



8-Lead SO Maximum Power Dissipation vs Ambient Temperature



Typical Application

The EL4089 can be used to DC-restore a video waveform (see Figure 1). The circuit forces the cable driving video amplifier's output to ground when the HOLD pin is at a logic low.

The "correction voltage" is stored on capacitor CX1, an external ceramic capacitor. The capacitor value is chosen from the system requirements. The typical input bias current to the video amplifier is 1µA, so for a 62µs hold time, and a 0.01µF capacitor, the output voltage drift is 6.2mV in one line.

The S/H amplifier can provide a typical current of 300µA to charge capacitor CX1, so with a 1.2µs sampling time, the output can be corrected by 36mV in each line.

Using a smaller value of CX1 increases both the voltage that can be corrected, and the drift while being held, likewise, using a larger value of CX1, reduces the voltages.

The RX1 resistor is in the circuit purely to simulate some external source impedance, and is not needed as a real

component. Likewise for RX2. The 75Ω back terminating resistor RXT is recommended when driving 75Ω cables.

The board layout should have a ground plane underneath the EL4089, with the ground plane cut away from the vicinity of the V_{IN}- pin, (pin 1). This helps to minimize the stray capacitance on pin 1.

Power supply bypassing is important, and a 0.1µF ceramic capacitor, from each power pin to ground, placed very close to the power pins, together with a 4.7µF tantalum bead capacitor, is recommended.

When both digital and analog grounds are on the same board, the EL4089 should be on the analog ground. The digital ground can be connected to the Analog ground through a 100Ω-300Ω resistor, near the EL4089. This allows the digital signal a return path, while preventing the digital noise from corrupting the analog ground.

TABLE OF CHARGE STORAGE CAPACITOR VS DROOP CHARGING RATES (NOTE)

CAP VALUE nF	DROOP IN 60µs mV	CHARGE IN 1.2µs mV	CHARGE IN 4µs mV
10	6	36	120
33	1.8	11	36
100	0.6	3.6	12

NOTE: Basic formulae are: V (droop) = Ib+ * (Line time - Sample time) / Capacitor and V (charge) = I_{OUT} * Sample time / Capacitor

For best results the source impedance should be kept low, using a buffer for example.

The S/H amplifier is current output and causes a small load on the input source during sampling. When sampling is done on the back porch with color burst there will be a small load on the color burst. Therefore for best performance, the input should be driven from an amplifier output or a 75Ω cable with 75Ω termination.

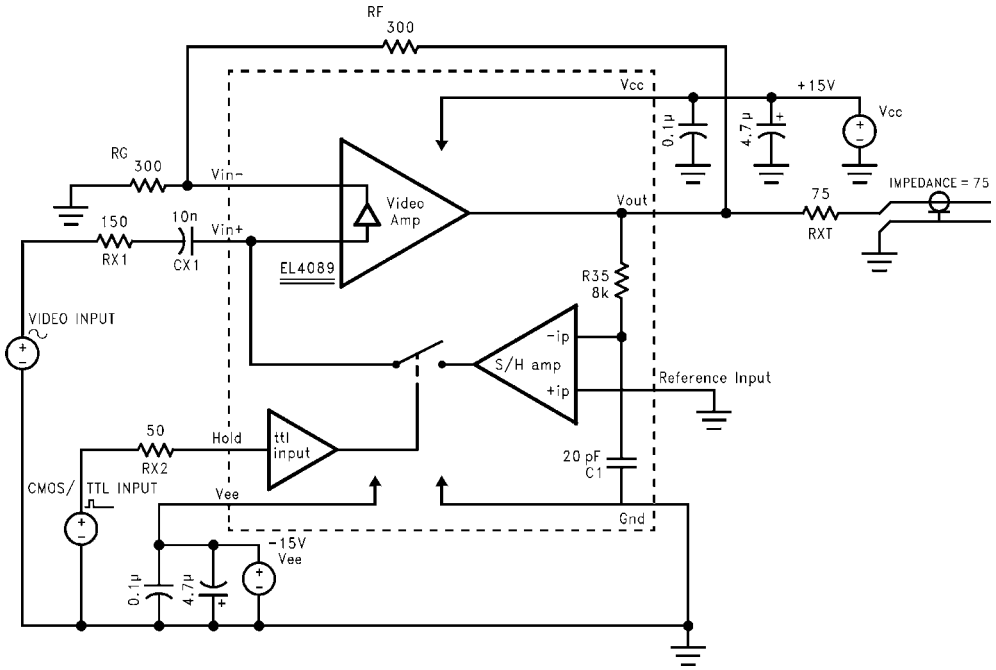


FIGURE 1.

EL4089 Macromodel

```
* Connections:      VIN-
*                   |   VIN+
*                   |   |   Ref
*                   |   |   |   Hold
*                   |   |   |   |   -Vsupply
*                   |   |   |   |   |   VOUT
*                   |   |   |   |   |   |   +Vsupply
*                   |   |   |   |   |   |   |
.subckt EL4089/EL 1   2   3   4   6   7   8
******** Restore section
g10 2 0 xx 0 430u
e10 yy 0 WW 3 4.66
Rfl 7 ww 8K
Cfl ww 0 20p
Rd yy ss 100
d10 xx 0 dd
d20 0 xx dd
s1 xx ss 4 0 swno
s2 0 xx 4 0 swnc
rsl 3 0 999K
Rhh 4 0 100K
.model swno vswitch (von=0.8 voff=2.4)
.model swnc vswitch (von=2.4 voff=0.8)
**********************
* Input Stage
e1 10 0 2 0 1.0
vis 10 9 0V
h2 9 12 Vxx 1.0
r1 1 11 20
I1 11 12 20nH
iinp 2 0 1u
iinn 1 0 18u
r12 2 0 2MEG
* Slew Rate Limiting
H1 13 0 vis 600
r2 13 14 1k
d1 14 0 dd
d2 0 14 dd
* High Frequency Pole
e2 30 0 14 0 0.00166666666
l3 30 17 1.47u
c5 17 0 0.47p
r5 17 0 700
* Transimpedance Stage
g1 0 18 17 0 1.0
rol 18 0 800k
cdp 18 0 11p
* Output Stage
q1 6 18 19 qp
q2 8 18 20 qn
q3 8 19 21 qn
q4 6 29=0 22 qp
r7 21 7 3
r8 22 7 3
ios1 8 19 2mA
iso2 20 6 2mA
*Supply Current
ips 8 6 6.5mA
*Error Term
```

```
iovs 0 23 12m
Vxx 23 0 0V
e4 24 0 2 0 1.0
e5 25 0 8 0 1.0
e6 26 0 6 0 1.0
r9 23 24 560
r10 25 23 1k
r11 26 23 1k
* Models
.model qn npn (is=5e-15, bf=100, tf=0.1ns)
.model qp pnp (is=5e-15, bf=100, tf=0.1ns)
.model dclamp d(is=1e-20, ibv=0.266, bv=2.24, n=4)
```

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