élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4101C - Preliminary

500MHz Video Front End - 4:1MUX + DC-Restore

Features

- 4:1 multiplexer with monitor out
- DC-restore amplifier
- ±5V operation
- 500MHz bandwidth

Applications

- HDTV/DTV analog inputs
- Video projectors
- Computer monitors
- Set top boxes
- Security video
- Broadcast video equipment

Ordering Information

Part No.	Package	Tape & Reel	Outline #
EL4101CU	24-Pin QSOP		MDP0040

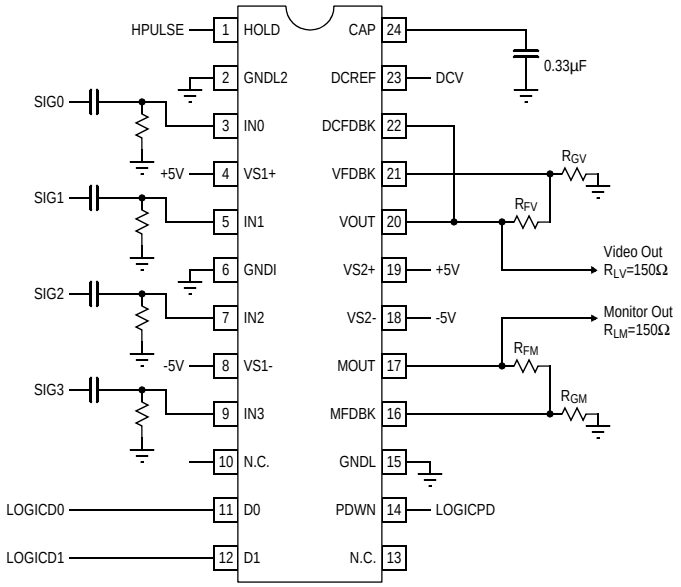
General Description

The EL4101C VFE (Video Front End) is designed to perform the basic input processing functions in an analog video system as well as provide analog input processing for digital video systems. The EL4101C VFE contains a 4:1 MUX input and a DC-restore amplifier. The MUX input can be used to select which input to use. The DC-restore allows the input signal to be positioned to the correct voltage level for either analog or digital processing. A buffered output of the MUX selection is also available for use as a monitor output.

With a 500MHz bandwidth and only 40mA supply current, the EL4101C is ideal for use in portable and fixed projectors, as well as HDTV, DTV and other high performance video applications.

The EL4101C is available in the 24-pin QSOP package and is specified for operation over the full -40°C to +85°C temperature range.

Connection Diagram



Note: Pin #6 should be a good high frequency ground

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Absolute Maximum Ratings (T_A = 25°C)

Values beyond absolute maximum ratings can cause the device to be pre-maturely damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (V_{S+} to V_S-)	11V
Input Voltage	V_S- - 0.3V, V_{S+} +0.3V
Storage Temperature Range	-65°C to +150°C
Ambient operating Temperature	-40°C to +85°C
Operating Junction Temperature	125°C
Power Dissipation	See Curves

Important Note:

All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$.

Electrical Characteristics

$V_{S1}+ = V_{S2}+ = 5V$, $V_{S1}- = V_{S2}- = -5V$, $R_{FV} = R_{GV} = R_{FM} = R_{GM} = 375$, $R_{LV} = R_{LM} = 150\Omega$, $C_{LV} = C_{LM} = 3p$, $C_H = 0.33n$, GAIN = 2.

Parameter	Parameter Description	Conditions	Min	Typ	Max	Unit
Supply						
$I_{S1}+$	Positive Supply Current 1			25		mA
I_S-	Negative Supply Current			38		mA
$I_{S2}+$	Positive Supply Current 2	V_{IN} = 0, I_L = 0		15		mA
$I_{S1S}+$	Positive Supply Current 1 in Standby	Standby		3.8		mA
$I_{SS}-$	Negative Supply Current in Standby	Standby		2		mA
$I_{S2S}+$	Positive Supply Current 2 in Standby	Standby		236		µA
Input						
I_B	Input Bias Current	V_{IN} = 0V	-22.4	-2.2	6.1	µA
I_{BO}	Input Bias Current Drift with Temp.	V_{IN} = 0V		TBD		nA/°C
V_{IH}	Input High Voltage		2			V
V_{IL}	Input Low Voltage				0.8	V
I_{IL}	Low Input Current for D0, D1, PDWN, HOLD	V_{IN} = 0V	25	48	75	µA
I_{IH}	High Input Current for D0, D1, PDWN, HOLD	V_{IN} =5V	0	-	10	µA
t_{SH}	Sample and Hold Delay Time			12		ns
Output						
V_{OSM}	Output Offset Voltage - Monitor	V_{IN} = 0V	-400	18	420	mV
V_{OS}	DC-restore Offset Voltage	Auto-zero on, DC_{REF} = 0	-5	-	5	mV
δV_{OS}	Output Offset Voltage Drift - Video	Auto-zero on		TBD		µV/°C
V_{OH}	Output Voltage Swing, Pos.	A_V = +1, monitor & video outputs	3.44	3.5		V
V_{OL}	Output Voltage Swing, Neg.	A_V = +1, monitor & video outputs	-3.43	-3.5		V
I_{SC}	Output Short Circuit Current	R_L = 10Ω, source or sink	65	100	140	mA
AC Performance						
SR	Slew Rate - Video Out (20%-80%)	$V_{OUT} = 4V_{P-P}$	1000	2100	4500	V/µs
SRM	Slew Rate - Monitor Out (20%-80%)	$V_{OUT} = 4V_{P-P}$	1250	2100	3900	V/µs
OS	Output Overshoot, Video	$V_{OUT} = 1V_{P-P}$		TBD		%
OSM	Output Overshoot, Monitor	$V_{OUT} = 1V_{P-P}$		TBD		%
t_S	Settling Time to 1%, Video	Hold mode		10		ns
t_{SM}	Settling Time to 1%, Monitor			10		ns
V_{REF}	DC-restore -Reference Voltage Range	V_{IN} = -2V to +2V	-2	-	2	V
t_{SD}	DC-restore - Settling Time to 1%	Sample mode on		2.5		µs
V_{OHS}	DC-restore - Video Output Hold Step	S - H transition		-0.5		mV
V_{OSB}	DC-restore - Offset vs. Black Level	Sample mode on	-1	-0.6	1	mV/V
I_{CCL}	DC-restore - Charge Current Limit, I_{CAP}	Sample mode on	210	260	345	µA
I_{DC}	DC-restore - Droop Current, I_{CAP}	Hold mode on	-30	-	30	nA

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V_{S1}+ = V_{S2}+ = 5V, V_{S1}- = V_{S2}- = -5V, R_{FV} = R_{GV} = R_{FM} = R_{GM} =375, R_{LV} = R_{LM} = 150Ω, C_{LV} = C_{LM} = 3p, C_H = 0.33n, GAIN = 2.

Parameter	Parameter Description	Conditions	Min	Typ	Max	Unit
BW	3dB Bandwidth, Video Out			500		MHz
BWM	3dB Bandwidth, Monitor Out			1000		MHz
0.1BW	±0.1dB Flat Bandwidth, Video Out			25		MHz
0.1BWM	±0.1dB Flat Bandwidth, Monitor Out			18		MHz
Vp	Peaking, Video			2.4		dB
Vpm	Peaking, Monitor			4.5		dB
dP	Diff. Phase @3.58MHz, Video			TBD		°
dG	Diff. Gain @3.58MHz, Video			TBD		%
dPM	Diff. Phase @3.58MHz, Monitor			TBD		°
dPG	Diff. Gain @3.58MHz, Monitor			TBD		%
e_n	Noise Voltage at Input for VOUT			TBD		nV/√Hz
e_{nm}	Noise Voltage at Input for MOUT			TBD		nV/√Hz
	Crosstalk [1] @10MHz	3 channel hostile		-45		dB
	Crosstalk [1] @100MHz	3 channel hostile		-20		dB

1. Total unwanted output normalized by wanted (or expected) output; add -10dB to get channel-to-channel isolation

Parallel Programming Truth Table

Inputs			State
PDWN	D1	D0	
0	0	0	IN0 Selected
0	0	1	IN1 Selected
0	1	0	IN2 Selected
0	1	1	IN3 Selected
1	X	X	Standby - Powered Down

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Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	HOLD	Logic Input	Hold pulse for DC-restore function
2	GNDL2	Logic Ground	Logic ground for “hold” buffer
3	IN0	High Frequency Signal	Video input #0
4	VS1+	Power	Positive power pin for quiet supply currents
5	IN1	High Frequency Signal	Video input #1
6	GNDI	Analog Signal	Reference voltage for attenuation function
7	IN2	High Frequency Signal	Video input #2
8	VS1-	Power	Negative power pin for quiet supply currents
9	IN3	High Frequency Signal	Video input #3
10			No connection
11	D0	Logic Input	Parallel control bit #0
12	D1	Logic Input	Parallel control bit #1
13			No connection
14	PDWN	Logic Input	Power down input to put chip in low current standby mode
15	GNDL	Logic Ground	Logic ground for D0, D1, PWDN buffers
16	MFDBK	High Frequency Signal	Monitor amplifier feedback
17	MOUT	High Frequency Signal	Monitor amplifier output
18	VS2-	Power	Negative power pin for heavy, pulsatile supply currents
19	VS2+	Power	Positive power pin for heavy, pulsatile supply currents
20	VOUT	High Frequency Signal	Video amplifier output
21	VFDBK	High Frequency Signal	Video amplifier feedback
22	DCFDBK	Analog Signal	Input to sample circuit
23	DCREF	Analog Signal	Reference DC voltage representing black level
24	CAP	Analog Signal	Sample storage capacitor for DC-restore circuit

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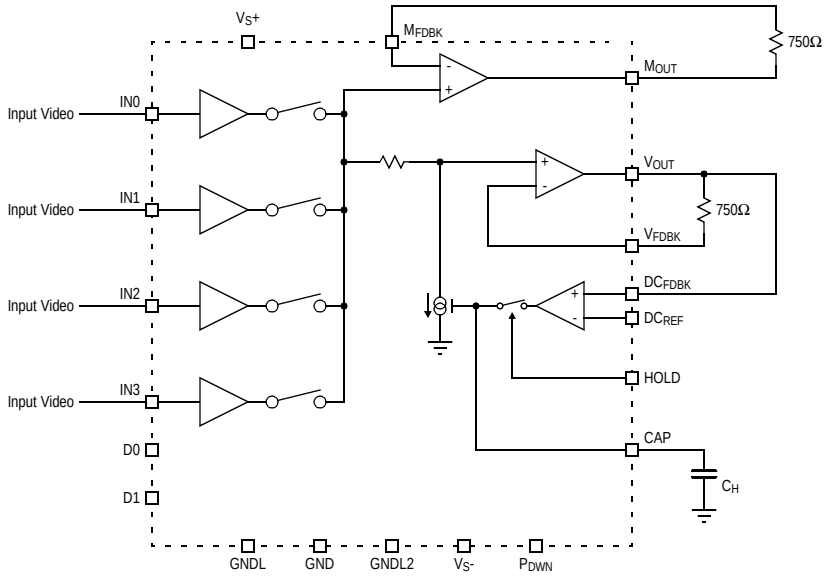
Block Diagram (Gain of 1)



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General Disclaimer

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