EL4102C - Preliminary

500MHz Video Front End: 4-1 MUX, VGA & DC-Restore

Features

- 4:1 multiplexer with monitor out
- 18dB variable gain amplifier
- DC-restore amplifier
- Digital control serial interface
- ±5V operation
- 500MHz bandwidth

Applications

- HDTV/DTV Analog Inputs
- Video Projectors
- Computer Monitors
- Set Top Boxes
- Security Video
- Broadcast Video Equipment

Ordering Information

Part No.	Package	Tape & Reel	Outline #
EL4102CU	24-Pin QSOP		MDP0040

General Description

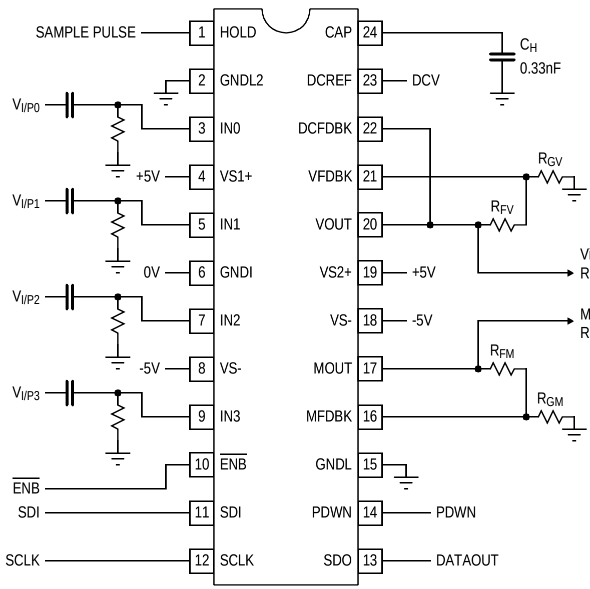
The EL4102C VFE (Video Front End) is designed to perform all of the input processing functions in an analog video system as well as provide analog input processing for digital video systems. The EL4102C VFE contains a 4:1 MUX input, a DC-restore amplifier and a variable gain amplifier. The MUX input can be used to select which input to use. In a digital system, the DC-restore and variable gain amplifiers allow the input signal to be positioned and scaled to give optimum A-to-D conversions results. In an analog system these perform the brightness and contrast operations. A buffered output of the MUX selection is also available for use as a monitor output.

With a 500MHz bandwidth and only 50mA supply current, the EL4102C is ideal for use in portable and fixed projectors, as well as HDTV, DTV and other high performance video applications.

A 3-wire digital interface enables full control of the input selection, as well as 0 to -18dB of gain and blanking operations.

The EL4102C is available in the QSOP24 package and is specified for operation over the -40°C to +85°C temperature range.

Connection Diagram



Note: All information contained in this data sheet has been carefully checked and is believed to be accurate as of the date of publication; however, this data sheet cannot be a "controlled document". Current revisions, if any, to these specifications are maintained at the factory and are available upon your request. We recommend checking the revision level before finalization of your design documentation.

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Absolute Maximum Ratings ($T_A = 25°C$)

Values beyond absolute maximum ratings can cause the device to be prematurely damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (V_{S+} to V_{S-})	11V
Input Voltage	V_S- - 0.3V, V_{S+} +0.3V
Storage Temperature Range	-65°C to +150°C
Ambient operating Temperature	-40°C to +85°C
Operating Junction Temperature	125°C
Power Dissipation	See Curves

Important Note:

All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$.

Electrical Characteristics

$V_{S1}+ = V_{S2}+ = 5V$, $V_{S1}- = V_{S2}- = -5V$, $R_{FV} = R_{FG} = 750$, $R_{GV} = R_{GM} =$ O.C., $A_V = 1$, $R_LV = R_{LM} = 150\Omega$, $C_{LV} = C_{LM} = 3p$, $C_H = 0.33n$, GAIN = 1.

Parameter	Description	Conditions	Min	Typ	Max	Unit
Supply						
$I_{S1}+$	Positive Supply Current 1			35		mA
I_S-	Negative Supply Current	$V_{IN} = 0$, $I_L = 0$		45		mA
$I_{S2}+$	Positive Supply Current 2	$V_{IN} = 0$, $I_L = 0$	14	15	20	mA
$I_{S1S}+$	Positive Supply Current 1 in Standby	Standby	3.8	5	7.3	mA
$I_{SS}-$	Negative Supply Current in Standby	Standby	0.57	1	1.3	mA
$I_{S2S}+$	Positive Supply Current 2 in Standby	Standby	-10	-	10	µA
$V_{S1}+$, $V_{S2}+$	Positive Supply Voltage		4.5	5.0	5.5	V
V_S-	Negative Supply Voltage		-4.5	-5.0	-5.5	V
Input						
Ib	Input Bias Current	V_{IN} = 0V	-22.4	-2.2	6.1	µA
Ibo	Input Bias Current Drift with Temp.	V_{IN} = 0V		TBD		nA/°C
V_{IH}	Input High Voltage		2			V
V_{IL}	Input Low Voltage				0.8	V
V_{IP}	Input Voltage Swing, Pos.	Saturated Input, Att. code = 01010	3.35	3.5		V
V_{IN}	Input Voltage Swing, Neg.	Saturated Input, Att. code = 01010		-3.5	-3.39	V
I_{IDL}	Low Input Current for SCLK and $\overline{ENB}$	V_{IN} = 0V	50	85	150	µA
I_{IDH}	High Input Current for SCLK and $\overline{ENB}$	V_{IN} =5V	0	0.1	10	µA
I_{IL}	Low Input Current for SDI, PDWN, HOLD	V_{IN} = 0V	15	48	75	µA
I_{IH}	High Input Current for SDI, PDWN, HOLD	V_{IN} =5V	0	0.1	10	µA
tsh	Sample and Hold Delay Time			15		ns
tsu	Data Set Up Time		TBD	10	TBD	ns
th	Data Hold Time		TBD	10	TBD	ns
fclk	Serial Clock Rate			TBD	5	MHz
tsue	Enable Set Up Time		TBD	10		ns
the	Enable Hold Time		TBD	10		ns
tpd	Clock to Data Output Delay	C_L = 10pF	TBD	21		ns
Output						
V_{OSM}	Output Offset Voltage - Monitor	V_{IN} = 0V	-400	30	420	mV
V_{OS}	DC-restore Offset Voltage	auto-zero on, DC_{REF} = 0	-5	-	5	mV
T_CV_{OS}	Output Offset Voltage Drift - Video	auto-zero on		15		µV/°C
V_O+	Output Voltage Swing, Pos.	Attenuator = 0dB, Monitor & Video Outputs	3.44	3.5		V
V_O-	Output Voltage Swing, Neg.	Attenuator = 0dB, Monitor & Video Outputs		-3.5	-3.43	V
V_{SDO} high	Serial Data Output High	I_L = +1mA		4.7		V
V_{SDO} low	Serial Data Output Low	I_L = -1mA		0.25		V

Electrical Characteristics

$V_{S1}+ = V_{S2}+ = 5V$, $V_{S1}- = V_{S2}- = -5V$, $R_{FV} = R_{FG} = 750$, $R_{GV} = R_{GM}$ = O.C., $A_V = 1$, $R_LV = R_{LM} = 150\Omega$, $C_{LV} = C_{LM} = 3p$, $C_H = 0.33n$, GAIN = 1.

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{SC}	Output Short Circuit Current	$R_L = 10\Omega$, Source or Sink	65	100		mA
AC Performance						
SR	Slew Rate - Video Out (20%-80%)	$V_{OUT} = 4V_{P-P}$	1000	2100	4500	V/µS
SRM	Slew Rate - Monitor Out (20%-80%)	$V_{OUT} = 4V_{P-P}$	1250	2100	3900	V/µS
OS	Output Overshoot, Video	$V_{OUT} = 1V_{P-P}$		TBD		%
OSM	Output Overshoot, Monitor	$V_{OUT} = 1V_{P-P}$		TBD		%
ts	Settling Time to 1%, Video	Hold Mode		TBD		ns
tsm	Settling Time to 1%, Monitor			TBD		ns
V_{REF}	DC-restore Reference Voltage Range	V_{IN} = -2V to +2V	-2	-	2	V
tsd	DC-restore - Settling Time to 1%	Sample Mode On		1.2		µS
V_{OHS}	DC-restore - Video Output Hold Step	S - H Transition		-1.1		mV
V_{OSB}	DC-restore - Offset vs. Black Level	Sample Mode On	-1	-0.6	1	mV/V
I_{CCL}	DC-restore - Charge Current Limit, I_{CAP}	Sample Mode On		260		µA
I_{DC}	DC-restore - Droop Current, I_{CAP}	Hold Mode On	-30	-	30	nA
BW	3dB Bandwidth, Video Out	Attenuator = 00000		TBD		MHz
BWM	3dB Bandwidth, Monitor Out			TBD		MHz
0.1BW	±0.1dB Flat Bandwidth, Video Out	Attenuator = 00000		TBD		MHz
0.1BWM	±0.1dB Flat Bandwidth, Monitor Out			TBD		MHz
Vp	Peaking, Video			TBD		dB
Vpm	Peaking, Monitor			TBD		dB
dP	Diff. Phase @3.58MHz, Video			TBD		°
dG	Diff. Gain @3.58MHz, Video			TBD		%
dPM	Diff. Phase @3.58MHz, Monitor			TBD		°
dPG	Diff. Gain @3.58MHz, Monitor			TBD		%
e_n	Noise Voltage at Input for V_{OUT}			TBD		nV/√Hz
e_{nm}	Noise Voltage at Input for M_{OUT}			TBD		nV/√Hz
	Crosstalk [1] @10MHz	3 channel hostile		-45		dB
	Crosstalk [1] @100MHz	3 channel hostile		-20		dB
	Attenuator Range		-	18.2	-	dB
	Attenuator Step Size	31 Steps	-	0.58	-	dB
	Relative Attenuation Error	Between any 2 levels	0	-	±0.2	dB

1. Total unwanted output normalized by wanted (or expected) output; add -10dB to get channel-to-channel isolation

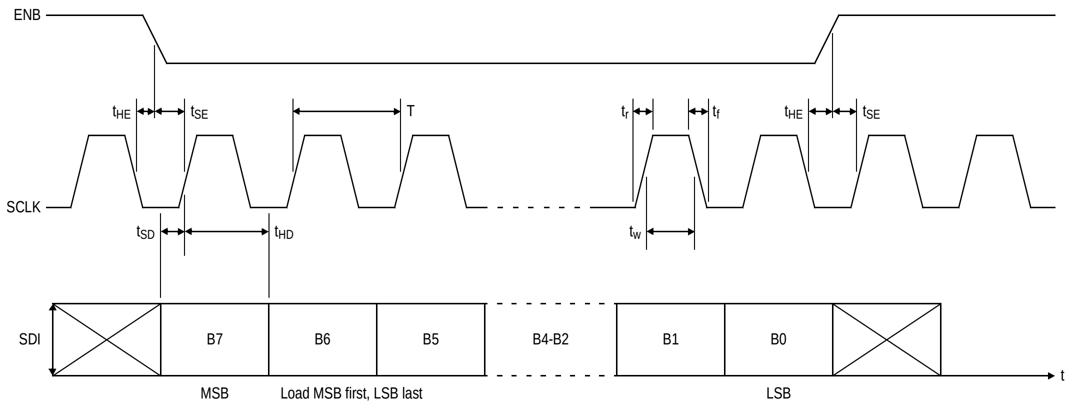
Serial Programming Truth Table

Inputs (X = Don't Care)								Attenuation
Standby	Attenuation					Input Selection		
MSB							LSB	
B7	B6	B5	B4	B3	B2	B1	B0	
0	0	0	0	0	0	X	X	0dB = 1.000
0	0	0	0	0	1	X	X	-0.6dB = 0.94
0	0	0	0	1	0	X	X	-1.2dB = 0.88
0	0	0	0	1	1	X	X	-1.7dB = 0.82
0	0	0	1	0	0	X	X	-2.3dB = 0.77
0	0	0	1	0	1	X	X	-2.9dB = 0.7
0	0	0	1	1	0	X	X	-3.5dB = 0.67
0	0	0	1	1	1	X	X	-4.1dB = 0.63
0	0	1	0	0	0	X	X	-4.6dB = 0.59
0	0	1	0	0	1	X	X	-5.2dB = 0.55
0	0	1	0	1	0	X	X	-5.8dB = 0.51
0	0	1	0	1	1	X	X	-6.4B = 0.48
0	0	1	1	0	0	X	X	-7.0dB = 0.45
0	0	1	1	0	1	X	X	-7.5dB = 0.42
0	0	1	1	1	0	X	X	-8.1dB = 0.39
0	0	1	1	1	1	X	X	-8.7dB = 0.37
0	1	0	0	0	0	X	X	-9.3dB = 0.34
0	1	0	0	0	1	X	X	-9.9dB = 0.32
0	1	0	0	1	0	X	X	-10.5dB = 0.30
0	1	0	0	1	1	X	X	-11.0dB = 0.28
0	1	0	1	0	0	X	X	-11.6dB = 0.26
0	1	0	1	0	1	X	X	-12.2dB = 0.25
0	1	0	1	1	0	X	X	-12.8dB = 0.23
0	1	0	1	1	1	X	X	-13.4dB = 0.22
0	1	1	0	0	0	X	X	-13.9dB = 0.20
0	1	1	0	0	1	X	X	-14.5dB = 0.19
0	1	1	0	1	0	X	X	-15.1dB = 0.18
0	1	1	0	1	1	X	X	-15.7dB = 0.17
0	1	1	1	0	0	X	X	-15.3dB = 0.15
0	1	1	1	0	1	X	X	-16.8dB = 0.14
0	1	1	1	1	0	X	X	-17.4dB = 0.13
0	1	1	1	1	1	X	X	-18.0dB = 0.12
0	X	X	X	X	X	1	1	IN3 Selected
0	X	X	X	X	X	1	0	IN2 Selected
0	X	X	X	X	X	0	1	IN1 Selected
0	X	X	X	X	X	0	0	IN0 Selected
1	X	X	X	X	X	X	X	Standby Mode - Powered Down
1	1	1	1	1	1	1	1	Wake-up Condition (-18.0dB, IN3, Powered Down)

Control Bits Logic Table

Bit	Function
B7	Standby - Power Down
B6	Gain Bit 4
B5	Gain Bit 3
B4	Gain Bit 2
B3	Gain Bit 1
B2	Gain Bit 0
B1	Input Select Bit 1
B0	Input Select Bit 0

Serial Timing Diagram



Serial Timing Parameters

Parameter	Example	Description
T	≥100 ns	Clock Period
t_r/t_f	0.05 x T	Clock Rise/Fall Time
t_{HE}	≥40ns	ENB Hold Time
t_{SE}	≥40ns	ENB Setup Time
t_{HD}	≥40ns	Data Hold Time
t_{SD}	≥40ns	Data Setup Time
t_w	0.50 x T	Clock Pulse Width

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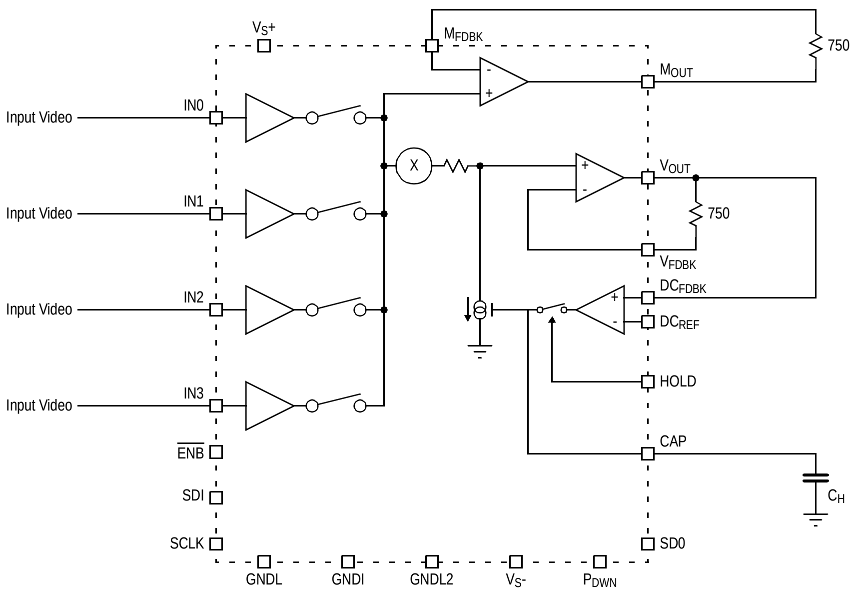
Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	HOLD	Logic Input	Hold pulse for DC-restore function
2	GNDL2	Logic Ground	Logic ground for “hold” buffer
3	IN0	High Frequency Signal	Video input #0
4	$V_{S1}+$	Power	Positive power pin for quiet supply currents
5	IN1	High Frequency Signal	Video input #1
6	GNDI	Analog Signal	Intermediate reference for attenuation function
7	IN2	High Frequency Signal	Video input #2
8	V_S-	Power	Negative power pin
0	IN3	High Frequency Signal	Video input #3
10	$\overline{ENB}$	Logic Input	Enable (negative true) input for loading serial data stream
11	SDI	Logic Input	Serial input data stream
12	SCLK	Logic Input	Serial data stream clock
13	SDO	Logic Output	Serial output data stream for connection to cascaded chip
14	P_{DWN}	Logic Input	Power down input to put chip in low current standby mode
15	GNDL	Logic Ground	Logic ground for logic buffers
16	M_{FDBK}	High Frequency Signal	Monitor amplifier feedback
17	M_{OUT}	High Frequency Signal	Monitor amplifier output
18	V_S-	Power	Negative power pin
19	$V_{S2}+$	Power	Positive power pin for heavy, pulsatile supply currents
20	V_{OUT}	High Frequency Signal	Video amplifier output
21	V_{FDBK}	High Frequency Signal	Video amplifier feedback
22	DC_{FDBK}	Analog Signal	Input to sample circuit
23	DC_{REF}	Analog Signal	Reference DC voltage representing black level
24	CAP	Analog Signal	Sample storage capacitor for DC-restore circuit

Block Diagram (Gain of 1)



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Applications Information

Using the Serial Data Output Connection for a Multi-chip Design

In a system design that uses three chips, (i.e. RGB, YUV, YPrPb systems) the control signal may be "daisy chained" through the three chips. This gives an advantage in that the control will be updated simultaneously on the three channels.

The serial data out (SDO) of chip one is connected to the serial data in (SDI) of chip two, similarly, chip two SDO is connected to SDI on chip three. The clock (SCLK) and enable (/ENB) signals are connected in parallel to all three chips. See figure yy for suggested interconnect of the control signals.

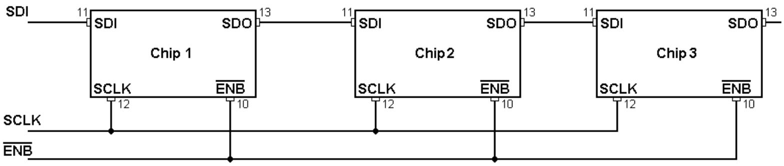
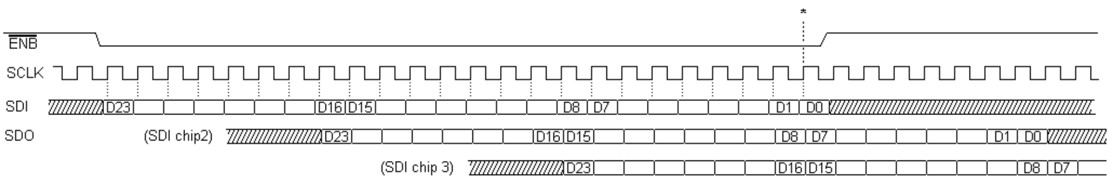


Figure xx shows the control signal waveforms when using this configuration. Note, that the last data bit clocked into the three chips occurs on the last positive clock edge that is within the enabled period. This will be D0 in the first chip, D8 and D16 on the second two chips. The rising edge of /ENB will then simultaneously transfer the data internally to the chip. Typically the data for each chip is held as an image in the micro-controller system; the load operation would prepare the update information as a 24-bit word ready for shifting into the three chips.



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General Disclaimer

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