Overview

Feature

- Tiny 2mm x 1mm x 0.5mm module
- Integrated 940nm IR VCSEL
- Crosstalk and ambient light cancellation
- Wide configuration range
- 2 channels (photopic ASL + IR)
- Offset emitter / detector package design

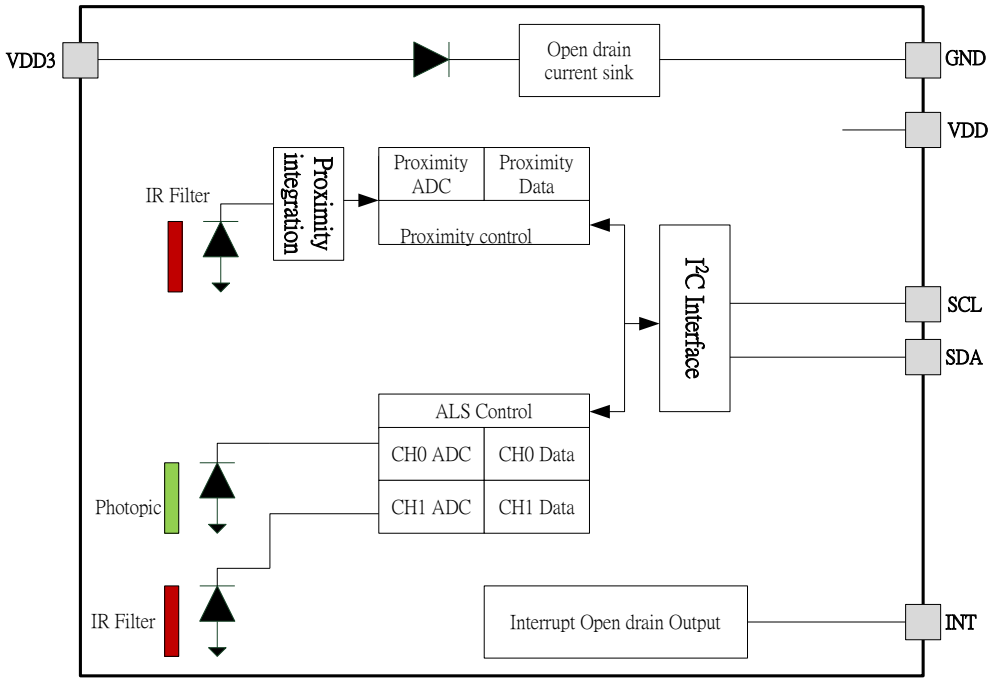
Application

- Mobile phone display management
- Mobile phone and wearable user proximity detection
- Wearable ambient light measurement

Description

The ELM2712 features proximity detection and digital ambient light sensing (ALS). The extremely tiny 2mm x 1mm module incorporates an IR VCSEL and on chip VCSEL driver. The proximity detection feature provides object detection (e.g. mobile device screen to user's ear) by photodiode detection of reflected IR energy (sourced by the integrated VCSEL). Detect/release events are interrupt driven, and occur when proximity result crosses upper and/or lower threshold settings. The proximity engine features a wide range offset adjustment to compensate for unwanted IR energy reflection at the sensor. Proximity results are further improved by automatic ambient light subtraction. The ALS and IR photodiodes have dedicated data converters producing 24-bit data. This architecture allows applications to accurately measure ambient light which enables devices to calculate illuminance to control display backlight.

Block Diagram



Pin Description

Description

Name	Pin No.	IO	Description
INT	1	IO	Interrupt pin (open drain)
GND	2	G	Ground
VDD3	3	P	Supply Voltage for IR emitter (3.0v~3.6v)
SDA	4	IO	IIC data (open drain)
SCL	5	I	IIC clock
VDD	6	P	Power Supply for sensor (1.7v~2.0v)

Electrical Specification

■ Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
VDD	Supply Voltage to GND	-0.3	2.0	V	
VDD3	IR emitter Voltage to GND	-0.3	3.6	V	
V_{IO}	Digital I/O Terminal Voltage	-0.3	3.6	V	
I_{IO}	Digital Output Terminal Current	-1	20	mA	
Electrostatic Discharge					
I_{SCR}	Input Current (latch-up immunity)	± 100		mA	Class II JEDEC JESD78E
ESD_{HBM}	HBM ElectrostaticDischarge	± 2000		V	JEDEC/ESDA JS-001-2017
ESD_{CDM}	CDM ElectrostaticDischarge	± 500		V	JEDEC JS-002-2014
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage TemperatureRange	-40	85	˚C	
T_{BODY}	Package Body Temperature		260	˚C	IPC/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.”
RH_{NC}	Relative Humidity (non-condensing)		85	%	
P_{DISS}	Power Dissipation		50	mW	Average power dissipation over a1 second period

Recommended Operation condition

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Supply Voltage to Sensor	1.7	1.8	1.98	V
VDD3	Supply Voltage to IR emitter	2.9	3.3	3.6	V
f_{I2C}	Clock frequency of I^2C	-	-	400	Khz
T_A	Operating Ambient Temperature	-30		85	˚C

Electrical and Proximity sensor characteristics

Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Active Proximity State (PON=1) (1)		322		μA
		Active ALS State (PON = 1) (1)		124		
		Idle State (PON=1)(2)		23		
		Sleep State (PON = 0) (3)		0.5		
V_{OL}	INT, SDA output low voltage	6mA sink current			0.6	V
I_{LEAK}	Leakage current, SDA, SCL, INT		-5		5	μA
V_{IH}	SCL, SDA input high voltage(3)		1.26			V
V_{IL}	SCL, SDA input low voltage				0.54	V
T_{Active}	Time from power-on to ready to receive I^2C commands			1.5		ms

Note(s):

1. Active state occurs when PON =1 and the device is actively integrating either proximity or ALS. For proximity, this time is determined by the number of pulses (PPLUSE) and the pulse length (PULSE_LEN). For ALS, this time is determined by the ALS integration time (ATIME). Both proximity and ALS active states can occur at the same time
2. Idle state occurs when PON=1 and the device is not in the active state.
3. Sleep state occurs when PON = 0 and I²C bus is idle. If sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.
4. Digital pins: SDA, SCL, INT are tolerant to a communication voltage up to 3.6V

■ ALS optical characteristics

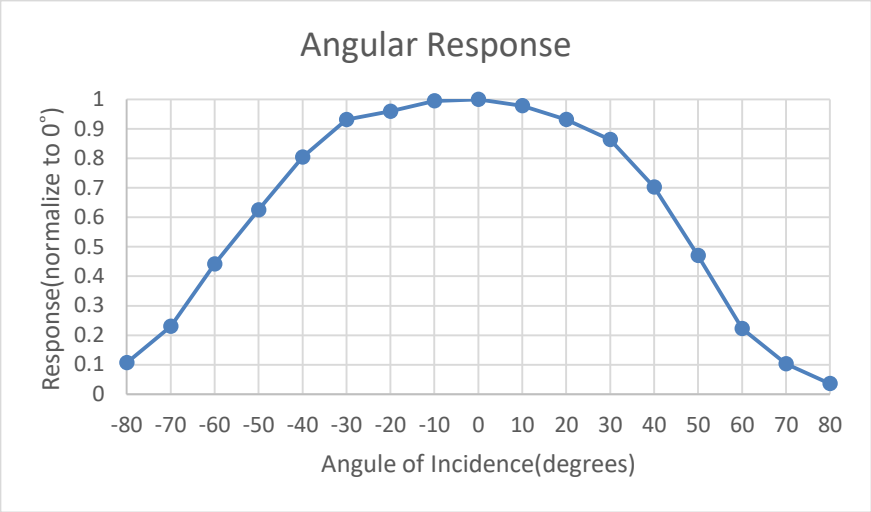
Parameter	Conditions	Min	Typ	Max	Unit
ALS sensitivity 1	6500K LED @ 500Lux AGAIN = 128x ATIME = 100ms	-15%	50105	+15%	Counts
ALS sensitivity 2	6500K LED @ 50Lux AGAIN = 1024x ATIME = 100ms	-15%	40100	+15%	Counts
ALS integration step size		2.746	2.78	2.815	ms
ALS dark count	0μW/cm^2 AGAIN = 1024x ATIME = 50ms	125	225	325	Counts
ALS 16x gain scaling	Relative to 128x		0.125		x
ALS 1024x gain scaling	Relative to 128x		8		x
ALS noise	AGAIN = 128x ATIME = 100ms		0.03		% (σ)

■ Proximity Optical characteristics

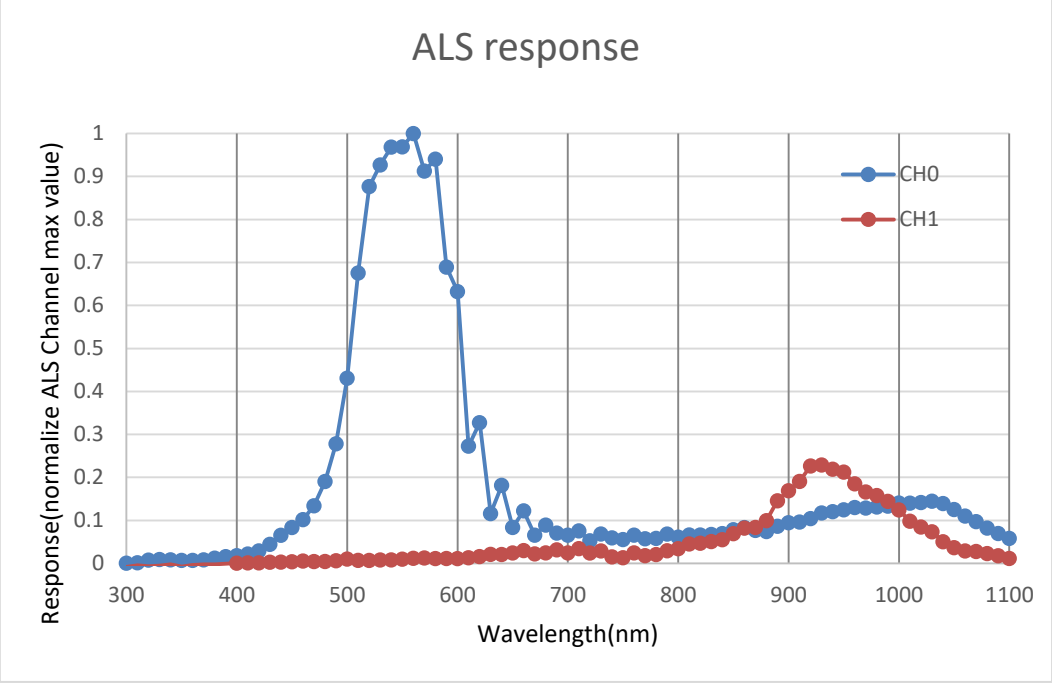
Parameter	Conditions	Min	Typ	Max	Unit
Response: absolute	PGAIN1 = 4x; PGAIN2 = 5x PLDRIVE = 8mA PPULSE = 4 pulses PPULSE_LEN = 34μs HW Averaging = 8 BINSRCH_TARGET = 15 APC = disabled Post Calibration Target material: 18% reflectivesurface No glass above module Target Size: 100mm x 100mm Target Distance: 30mm		285		Counts
Part to Part Variation				±25	%
Response: no target	Same as Response: absoluteexcept no target	4	15	30	Counts

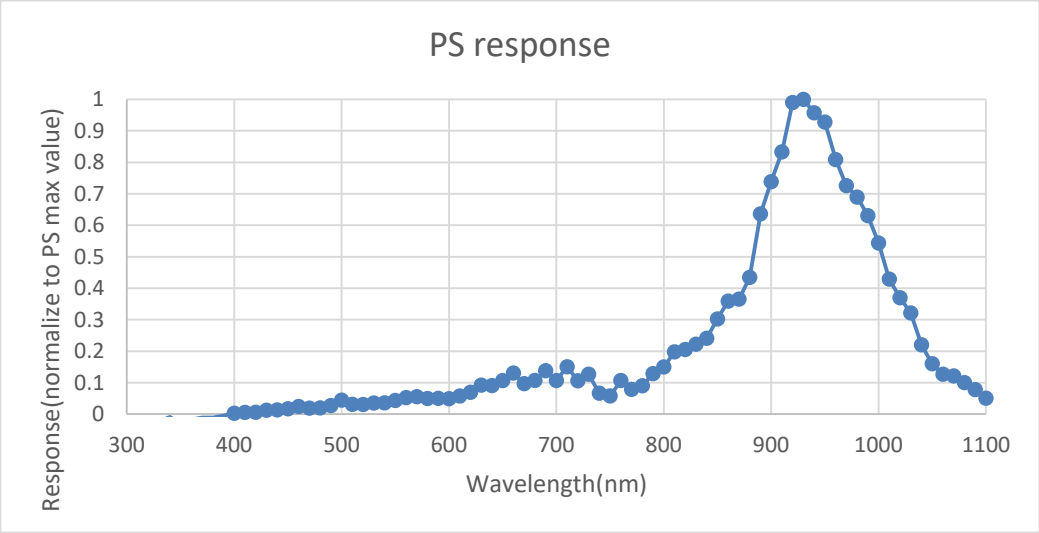
Typical Operating Characteristics

FOV



Spectrum

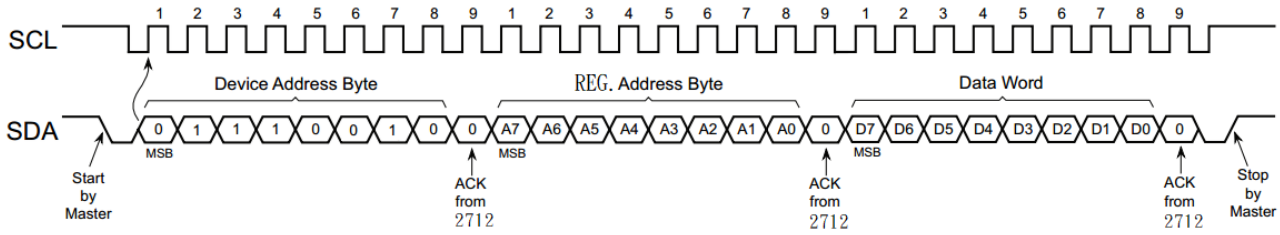



PS response
Response(normalize to PS max value)
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
300
400
500
600
700
800
900
1000
1100
Wavelength(nm)

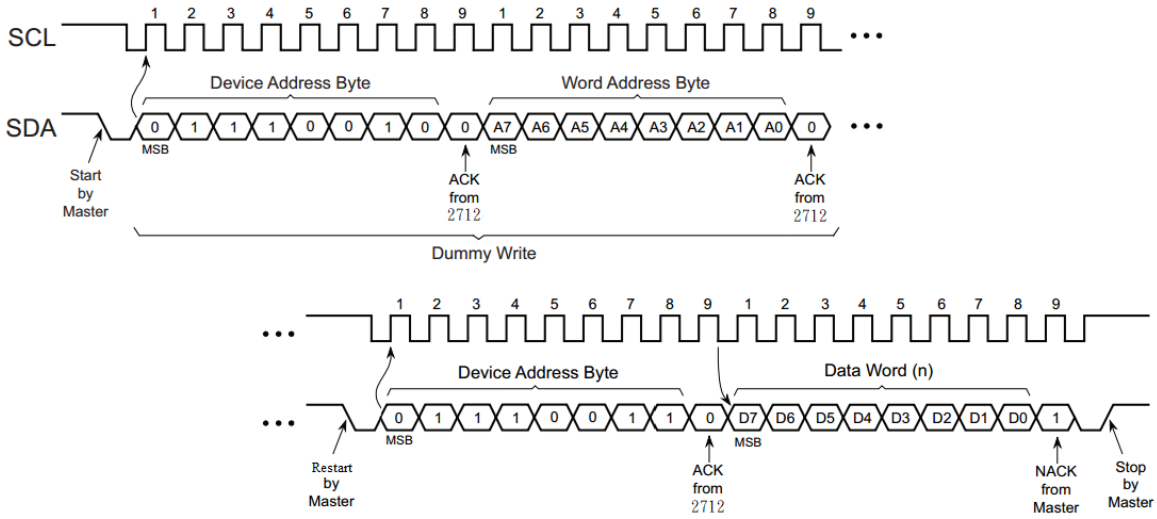
I2C Timing Diagram

IIC Communication

Write:



Read:



■ I2C address selection

Master I²C Bus Signal		7-Bit I²C Address
Clock	Data	
SCL	SDA	0x39
SDA	SCL	0x38

Notes:

A Single dummy I2C access (read or write with valid I2C stop) to the device is required to initialize the device their respective I2C address. The device will feedback a NOT-ACKNOWLEDGE (NACK) during initial dummy access.

Register Description

- Register table

Address	Register Name	R/W	Register Function	Reset Value
0x80	ENABLE	R/W	Enables states and interrupts	0x00
0x81	ATIME	R/W	ALS integration time	0x00
0x82	PRATE	R/W	Proximity time	0x00
0x83	AWTIME	R/W	ALS wait time	0x00
0x84	AILTL	R/W	ALS interrupt low threshold low byte	0x00
0x85	AILTH	R/W	ALS interrupt low threshold high byte	0x00
0x86	AIHTL	R/W	ALS interrupt high threshold low byte	0x00
0x87	AIHTH	R/W	ALS interrupt high threshold high byte	0x00
0x88	PILTL	R/W	Proximity interrupt low threshold low byte	0x00
0x89	PILTH	R/W	Proximity interrupt low threshold high byte	0x00
0x8A	PIHTL	R/W	Proximity interrupt high threshold low byte	0x00
0x8B	PIHTH	R/W	Proximity interrupt high threshold high byte	0x00
0x8C	PERS	R/W	ALS and proximity interrupt persistence filters	0x00
0x8D	CFG0	R/W	Configuration zero	0x50
0x8E	PCFG0	R/W	Proximity configuration zero	0x8F
0x8F	PCFG1	R/W	Proximity configuration one	0x32
0x90	PCFG2	R/W	Proximity configuration one	0x20
0x91	REVID	R	Revision ID	0x00
0x92	ID	R	Device ID	0x64
0x93	CFG1	R/W	Configuration one	0x68
0x94	STATUS	R, SC	Device status	0x00
0x95	ALSL	R	ALS (CH0) low data	0x00
0x96	ALSM	R	ALS (CH0) middle data	0x00
0x97	ALSH	R	ALS (CH0) high data	0x00
0x98	IRL	R	IR (CH1) low data	0x00
0x99	IRM	R	IR (CH1) middle data	0x00
0x9A	IRH	R	IR (CH1) high data	0x00

0x9B	PDATAL	R	Proximity ADC low data	0x00
0x9C	PDATAH	R	Proximity ADC high data	0x00
0xA6	REVID2	R	Revision ID two	0x00
0xA8	SOFTRST	R/W	Soft reset	0x00
0xA9	PWTIME	R/W	Proximity wait time	0x00
0xAB	CFG3	R/W	Configuration three	0x01
0xAE	CFG6	R/W	Configuration six	0x3F
0xC0	POFFSETL	R/W	Proximity offset low data	0x00
0xC1	POFFSETH	R/W	Proximity offset high data	0x00
0xD7	CALIB	R/W	Proximity offset calibration	0x00
0xD8	CALIB_OFFSET	R/W	Proximity extension offset calibration	0x00
0xD9	CALIBCFG	R/W	Proximity offset calibration control	0x50
0xDC	CALIBSTAT	R/W	Proximity offset calibration status	0x00
0xDD	INTENAB	R/W	Interrupt enable	0x00
0xF5	AS_CFG	R/W	ALS Configuration	0x18
0xF6	PSDA	R/W	Proximity offset Calibration	0x60

Detail of Register Description

- *Enable register (Address 0x80)*

Addr: 0x80		ENABLE		
Bit	Bit Name	Default	Access	Bit Description
7:5	Reserved	000	--	Reserved.
4	PWEN	0	RW	**PS Wait Time Enable Flag** This bit activates the proximity wait feature which is setby the PWTIME register. Active high.
3	AWEN	0	RW	**ALS Wait Time Enable Flag** AWEN = 1, ALS wait time is enabled. AWEN = 0, ALS wait time is disabled.
2	PEN	0	RW	**PS Enable Flag** This bit activates the proximity detection. Active high.
1	AEN	0	RW	**ALS Enable Flag** AEN = 1, Ambient light function is enabled. AEN = 0, Ambient light function is disabled.
0	PON	0	RW	**Power On Enable Flag** This field activates the internal oscillator and ADCchannels. Active high.

- *ATIME register (Address 0x81)*

Addr:0x81		ATIME		
Bit	Bit Name	Default	Access	Bit Description
7:0	ATIME	0x00	RW	**ALS Integration Time Value** The ATIME value specifies the ALS integration time in 2.78ms intervals. 0x00 indicates 2.78ms. The maximum ALS count value depends on the integration time.

- *PRATE register (Address 0x82)*

Addr:0x82		PRATE		
Bit	Bit Name	Default	Access	Bit Description

7:0	PRATE	0x00	RW	**PS Integration Time Value** The PRATE value specifies the PS integration time in 2.78ms intervals. 0x00 indicates 2.78ms. The maximum PS count value depends on the integration time.

Note :

- **PS Integration Time depends on the "Pulse Length", "Pulse Number".**
- **PS Integration Time must be set more than 20 x 2 + 2 x (4 + Pulse_Length + 2) x (Pulse_Number + 1) + 9 + 69 (us)**

■ *AWTIME register (Address 0x83)*

Addr:0x83		AWTIME		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AWTIME	0x00	RW	**ALS Wait Time Value** The AWTIME value specifies the ALS wait time in 2.78ms intervals. 0x00 indicates 2.78ms.

■ *AILTL Register (Address 0x84)*

Addr: 0x84		AILTL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AILTL	0x00	RW	**ALS Low Threshold Value** The AILTL value specifies the low byte of the ALS LOW threshold.

■ *AILTH Register (Address 0x85)*

Addr: 0x85		AILTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AILTH	0x00	RW	**ALS Low Threshold Value** The AILTH value specifies the high byte of the ALS LOW threshold.

The ALS Low Threshold (AIL) is obtained by combining the AILTH and AILTL registers and left-shifting them by 8 bits to form a 24-bit threshold value.

■ *AIHTL Register (Address 0x86)*

Addr: 0x86		AIHTL		
Bit	Bit Name	Default	Access	Bit Description
7:0	AIHTL	0x00	RW	**ALS High Threshold Value** The AIHTL value specifies the low byte of the ALS HIGH threshold.

- *AIHTH Register (Address 0x87)*

Addr: 0x87		AIHTH		
Bit	Bit Name	Default	Access	Bit Description
7:0	AIHTH	0x00	RW	**ALS High Threshold Value** The AIHTH value specifies the high byte of the ALS HIGH threshold.

The ALS High Threshold (AIH) is obtained by combining the AIHTH and AITL registers and left-shifting them by 8 bits to form a 24-bit threshold value.

- *PILTL Register (Address 0x88)*

Addr: 0x88		PILTL		
Bit	Bit Name	Default	Access	Bit Description
7:0	PILTL	0x00	RW	**PS Low Threshold Value** This register contains the low byte of the 12-bit proximity LOW threshold when APC is disabled. If APC is enabled, the register contains the low byte of the 16-bit proximity LOW threshold.

- *PILTH Register (Address 0x89)*

Addr: 0x89		AILTH		
Bit	Bit Name	Default	Access	Bit Description
7:0	PILTH	0x00	RW	**PS Low Threshold Value** This register contains the upper 4-bits of the 12-bit proximity LOW threshold when APC is disabled. If APC is enabled, the register contains the high byte of the 16-bit proximity LOW threshold.

■ *PIHTL Register (Address 0x8A)*

Addr: 0x8A		AIHTL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PIHTL	0x00	RW	**PS High Threshold Value** This register contains the low byte of the 12-bit proximity HIGH threshold when APC is disabled. If APC is enabled, the register contains the low byte of the 16-bit proximity HIGH threshold.

■ *PIHTH Register (Address 0x8B)*

Addr: 0x8B		AIHTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PIHTH	0x00	RW	**PS High Threshold Value** This register contains the upper4-bits of the 12-bit proximity HIGH threshold when APC is disabled. If APC is enabled, the register contains the high byte of the 16-bit proximity HIGH threshold.

■ *PERS Register (Address 0x8C)*

Addr: 0x8C		PERS			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:4	PPERS	0000	RW	This register sets the PS persistence filter.	
				0 (0000)	Every PS cycle
				1 (0001)	Any value outside PS thresholds
				2 (0010)	2 consecutive PS values out of range
				3 (0011)	3 consecutive PS values out of range
				4 (0100)	4 consecutive PS values out of range
				5 (0101)	5 consecutive PS values out of range
				6 (0110)	6 consecutive PS values out of range
				7 (0111)	7 consecutive PS values out of range
				...	
				13 (1101)	13 consecutive PS values out of range

				14 (1110)	14 consecutive PS values out of range
				15 (1111)	15 consecutive PS values out of range
3:0	APERS	0000	RW	This register sets the ALS persistence filter.	
				0 (0000)	Every ALS cycle
				1 (0001)	Any value outside ALS thresholds
				2 (0010)	2 consecutive ALS values out of range
				3 (0011)	3 consecutive ALS values out of range
				4 (0100)	5 consecutive ALS values out of range
				5 (0101)	10 consecutive ALS values out of range
				6 (0110)	15 consecutive ALS values out of range
				...	
				13 (1101)	50 consecutive ALS values out of range
				14 (1110)	55 consecutive ALS values out of range
				15 (1111)	60 consecutive ALS values out of range

■ *CFG0 Register (Address 0x8D)*

Addr: 0x8D		CFG0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved	0101	--	Reserved. **Must be set to default value.**
3	PWLONG	0	RW	**PS Wait Long Flag** The PWTIME is increased by a factor of 16 when PWLONG is asserted. PWLONG = 1, PWTIME = PWTIME x 16 PWLONG = 0, PWTIME = PWTIME x 1
2	AWLONG	0	RW	**ALS Wait Long Flag** The AWTIME is increased by a factor of 16 when AWLONG is asserted. AWLONG = 1, AWTIME = AWTIME x 16 AWLONG = 0, AWTIME = AWTIME x 1
1:0	Reserved	00	RW	Reserved. **Must be set to default value.**

■ *PCFG0 Register (Address 0x8E)*

Addr: 0x8E		PFCG0		
Bit	Bit Name	Default	Access	Bit Description
7:6	PGAIN1	10	RW	**PS Gain 1 Value** PGAIN1 = 0, 1x gain. PGAIN1 = 1, 2x gain. PGAIN1 = 2, 4x gain. PGAIN1 = 3, 8x gain.
5:0	PPULSE	001111	RW	**PS Pulse Number Value** The PPULSE sets the maximum number of pulses in a single proximity cycle. Max. pulse number=64

■ *PCFG1 Register (Address 0x8F)*

Addr: 0x8F		PFCG1		
Bit	Bit Name	Default	Access	Bit Description
7:6	PPULSE_LENH	00	RW	**PS Pulse Length High Byte Value** These bits are the 2 most significant bits of the 10-bit pulse length control setting. The lower 8 bits are in the PCFG2 register. The minimum pulse length is 5μs.
5:4	Reserved	11	--	Reserved. **Must be set to default value.**
3:0	PLDRIVE	0010	RW	**PS Pulse Drive Current** The drive strength of the IR VCSEL current is set by the field

Value	VCSEL Current
(0001)1	7mA
(0010)2	8mA
(0011)3	9mA
(0100)4	10mA
(0101)5	3mA
(0110)6	4mA
(0111)7	5mA
(1000)8	6mA
others	7mA

■ PCFG2 Register (Address 0x90)

Addr: 0x90		PCFG2		
Bit	Bit Name	Default	Access	Bit Description
7:0	PPULSE_LENL	0x20	RW	**PS Pulse Length Low Byte Value** These bits are the 8 least significant bits of the 10-bit pulse length control setting. The upper 2 bits are in the PCFG1 register. The minimum pulse length is 5μs.

■ REVID Register (Address 0x91)

Addr: 0x91		REVID		
Bit	Bit Name	Default	Access	Bit Description
7:3	Reserved	00000	RO	Reserved.
2:0	REVID	000	RO	Device revision number.

■ ID Register (Address 0x92)

Addr: 0x92		ID		
Bit	Bit Name	Default	Access	Bit Description
7:2	ID	011001	RO	Device type identification.
1:0	Reserved	00	RO	Reserved.

■ CFG1 Register (Address 0x93)

Addr: 0x93		CFG1		
Bit	Bit Name	Default	Access	Bit Description
7	Reserved	0	--	Reserved.
6:5	PGAIN2	11	RW	**PS Gain2 Value** PGAIN2 = 0, 2.5x gain. PGAIN2 = 1, 5x gain. PGAIN2 = 3, 10x gain. Others, 1x gain
4:0	AGAIN	01000	RW	**ALS Gain Value**

				AGAIN = 8, 128x gain. AGAIN = 11, 1024x gain. Others, Reserved.

- STATUS Register (Address 0x94)

Addr: 0x94		STATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ASAT	0	R, SC	**ALS Saturation Flag** Analog saturation flag signals that the ALS results may be unreliable due to saturation of the AFE. (Note : λ data = 16'hFFFF)
6	PSAT	0	R, SC	**PS Saturation Flag** Proximity saturation flag indicates that an ambient- or reflective-saturation event occurred during a previous proximity cycle. (Note : PS_IR data = 12'h000 or PS_EM data = 12'h000 including hardware average)
5	PINT	0	R, SC	**PS Interrupt Flag** Proximity interrupt flag indicates that proximity results have exceeded thresholds and persistence settings.
4	AINT	0	R, SC	**ALS Interrupt Flag** ALS interrupt flag indicates that proximity results have exceeded thresholds and persistence settings.
3	CINT	0	R,SC	**Calibration Interrupt Flag** Calibration interrupt flag indicates that calibration has completed.
2	ZINT	0	R,SC	**PS Zero Detection Flag** Zero detection interrupt flag indicates that a zero value in PDATA has caused the proximity offset to be decremented (if AUTO_OFFSET_ADJ = 1).
1	PSAT_REFLE	0	R,SC	**PS Reflective Proximity Saturation Flag** The Reflective Proximity Saturation Interrupt flag signals

				that the AFE has saturated during the IR VCSEL active portion of proximity integration. (Note : one PS_IR data = 12'h000)
0	PSAT_AMBIT	0	R,SC	**PS Ambient Proximity Saturation Flag** The Ambient Proximity Saturation Interrupt flag signals that the AFE has saturated during the IR VCSEL inactive portion of proximity integration. (Note : one PS_EM data = 12'h000)

- ALSL Register (Address 0x95)

Addr: 0x95		ALSL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ALSL	0x00	RO	**ALS Channel 0 Low Byte Data** This register contains the low byte of the 24-bit ALS channel (CH0) data.

- ALSM Register (Address 0x96)

Addr: 0x96		ALSM		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ALSM	0x00	RO	**ALS Channel 0 Middle Byte Data** This register contains the middle byte of the 24-bit ALS channel (CH0) data.

- ALSH Register (Address 0x97)

Addr: 0x97		ALSH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ALSH	0x00	RO	**ALS Channel 0 High Byte Data** This register contains the high byte of the 24-bit ALS channel (CH0) data.

- IRL Register (Address 0x98)

Addr: 0x98		IRL		
Bit	Bit Name	Default	Access	Bit Description
7:0	IRL	0x00	RO	**ALS Channel 1 low Byte Data** This register contains the low byte of the 24-bit ALS channel (CH1) data.

- IRM Register (Address 0x99)

Addr: 0x99		IRM		
Bit	Bit Name	Default	Access	Bit Description
7:0	IRM	0x00	RO	**ALS Channel 1 Middle Byte Data** This register contains the middle byte of the 24-bit ALS channel (CH1) data.

- IRH Register (Address 0x9A)

Addr: 0x9A		ALSH		
Bit	Bit Name	Default	Access	Bit Description
7:0	IRH	0x00	RO	**ALS Channel 1 High Byte Data** This register contains the high byte of the 24-bit ALS channel (CH1) data.

- PDATAL Register (Address 0x9B)

Addr: 0x9B		PDATAL		
Bit	Bit Name	Default	Access	Bit Description
7:0	PDATAL	0x00	RO	**PS Low Byte Data (PS_L_Data)** This register contains the low byte of the 16-bit proximity ADC data.

- PDATAH Register (Address 0x9C)

Addr: 0x9C		PDATAH		
Bit	Bit Name	Default	Access	Bit Description
7:0	PDATAH	0x00	RO	**PS High Byte Data (PS_H_Data)**

				This register contains the High byte of the 16-bit proximity ADC data.

■ REVID2 Register (Address 0xA6)

Addr: 0xA6		REVID2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved	0000	RO	Reserved.
3:0	VER_ID	0000	RO	Device Version Number

■ SOFTRST Register (Address 0xA8)

Addr: 0xA8		IRM		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	Reserved	000000	--	Reserved.
1	POR	0	RW	**Power On Reset Enable Flag** Writing a 1 to this bit will cause a power on reset. This will immediately terminate all device operation and put the device into the sleep state. POR = 1, All device operation will be terminated immediately. POR = 0, Normal operation.
0	SOFTRST	0	RW	**Software Reset Enable Flag** Writing a 1 to this bit will cause all registers to be reset to their default state. This will immediately terminate all device operation and put the device into the sleep state. SOFTRST = 1, All registers will be reset to the default state. SOFTRST = 0, Normal operation.

■ PWTIME Register (Address 0xA9)

Addr: 0xA9		PWTIME		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**

<table>
<tr><td rowspan="11">7:0</td><td rowspan="11">PWTIME</td><td rowspan="11">0x00</td><td rowspan="11">RW</td><td colspan="3">PS Wait Time Value
The PWTIME value specifies the PS wait time in 2.78ms intervals. 0x00 indicates 2.78ms.</td></tr>
<tr><td>PWTIME</td><td>Wait Cycles</td><td>Wait Time</td></tr>
<tr><td>0x00</td><td>1</td><td>2.78ms</td></tr>
<tr><td>0x01</td><td>2</td><td>5.56ms</td></tr>
<tr><td>0x11</td><td>18</td><td>50ms</td></tr>
<tr><td>0x23</td><td>36</td><td>100ms</td></tr>
<tr><td colspan="3">……..</td></tr>
<tr><td>0x3F</td><td>64</td><td>178ms</td></tr>
<tr><td colspan="3">…….</td></tr>
<tr><td>0xFF</td><td>256</td><td>712ms</td></tr>
</table>

- CFG3 Register (0x AB)

<table>
<tr><th colspan="2">Addr: 0xAB</th><th colspan="3">CFG8</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th>Bit Description</th></tr>
<tr><td>7</td><td>INTRD_CLEAR</td><td>0</td><td>RW</td><td>Status Reset Flag
If set, then flag bits in the STATUS register will be reset whenever the STATUS register is read over I2C.
INTRD_CLR = 1, All flag bits of the STATUS register are reset.
INTRD_CLR = 0, IDLE.</td></tr>
<tr><td>6:5</td><td>Reserved</td><td>00</td><td>--</td><td>Reserved.</td></tr>
<tr><td rowspan="6">4</td><td rowspan="6">SAI</td><td rowspan="6">0</td><td rowspan="6">RW</td><td>Sleep After Interrupt Enable Flag
The Sleep After Interrupt bit is used to place the device into a low power mode upon an interrupt pin assertion.</td></tr>
<tr><td>
<table>
<tr><th>PON</th><th>SAI</th><th>INT</th><th>Oscillator</th></tr>
<tr><td>0</td><td>X</td><td>X</td><td>OFF</td></tr>
<tr><td>1</td><td>0</td><td>X</td><td>ON</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>ON</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>OFF</td></tr>
</table>
</td></tr>
<tr><td>3:0</td><td>Reserved</td><td>0001</td><td>--</td><td>Reserved. Must be set to default value.</td></tr>
</table>

- CFG6 Register (Address 0xAE)

Addr: 0xAE		CFG6		
Bit	Bit Name	Default	Access	Bit Description
7	AGC	0	RW	**Auto Gain Control Enable Flag**
6	APC_DISABLE	0	RW	**Proximity Automatic Pulse Control (APC) Disable Flag** APC_DISABLE = 0, APC is enabled. APC_DISABLE = 1, APC is disabled.
5:0	Reserved	111111	--	Reserved. **Must be set to default value.**

- POFFSETL Register (Address 0xC0)

Addr: 0xC0		POFFSETL		
Bit	Bit Name	Default	Access	Bit Description
7:0	POFFSETL	0x00	RW	**Proximity Crosstalk Offset Low Byte** This register contains the low byte of the signed proximity offset adjust value.

- POFFSETH Register (Address 0xC1)

Addr: 0xC1		POFFSETH		
Bit	Bit Name	Default	Access	Bit Description
7:5	Reserved	000	--	Reserved.
4:0	POFFSETH	00000	RW	**Proximity Crosstalk Offset High Byte** This register contains the high byte of the signed proximity offset adjust value.

■ CALIB Register (Address 0xD7)

Addr: 0xD7		CALIB		
Bit	Bit Name	Default	Access	Bit Description
7	CALAVG	0	RW	**Calibration Average Enable Flag** Enables proximity hardware averaging as selected with PROX_AVG during calibration. CALAVG = 0, No hardware averaging CALAVG = 1, Hardware averaging enabled
6:5	Reserved	00	--	Reserved.
4	CALPRATE	0	RW	**Calibration PRATE Enable Flag** Enables PRATE during calibration. Useful when averaging is enabled. CALPRATE = 0, PRATE ignored CALPRATE = 1, PRATE applied between averaging samples
3:1	Reserved	000	--	Reserved.
0	START_OFFSET_CAL	0	RW	**Calibration Start Flag** Calibration sequence start. START_OFFSET_CAL = 1, Calibration start. START_OFFSET_CAL = 0, IDLE.

■ CALIB_OFFSET Register (Address 0xD8)

Addr: 0xD8		CALIB_OFFSET		
Bit	Bit Name	Default	Access	Bit Description
7:6	Reserved	00	--	Reserved.
5	EN_RANGE_EXTENSION	0	RW	**Offset Range Extension Enable Flag** Setting this bit to a 1 enables the proximity offset range extension functionality. See the OFFSET_RANGE_EXTENSION bits. EN_RANGE_EXTENSION = 0, Offset range extension is disabled. EN_RANGE_EXTENSION = 1, Offset range extension is enabled.

4:0	OFFSET_RANGE_EXTENSION	00000	RW	**Offset Range Selection Flag** Offset range extension selection.

■ CALIBCFG Register (Address 0xD9)

Addr: 0xD9		CALIBCFG			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:5	BINSRCH_TARGET	010	RW	**Proximity Offset Calibration Target**	
				Value	PDATA Target
				(000)0	3
				(001)1	7
				(010)2	15
				(011)3	31
				(100)4	63
				(101)5	127
				(110)6	255
				(111)7	511
4	Reserved	1	--	Reserved.; **Static value 1**	
3	AT_OFS_ADJ	0	RW	**Auto Offset Adjustment** If set, this bit causes the value in POFFSETL/H register to be decremented if PDATA ever becomes zero.	
2:0	PROX_AVG	000	RW	**PS Hardware Average Number** PROX_AVG defines the number of ADC samples collected and hardware averaged during a proximity cycle.	
				Value	Averaging Samples
				(000)0	Disable
				(001)1	2
				(010)2	4
				(011)3	8
				(100)4	16

■ CALIBSTAT Register (Address 0xDC)

Addr: 0xDC		CALIBSTAT		
Bit	Bit Name	Default	Access	Bit Description
7:3	Reserved	00000	--	Reserved.
2	OFFSET_ ADJUSTE D	0	RW	Bit is set when the proximity offset has been automatically decremented if AUTO_OFFSET_ADJ = 1 (see CALIBCFG register). This bit can be cleared by writing 1 to it or setting AUTO_OFFSET_ADJ to 0.
1	Reserved	0	--	Reserved.
0	CALIB_FINISH ED	0	RW	This flag indicates that calibration has finished. This bit is a copy of the CINT bit in the STATUS register. It will be cleared when the CINT bit is cleared.

■ INTENAB Register (Address 0xDD)

Addr: 0xDD		INTENAB		
Bit	Bit Name	Default	Access	Bit Description
7	ASIEN	0	RW	ALS Saturation Interrupt Enable Flag
6	PSIEN	0	RW	PS Saturation Interrupt Enable Flag
5	PIEN	0	RW	PS Interrupt Enable Flag
4	AIEN	0	RW	ALS Interrupt Enable Flag
3	CIEN	0	RW	Calibration Interrupt Enable Flag
2	ZIEN	0	RW	Zero detect Interrupt Enable Flag
1:0	Reserved	00	--	Reserved.

■ AS_CFG Register (Address 0xF5)

Addr: 0xF5		AS_CFG				
Bit	Bit Name	Default	Access	Bit Description		
7:2	Reserved	000110	--	**Must be written as 000100.**		
1:0	CITGTIME	00	RW	ALS Integration Time Value		
				CITGTIME	Integration Cycle	Integration Time(us)
				0	8/8	2774
				1	Reserved	Reserved

				2	1/8	344
				3	1/64	44

The CFG1 Register bit4 to bit0 set as"01000", if CITGTIME[1:0]=0, AGAIN=128X, else if CITGTIME[1:0]=2, AGAIN=16X, else CITGTIME[1:0]=3, AGAIN=2X

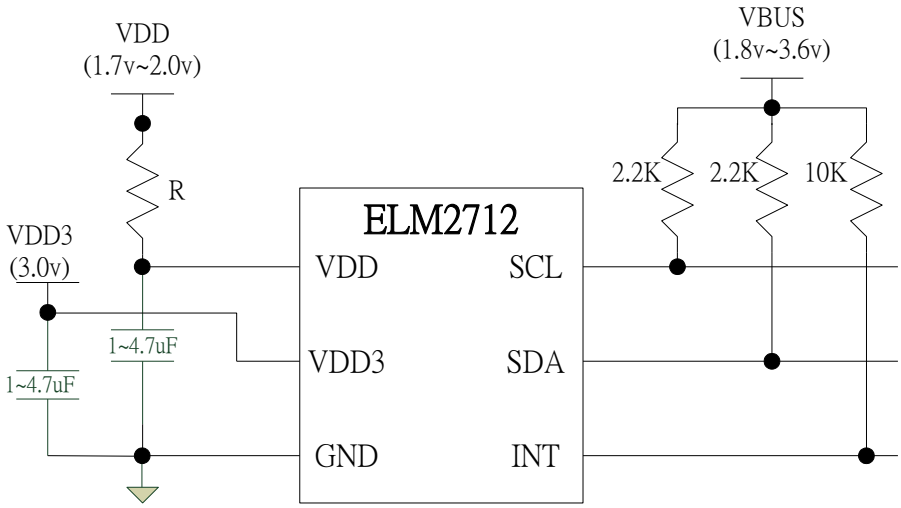
- PSDA Register (Address 0xF6)

Addr: 0xF6		PSDA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	RS1,RS0	01	RW	Full range PS offset Setting 00 lowest
5:0	PSDA	100000	RW	PS Offset Calibration DA Selection Flag

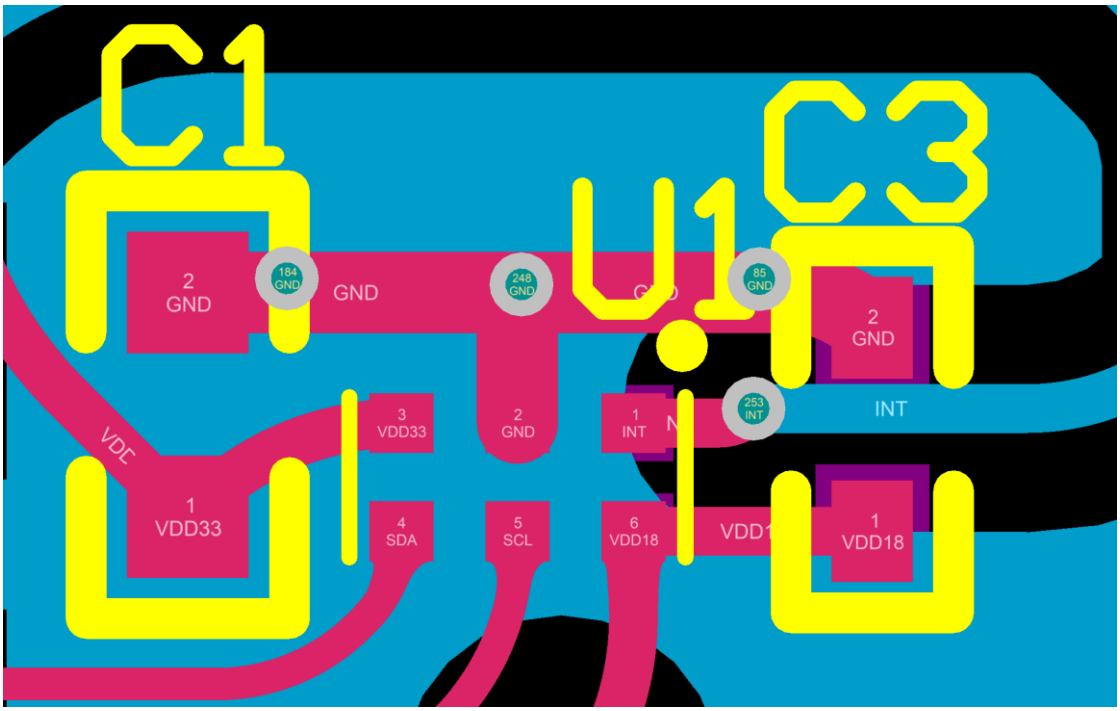
- AGC_GAIN_HYST Register (Address 0xF7)

Addr: 0xF7		AGC_GAIN_HYST			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:4	Reserved	0000	--	Reserved.	
3:2	AGCHTHR	10	RW	**Auto Gain Control High Threshold Value**	
				Value	Threshold Value
				(00)0	0x7FFF
				(01)1	0x9FFF
				(10)2	0xBFFF
				(11)3	0xDFFF
1:0	AGCLTHR	01	RW	**Auto Gain Control Low Threshold Value**	
				Value	Threshold Value
				(00)0	0x0FFF
				(01)1	0x1FFF
				(10)2	0x3FFF
				(11)3	0x5FFF

Application Note

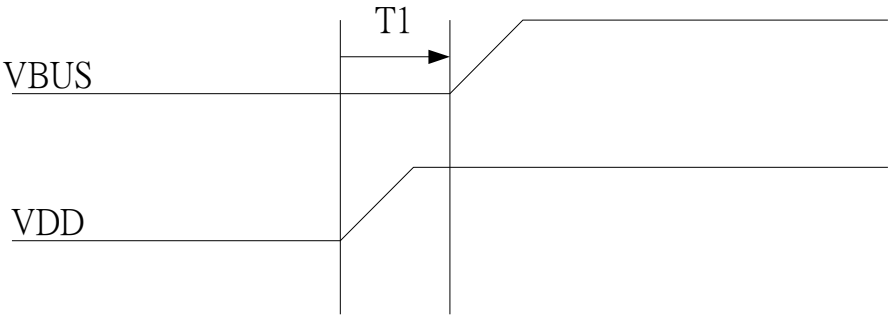


Note: The recommended R value is 22 ohm



Recommended Circuit Layout

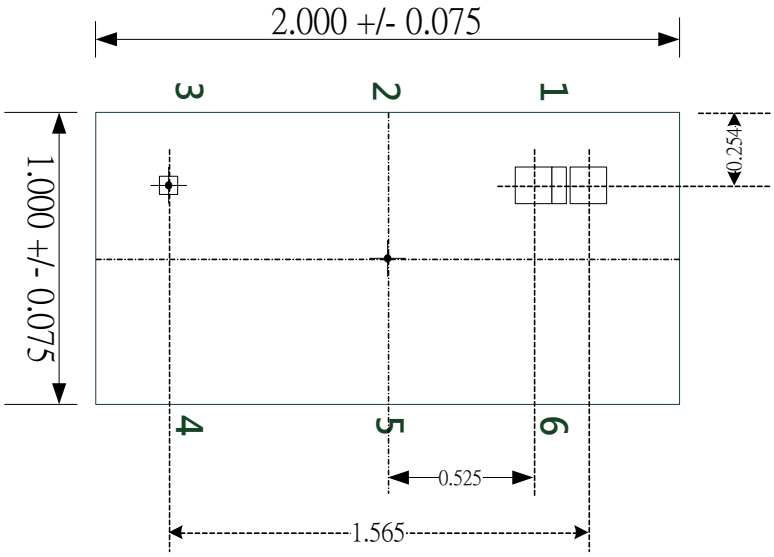
- Power on Sequence



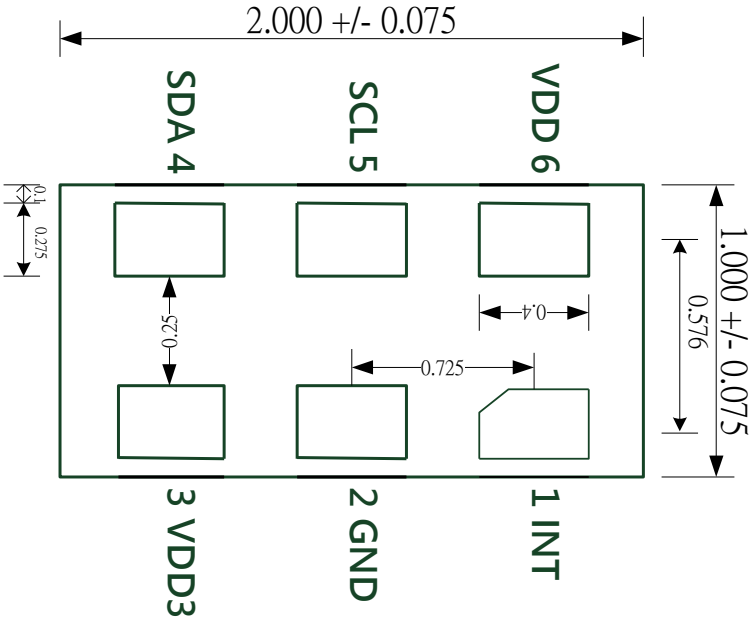
Note: The T1 time is recommended more than 30ms (VDD first is recommended)

Package

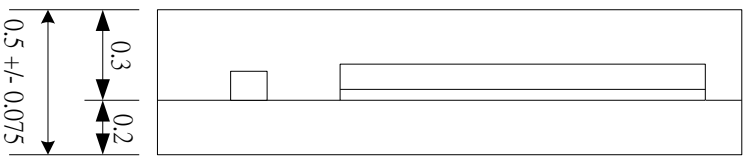
- Top View



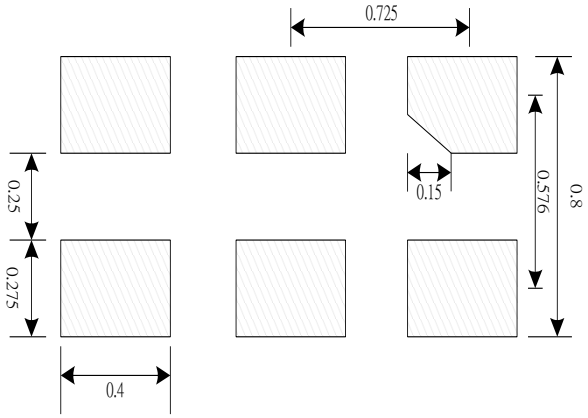
- Bottom View



- Side View

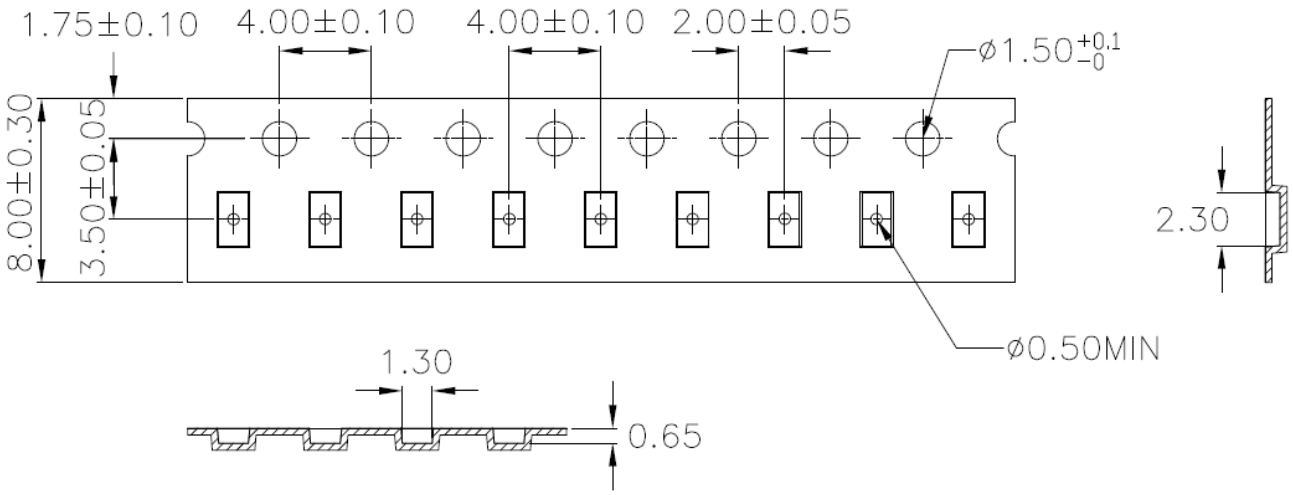


- Recommended PCB Layout

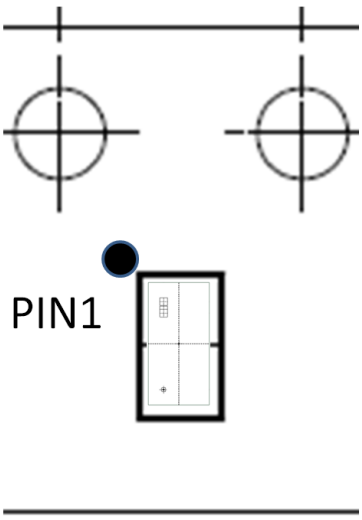


Note: all dimensions are in mm

Tape and Reel Information



Chip in Reel



Note: all dimensions are in mm

Order & Packing Information

Package	Product ID	Packing
OPLGA 2x1x0.5mm	ELM2712BGP06NDR	Tape & Reel 3K pcs

GP06: OPLGA 2x1x0.5mm 6PIN

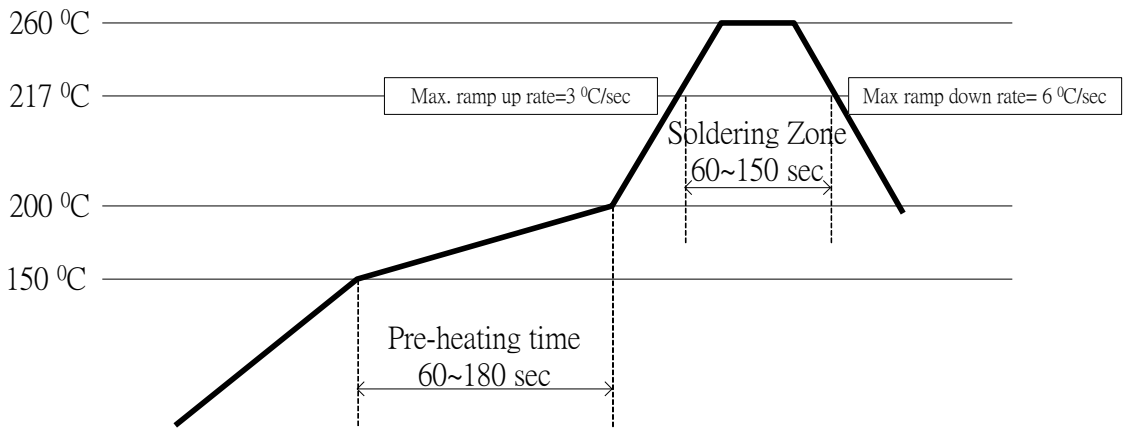
N: RoHS & Halogen free

D:-30~85℃

R:Tape & Reel

Soldering Information

- Soldering condition



Note [1]: Reflow soldering should not be done more than three times

Note [2]: When soldering, do not stress on IC during heating

Note [3]: After soldering, do not warp the board

Recommended of storage method and ESD precaution

Dry box storage is recommended as soon as the aluminum bag has been opened. It could prevent moisture absorption.
The following conditions should be followed if dry boxes are not available

-- Storage temperature 10C to 30C
-- Storage humidity <= 60% RH max

After more than 72 hours Under the conditions moisture content will be too high for reflow soldering. In case of moisture absorption, the devices will recover to former conditions by drying under the following condition

-- 192 hours at 40C and 5% RH or
-- 96 hours at 60C and < 5% RH for device containers, or
-- 24 hours at 125C is not suitable for reel

ESD precaution
-- When the Chips are removed from Anti-static bag, please follow the handing procedure to prevent ESD damage