Multi Frequency Contactless Identification Device

Anti-Collision compatible with BTG's Supertag Category Protocols

Description

The EM4022 (previously named P4022) chip implements patented anti-collision protocols for both *high* frequency and *low* frequency applications. It is even possible to identify transponders with identical codes, thereby making it possible to count identical items. The chip is typically used in "passive" transponder applications, i.e. it does not require a battery power source. Instead, it is powered up by an electromagnetic energy field or beam transmitted by the reader, which is received and rectified to generate a supply voltage for the chip. A pre-programmed code is transmitted to the reader by varying the amount of energy that is reflected back to the reader. This is done by modulating an antenna or coil, thereby effectively varying the load seen by the reader.

Typical Applications

- Access control
- Animal tagging
- Asset control
- Sports event timing
- Licensing
- Electronic keys
- Auto-tolling

Features

- Implements all BTG anti-collision protocols: Fast SWITCH-OFF, SLOW-DOWN, and FREE-RUNNING
- Can be used to implement low frequency inductive coupled transponders, high frequency RF coupled transponders or bi-frequency transponders
- Reading 500 transponders in less than one second for high frequency applications
- Factory programmed 64 bit ID number
- Data rate options form 4 kbit/s to 64 kbit/s
- Manchester data encoding
- Any field frequency: Typically 125 kHz, 13.56 MHz inductive and 100 MHz to 2.54 GHz RF
- Data transmission done by amplitude modulation
- Trimmed 110 pF ± 3% on-chip resonant capacitor
- On-chip oscillator, rectifier and voltage limiter
- Low power consumption
- Low voltage operation : down to 1.5 V at ambient temperature
- -40 to +85 °C operating temperature range

Pin Assignment

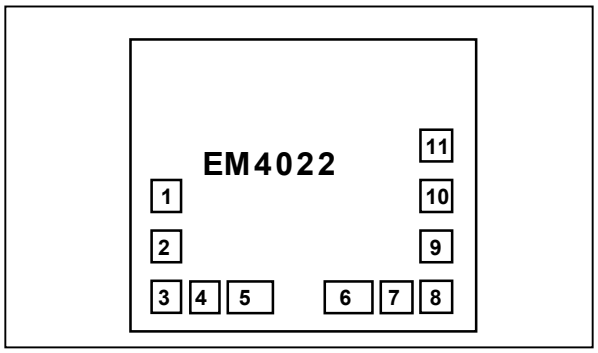

Fig. 1

Pad N°	Name	Function
1	XCLK	external test clock input
2	V_{DD}	positive supply
3	M	connection to antenna
4	M_{TST}	test output
5	COIL1	Coil terminal 1
6	COIL2	Coil terminal 2
7	V_{SSTST}	negative test supply output
8	V_{SS}	negative supply
9	GAP	GAP input
10	SI	Serial test data input (pull down)
11	TMC	Test mode control (pull down)

Typical Operating Configurations

Low frequency inductive transponder .

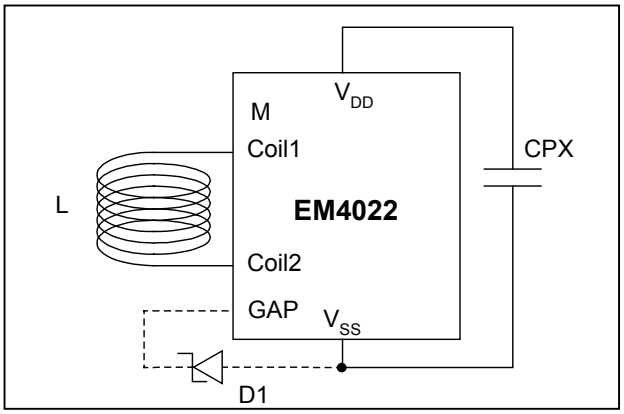

Fig. 2

Low frequency applications are those applications that can make use of the on-chip full wave rectifier bridge to rectify the incident energy. These are typically applications that use inductive coupling to transmit energy to the chip. The carrier frequency is typically less than 500 kHz. The design of the on-chip rectifier and resonance capacitor is optimized for frequencies in the order of 125 kHz. Low frequency transponders can be implemented using just a EM4022 chip and an external coil that resonates with the on-chip tuning capacitor at the required carrier frequency. An external power storage capacitor is required to maintain the supply voltage above the integrated power on reset level.
In a very strong field, due to the forward resistance of the diode, the GAP input must be limited at V_{SS}-0.3V by a schottky diode (D1)

Medium frequency (13.56 MHz) inductive transponder implementation

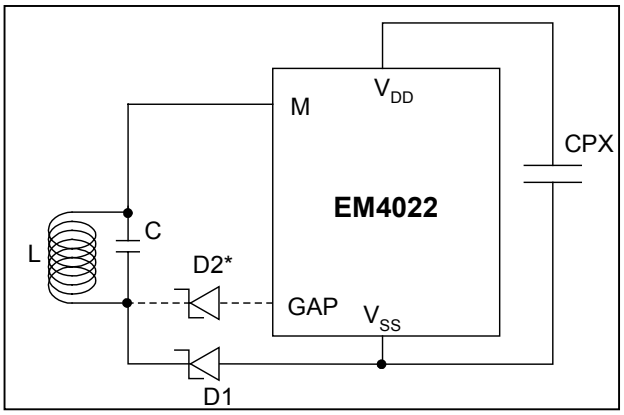

Fig. 3

L: coil antenna (typical value 1.35 µH).
C: tuning capacitor (typical value 100 pF)

Medium frequency applications are those which cannot use the integrated full wave rectifier and where the transponder power is transmitted through a coil. External microwave schottky diodes are required to rectify the carrier wave. An external power storage capacitor can be added to improve reading range.
These applications allow higher data rates (64 kbit/s). Where reading rates of 500 transponders per second can be achieved

High frequency RF transponder implementation.

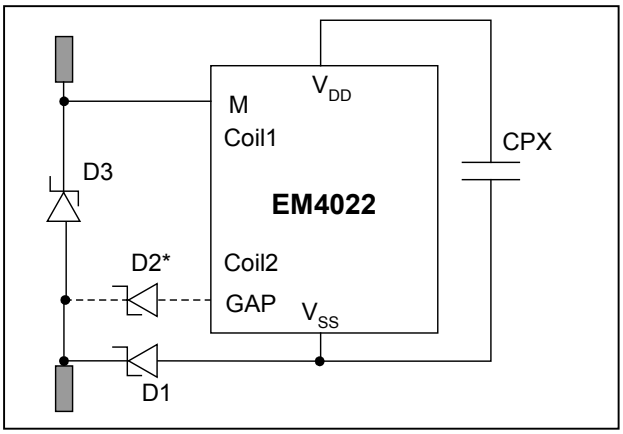

Fig. 4

D2 in figure 2 and 3 is optional and is only used for GAP enable versions. All diodes are schottky type.

High frequency applications are similar to medium frequency applications. These are typically applications that use electromagnetic RF coupling to transmit energy to the chip using carrier frequencies greater than 100 MHz. High frequency transponders can be implemented using a EM4022 chip, two or three microwave diodes and a printed antenna. High frequency RF coupled applications typically have higher reading distances (> 4 m) and

Bi-frequency applications are possible by implementing a coil between coil1 and coil2 connections in the high frequency application (fig. 4).

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum AC peak current induced on COIL1 and COIL2	I_{COIL}	± 30 mA
Maximum DC voltage induced between M and V_{SS}	V_M (note1)	5 V
Maximum DC current supplied into M	I_M (note1)	60 mA
Power supply	V_{DD} - V_{SS}	-0.3 to V_M
Max. voltage other pads	V_{max}	V_{DD} + 0.3 V
Min. voltage other pads	V_{max}	V_{SS} - 0.3 V
Storage temperature	T_{STORE}	-55 to +125°C
Electrostatic discharge maximum to MIL-STD-883C method 3015	V_{ESD}	1000 V

note1) whatever is reached first

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, due to the unique properties of this device, anti-static precautions should be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all the terminal voltages are kept within the supply voltage range.

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Operating temperature	T_A	-40		+85	°C
Maximum coil current	I_{COIL}	-10		10	mA
AC voltage on coil*	V_{COIL}			15	V_{pp}
DC voltage on M*	V_M		3.5		V

* The AC voltage on the coil and the DC voltage at pad M are limited by the on-chip shunt regulator loaded at I_{COIL} in table 3

Electrical Characteristics

V_{SUPPLY} between 2.0 V and 3.0 V, T_A = 25 °C, unless otherwise specified.

Parameter	Symbol	Test conditions	Min	Typ	Max	Units
Supply voltage (V_{DD} - V_{SS})	V_{SUPPLY}		V_{PONR} +100mV		V_M	V
Regulated voltage	V_M	I_M = 50 mA	3.3	4	4.7	V
Oscillator frequency	F_{OSC}	V_{SUPPLY} = 3 V	92	125	160	kHz
Power-on reset threshold	V_{PONR}	V_{SUPPLY} rising	0.9	1.4	1.8	V
Power-on reset threshold	V_{PONF}	V_{SUPPLY} falling	0.7	1.2	1.6	V
Power-on reset hysteresis	V_{PHYS}		80	160	240	mV
GAP input time constant	T_{GAP}	Extrapolated with an external capacitor of 64nF		0.4		µs
Modulation transistor ON resistance	R_{ON}	V_{SUPPLY} = 3 V		4	8	Ω
Resonance capacitor	C_R	f = 100KHz, 100mVpp	106.7	110	113.3	pF
Supply capacitor	C_{SUP}	f = 100KHz, 100mVpp		140		pF
Current consumption in modulation state	I_{MOD}	V_{SUPPLY} = 2 V	6	9	13	µA
Shunt Regulator current consumption	I_{SHUNT}	V_{SUPPLY} = 2V		200	500	nA
Gap pull-up current consumption	I_{GAP}	V_{GAP} = 0V, V_{SUPPLY} = 2V	1.8	5	7	µA
Dynamic current consumption	I_{DYN}	f_{OSC} = 128KHz, V_{SUPPLY} = 2V	3.5	5	6.5	µA

Timing Characteristics

1) All timings are derived from the on-chip oscillator.
2) The minimum *low frequency* GAP width for a single chip is 1 bit at its own clock frequency. The reader must however allow for the spread in clock frequencies possible in a group of tags. Therefore the minimum width of the GAP in MUTE and WAKE-UP signals must be 1.5 bits. High frequency GAPs can be arbitrarily.
3) The maximum GAP width for a single chip is 6 bits at its own clock frequency. The reader must however allow for the spread in clock frequencies possible in a group of tags. Therefore the maximum width of the GAP in MUTE and WAKE-UP signals must be 5 bits.

Parameter	Symbol	Test conditions	Min	Typ	Max	Units
High frequency GAP width	T_{HFGAP}		50			ns
High frequency ACK GAP width	W_{HFACK}				6	bit
High frequency MUTE and WAKE-UP GAP width	W_{HFMUTE}				5	bit
Low frequency ACK GAP width	W_{LFGAP}		1.0	2	6	bit
Low frequency MUTE and WAKE-UP GAP width	W_{LFACK}		1.5	2	5	bit
GAP separation in WAKE-UP signal	W_{LFMUTE}		1.5	2	5	bit

Power storage capacitor calculation

The global current consumption of the device defines the external storage capacitor.
When the device modulate, the supply voltage is picked from the supply capacitor and should never decrease under the falling edge of the power on reset (V_{PONF}). If this occurs, the device goes in a reset mode and any data transmission is aborted. The worst case for the storage capacitor calculation is when the device is put in the electromagnetic field. At this moment the supply reaches the V_{PONR} and start to modulate. During modulation the power store in the capacitor must be high enough so that at the end of the modulation the supply is higher than $V_{PORF.}$. This means that the voltage reduction on the capacitor must be less than the hysteresis of the power on reset (V_{PHYS}).
And this when the chip has a supply voltage of around the power on reset threshold
The total current consumption from the storage capacitor is defined by the modulation current I_{MOD},
This current is the consumption of the power on reset block, oscillator and the logic which work at a typical frequency of 125KHz. The GAP current is also included in this parameter.
The duration where this currents is present for the capacitor calculation, is dependent of the data rate

Calculation example :
Below we define typical cases combinations :
F_{OSC} = 125 KHz
V_{PHYS} = 120 mV
I_{MOD} = 9 µA
Data rate is 4 KBaud.

$$CPx = \frac{I_{MOD} * 128 * 10^3}{F_{OSC} * V_{HYS} * BaudRate}$$
$$= \frac{9 * 10^{-6} * 128 * 10^3}{125 * 10^3 * 160 * 10^{-3} * 4 * 10^3} = 14.4nF$$

Of course, this value can be adapted to the electromagnetic power and to the performances that must be achieved. If a tag is put in a field within a short time, the emitting power must be high enough to charge up the capacitor.
The chip integrates a 140pF supply capacitor.

Block Diagram

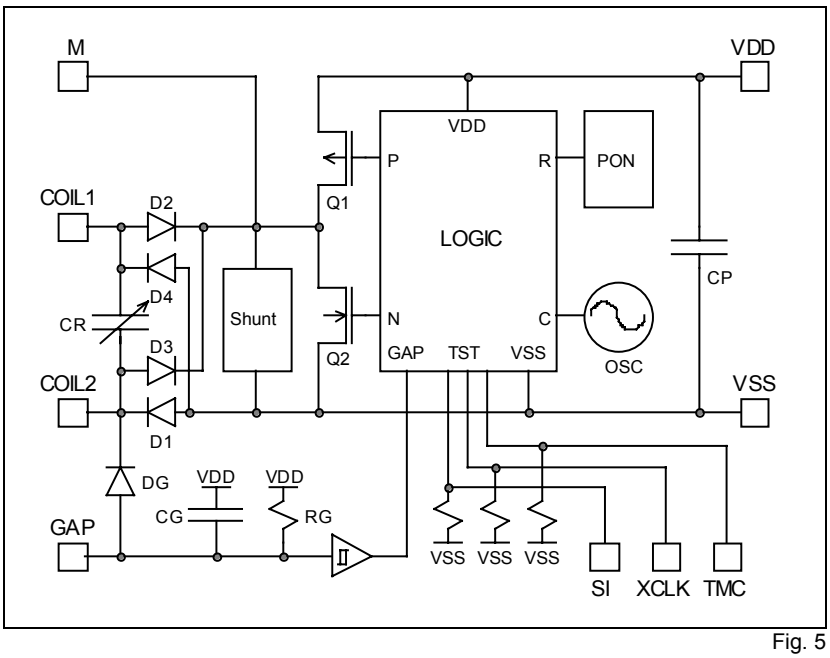

Fig. 5

Functional description

Resonance capacitor

The resonance capacitor CR has a nominal value of 110 pF and is trimmed to achieving a high stability over the whole production. For resonance at 125 kHz an external 14.7 mH coil is required. At 13.65 MHz the required coil inductance drops to 1.2 µH.

Rectifier bridge

Diodes D1-D4 form a full wave rectifier bridge. They have relatively large forward resistances (100 -200 Ω). This is sufficient at 125 kHz, where the output impedance of the tuned circuit is high, but at 13.5 MHz the diode resistance becomes significant and external diodes have to be used to bypass the internal ones. The diode resistance affects the rate at which the power capacitor CP can be charged. It also affects the modulation depth that can be achieved.

Shunt regulator

The shunt regulator has two functions. It limits the voltage across the logic and in high frequency applications it limits the voltage across the external microwave Schottky diodes, which typically have reverse breakdown voltages of 5 V.

Oscillator

The on-chip RC oscillator has a center frequency of 128 kHz. It gives the main clock of the logic and defines the effective data/rate.

Power-on reset (PON)

The reset signal keeps the logic in reset when the supply voltage is lower than the threshold voltage. This prevents incorrect operation and spurious transmissions when the supply voltage is too low for the oscillator and logic to work properly. It also ensures that transistor Q2 is off and transistor Q1 is on during power-up to ensure that the chip starts up.

Modulation transistor

The N channel transistor Q2 is used to modulate the transponder coil or antenna. When it is turned on it loads the antenna or coil, thereby changing the load seen by the reader antenna or coil, and effectively changing the amount of energy that is reflected to the reader. Its low on resistance is especially designed for high frequency applications.

Charge preservation transistor

The P channel transistor Q1 is turned off whenever the modulation transistor Q2 is turned on to prevent Q2 from discharging the power storage capacitor. This is done in a non-overlapping manner, i.e. Q1 is first turned off before Q2 is turned on, and Q2 is turned off before Q1 is turned on.

Gap detection

Poly-silicon diode DG is used to detect a gap in the illuminating field. It is a minimum sized diode with forward resistance in the order of 2 kΩ. The low pass filter shown diagrammatically as CG and RG actually consists of a pull-up transistor (approximately 100 kΩ) in conjunction with the parasitic capacitance of the GAP input pad (approximately 2.5 pF).
Through the diode the GAP input will be pulled low during each negative going cycle of the carrier. When the carrier is switched off, the GAP input will be pulled high by the pull-up transistor.
At very high carrier frequencies (> 100 MHz) the carrier will be filtered out, so that the GAP input will be low continuously when the carrier is present. When the carrier disappears, the GAP input will go high with the time constant of the low pass filter. At very low frequencies the GAP input will go high and low at each cycle of the carrier, and will stay high when the carrier disappears. To detect the gap, the logic must check for a high period longer than the maximum high period of the carrier.
As the rise and fall times of the GAP can be slow, a Schmitt trigger is used to buffer the GAP input.

LOGIC block

Depending on the state of the SI input at power-up, the EM4022 either enters a test mode (SI = 1) or its normal operating mode (SI = 0). The SI pin is internally pulled down, so that it can be left open for normal operation.

After the power-on reset has disappeared, the chip boots by reading the SEED and CTL ROMs.
The chip then enters its normal operating mode, which basically consists of clocking a 16 bit timer counter with the bit rate clock until it compares with the number in the random number generator. At this point a code (which is stored in the ID ROM) is transmitted with the correct preamble at the correct data rate and encoded correctly. The random number generator is clocked to generate a new pseudo random number, and the 16 bit counter is reset to start a new delay.
The width of the comparison between the 16 bit random number and the 16 bit delay count determines the maximum possible delay between transmissions (repetition rate). Any one of eight maximum delay settings can be pre-programmed.
The basic free-running mode as described above can be modified by the reception of GAP (MUTE and ACK) signals, if these are enabled by the CTL bits.
If an ACK signal is received after transmission of a code, the chip either turns itself off completely or reduces the rate at which the delay counter is clocked, thereby slowing down the rate at which codes are transmitted.
If a MUTE signal is received while the chip is not transmitting, the current operation of the chip is interrupted for 128 clock periods, after which it continues normally. Reception of more MUTEs during the sleep state restarts the sleep state. The sleep state is also terminated by the reception of a WAKE-UP signal (an ACK signal to a chip which has just completed transmitting).

ACK timing diagram

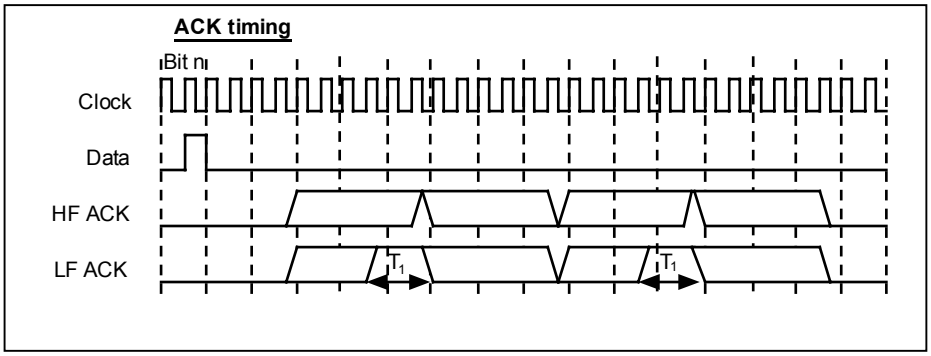

Fig. 6

GAP Detection Algorithm

The GAP detection logic contains two main controllers, one for detecting the ACK signal, and one for detecting the MUTE and WAKE-UP signals. The WAKE-UP signal is also called an asynchronous ACK, as it is really an ACK meant for another chip. It also contains a pre-processor for low frequency GAP signals.

Refer to the timing diagrams in Figure 6 and 7 for the following detailed description of the GAP detection algorithms.

ACK

The controller checks for a LOW 1.75 bit periods after the last bit of code has been transmitted. It then checks for a HIGH 3 bits later, a LOW 3 bits later and finally a HIGH a further 3 bits later.

The reader should synchronise itself to the frequency of the received code, check the CRC and then send two GAPs so that the above pattern is matched. Ideally to achieve the lowest error rate, the GAPS should be as narrow as possible and situated 4.75 and 7.75 bits after the last bit of code.

In practice allowance must be made for the fact that the on-chip oscillator can drift in the time between when the last code bit is transmitted and when the GAPs are expected. One reason for the drift is that the oscillator is supply voltage dependent, and the supply voltage will typically be rising during this time, since the transponder will not be modulating its coil or antenna.

The slope of the rising and falling edges of the GAPs can also be adjusted to reduce reader power bandwidth. In the case of high frequency GAPs the envelope is used directly. Low frequency GAPs have to be pre-processed. They are detected by checking for high periods lasting longer than one bit period. For this reason there is a set-up time of 1 bit. The minimum GAP width is therefore 1 bit period (T_1 in the timing diagram).

MUTE

The MUTE signal is received asynchronously by the transponder. The controller checks for a HIGH less than 7 bits wide after pre-processing (T_2 in the timing diagram). As in the case of the ACK, low frequency MUTE GAPs must be at least one bit wide (T1 in the timing diagram), but high frequency GAPs can be arbitrarily narrow.

When transmitting a MUTE, the reader must take into account that there could be a spread in the clock frequencies of all the receiving transponders.

The reader should therefor limit the width of a MUTE to be less than 5 bits of the nominal bit rate (T_4 in the timing diagram). A low frequency MUTE should also be wider than 1.5 bits of the nominal bit rate (T_3 in the timing diagram).

The MUTE should be sent as early as possible after a code transmission has been detected, while still making sure that it is a code transmission and not just noise. The earlier the MUTE is sent, the more time the reader has to recover before the SYNCH and code bits arrive, and the smaller the probability that another transponder has started a colliding transmission

MUTE and WAKE-UP timing diagrams

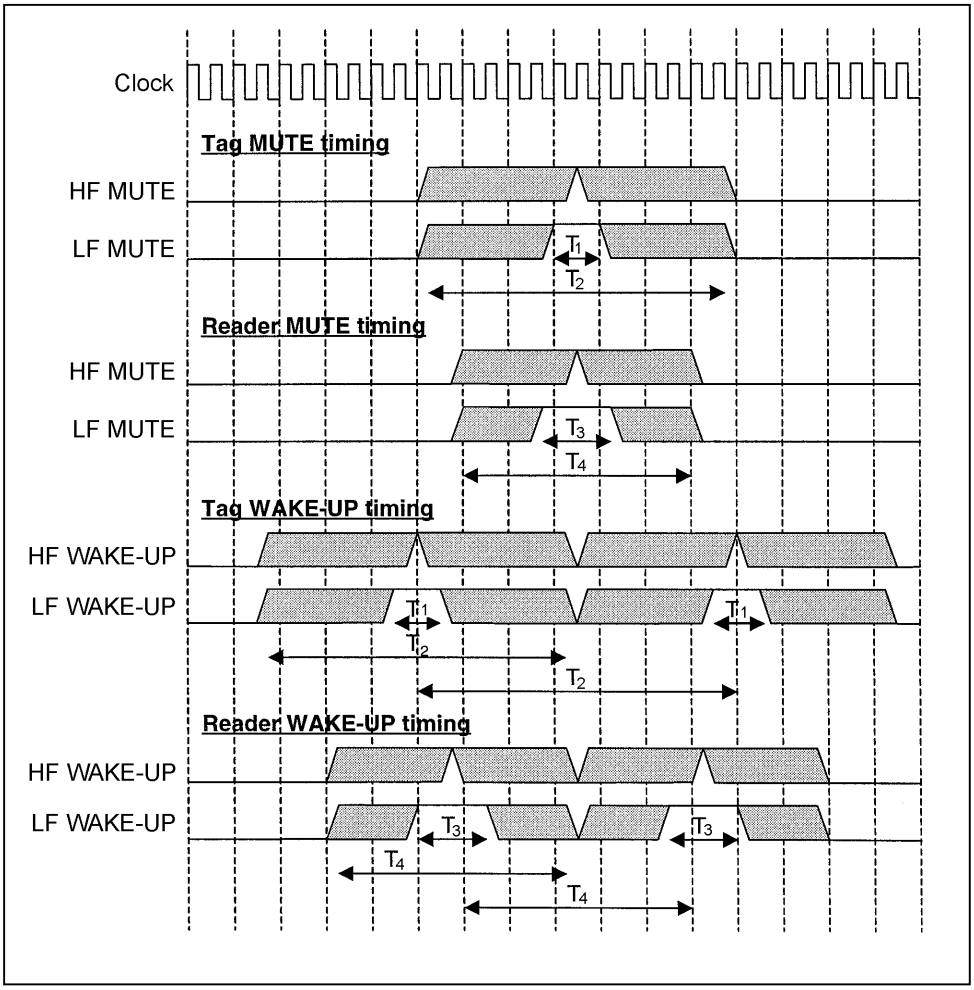

Fig. 7

WAKE-UP

An ACK sent after correct reception of a code is interpreted by the other transponders in the field as a WAKE-UP. The ACK arrives synchronously at the transponder that has just transmitted, but asynchronously at all the other transponders. If necessary, a WAKE-UP can also be sent if the code is not received correctly, ensuring that it will not be interpreted as an ACK by the transmitting transponder. This could speed up the protocol, but runs the risk of turning transponders off by accident.

To detect a WAKE-UP, the chip checks for two GAPs, less than 7 bits apart and each less than seven bits wide. As with the MUTE allowance must made for the spread in clock frequencies. To be safely interpreted as a WAKE-UP, the GAPs should be sent less than 5 bits apart, and each should be less than 5 bits wide.

This has an implication in the case of the high frequency ACK, which could theoretically consist of two very narrow GAPs 6 bits apart. In practice though, the GAPs will be typically at least one bit wide, making the separation five bits.

Like the MUTE, the low frequency ACK GAPs should be at least 1.5 bits wide to serve as a reliable WAKE-UP.

It should be noted that failure to reliably recognise WAKE-UPs is not critical. The protocol might be slowed down marginally, but will still work, as the chips time-out of the sleep mode automatically after 128 bits.

Data Encoder

The transmitted code always consists of an 11 bit preamble followed by the 64 code bits. The preamble consists of 8 start bits (ZEROES), followed by a SYNCH. The SYNCH consists of a LOW for two bit periods followed by a ONE.

The EM4022 can be programmed for one of two data encoding methods. The first method is a variation on Manchester II, i.e. a ONE is represented by a HIGH in the first half of a bit period, and a ZERO is represented by a LOW in the first half of a bit period.

The second encoding method is called GLITCH encoding. A ONE is represented by a HIGH in the first quarter of the bit period, while a ZERO is represented by a HIGH in the third quarter of the bit period.

In GLITCH encoding the longest modulation period is one quarter of a bit period, compared to the Manchester encoding, where the longest modulation period is one full bit period. GLITCH encoding therefore requires a much smaller power storage capacitor.

Data Encoding

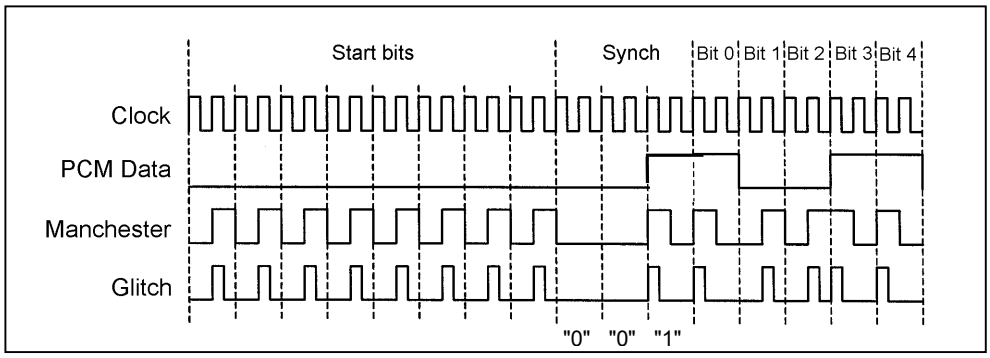

Fig. 8

ROM programming

The EM4022 contains three laser fuse ROM blocks that are pre-programmed by the foundry.

CODE ID ROM

This ROM contains the 64 bit ID code. The foundry will automatically program a unique 48 bit ID and 16 bit CRC. In this case the most significant bit of the ID is programmed into bit 0 of the ROM, which will be transmitted first.

CONTROL ROM

The operational modes of the EM4022 are pre-programmed into the CONTROL ROM. The contents of this one is not read out.

CRC Block Diagram

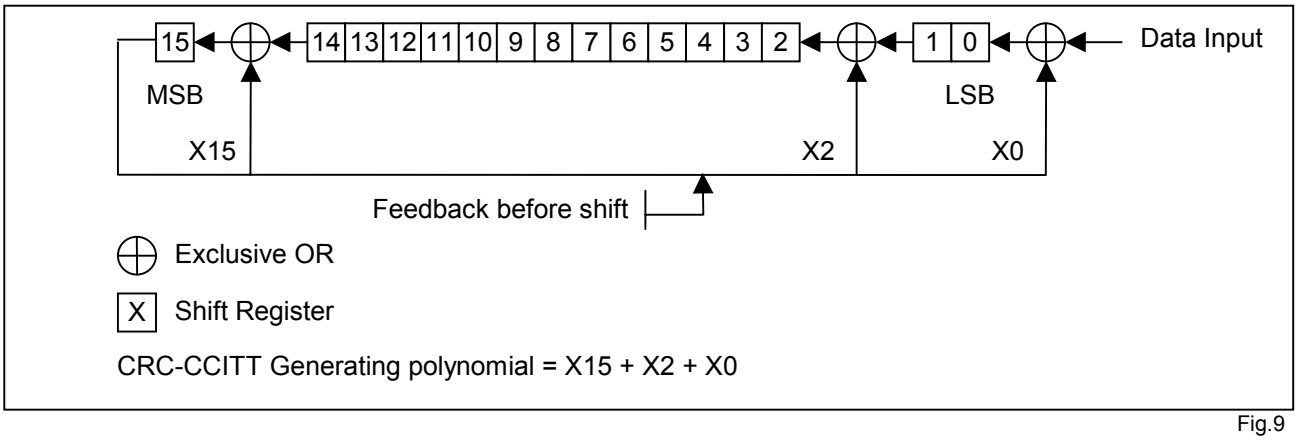

Fig.9

Control ROM Bit definition

Parameter	Value	Mode
Fast / Normal Mode	0 1	Normal Fast
Free-running	0 1	GAP detection enabled GAP disabled (Free-running)
ACK mode	0 1	Slow-down Switch-off
Maximum initial random delay	0 1 2 3 4 5 6 7	0 (Continuous) 16 bits 64 bits 256 bits 1 kbits 4 kbits 16 kbits 64 kbits
Data rate	0 1 2 3 4 5 6 7	64 kbit/s 32 kbit/s 16 kbit/s 8 kbit/s 4 kbit/s 2 kbit/s 1 kbit/s 0.5 kbit/s
Encoding method	0 1	Glitch encoding Manchester encoding
GAP type	0 1	Low frequency GAP detection High frequency GAP detection

Anti-collision Protocol Overview

The protocols are a collection of simple but fast and reliable anti-collision protocols. They allow fast reading of large numbers of transponders simultaneously using a single reader. It is even possible to identify transponders with identical codes, thereby making it possible to count identical items.

Free-running protocol

The basis of the BTG-Supertag series of protocols is that transponders transmit their own codes at random times to a reader. By just listening and recording unique codes when they are received, the reader can eventually detect every tag. The reader detects collisions by typically checking a CRC.

This basic protocol is known as the “Free-running” protocol. It requires uniquely coded tags. Its main advantage is that the reader design is simple, and the spectrum requirement is much less – a very narrow band is required.
Figure 10 shows a sequence of three transponders. The reader starts first to read transponder 1 but during his data transmission, transponder 3 starts to modulate. In this case, due to the CRC check no transponder is detected. A transponder is taken into account, if it transmits a complete data stream without any disturbance

Control ROM Map

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Byte[1]								Byte[0]							
					HF GAP	Man-chester	Data rate			Random delay			Switch-off	Free-running	Fast

Free running example

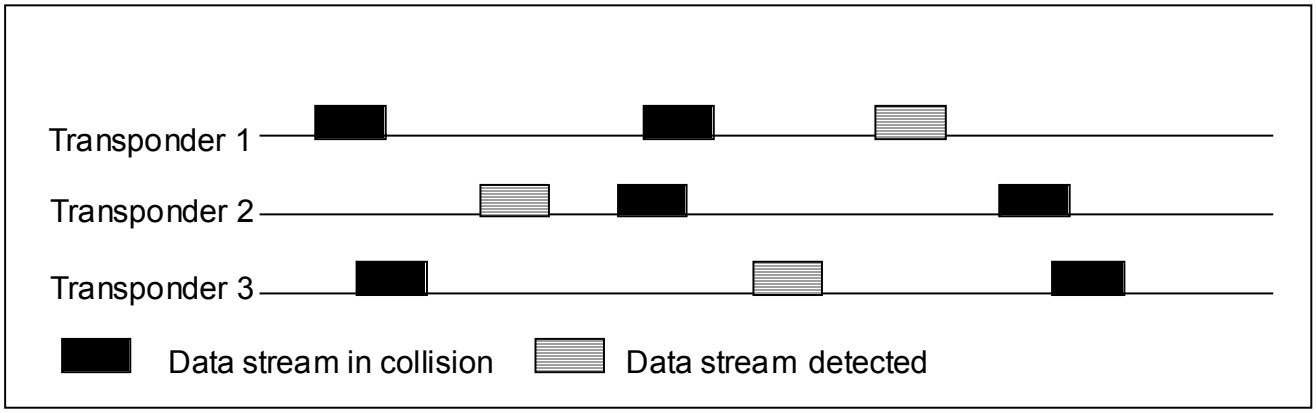

Fig. 10

Bi-directional protocols
Allowing bi-directional communication between reader and transponders can speed up the basic free-running protocol. Communication from the reader to transponders is achieved by turning the illuminating energy field off for short periods. The transponders detect these gaps in the energy transmission and interpret them as required.

Switch-off and Slow-down Modes
Reducing the effective population of transmitting transponders in the reader field can speed up the free-running protocol. One method to achieve this is by either switching transponders off or slowing them down once they have been detected. To achieve this, the reader sends an ACK signal to a transponder after its code has been successfully received. The transponder then either switches off completely or reduces its repeat rate until it is powered down. This reduces the number of collisions between transponder transmissions, thereby reducing the time required to read a group of tags.
Figure 11 shows a typical situation where a collision occurs between transponder 1 and 3. Then, as soon as transponder 2 is read, the reader sends an ACK signal to this one switching it off as long hi is powered up from the field. This eliminates the collision between transponder 1 and 2 in the next step The Switch-off protocol's main advantage is that identical transponders can be counted.

In the EM4022 the ACK signal is implemented as two consecutive *gaps* with the appropriate timing and received at a specific time after a code has been transmitted.
The slow-down mode is a compromise between the free-running mode and the switch-off mode. Etch time a transponder is read, the reader send an ACK to double the random repetition rate. This reduces the collisions and in the time increases the saturation level.
Figure 12 show a typical case of this mode of operation.

Fast Mode
A second method of speeding up the reading of tags, is to inhibit other transponders from transmitting while one transponder is transmitting. This is done by sending a MUTE signal to all of the transponders when the start of a transmission is detected. The transponders stay muted long enough (128 bit of its own clock) to allow the transmission of one code (see figure 13). This allows the transponder that has started transmitting to complete its transmission without any collisions. The other transponders continue with their own protocols automatically after a time out, or continue immediately upon detection of an ACK signal indicating that the transmission that caused the MUTE has been completed.
In the EM4022 the MUTE signal is implemented as a single *gap* received while the transponder is not transmitting.

Switch-off example

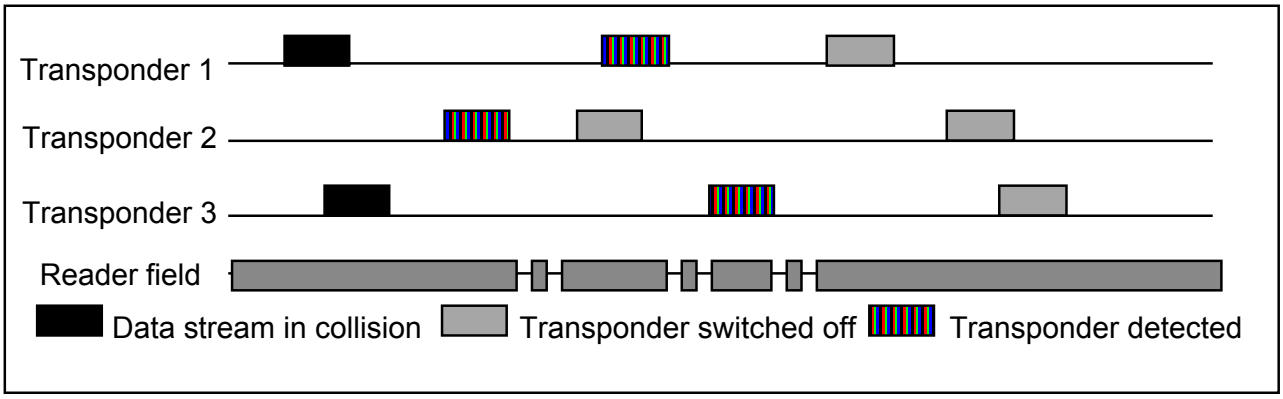

Fig. 11

Slow-down example

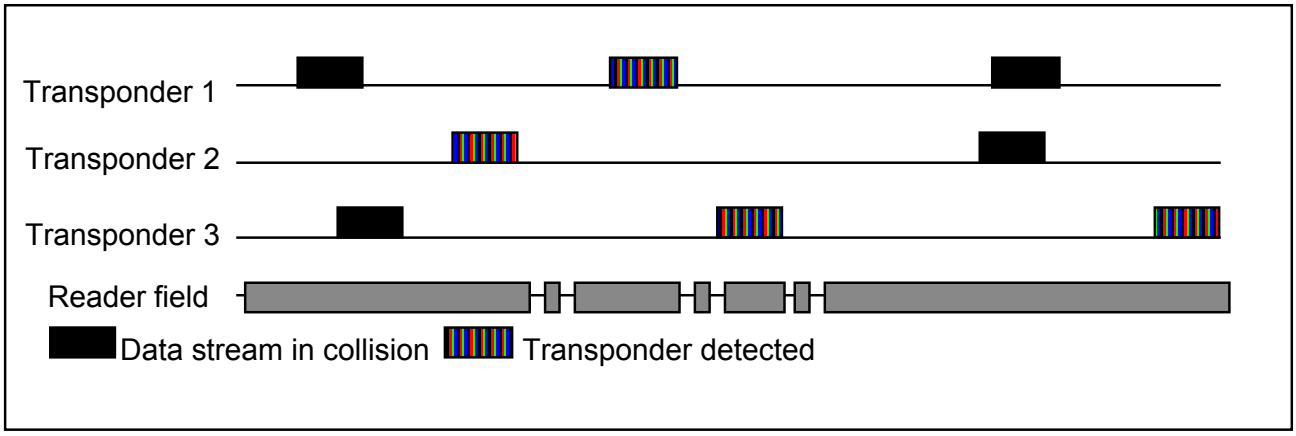

Fig. 12

Fast mode example

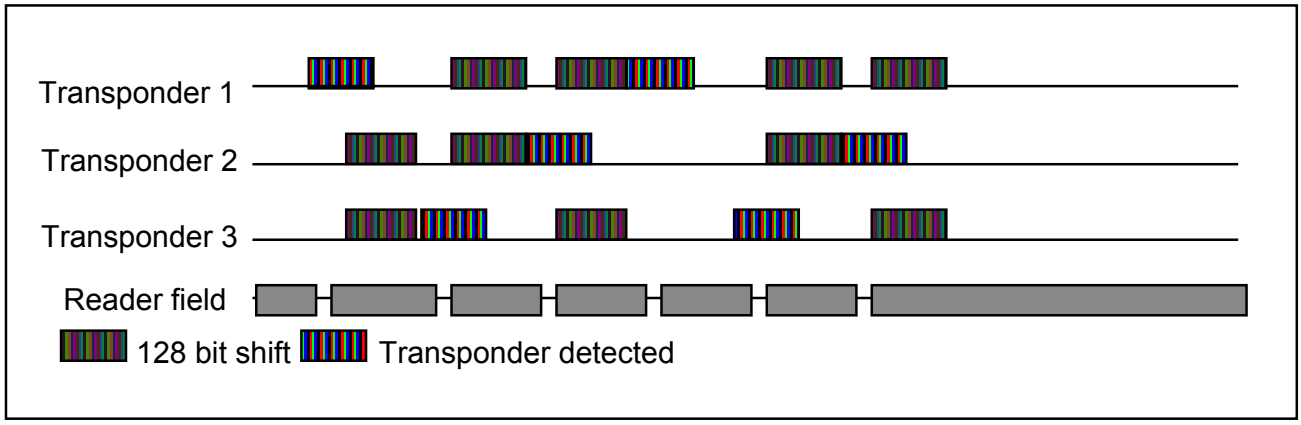

Fig. 13

Protocol combinations

The free-running and the two basic bi-directional protocols, switch-off and slow-down, can all be combined with the Fast protocol to give six different protocols, i.e. Normal free-running, slow-down, Normal switch-off, Fast free-running, slow-down, and Fast switch-off.

The following should be noted about the different protocols:

1) The switch-off protocols must be used for counting applications.

2) All the protocols except the switch-off protocols have built in redundancy because of the fact that they can transmit a code more than once.

3) Normal free-running is the only unidirectional protocol. It has the lowest power spectrum requirement because the reader transmits a CW wave.

4) Fast switch-off and Fast slow-down are the fastest protocols, and should be used where speed is important, or where the data rate limits the reading rate. Fast slow-down is slightly slower, but theoretically has a lower error rate.

5) For 125 kHz inductive applications using a 4 kbit/s data rate, Fast slow-down is probably the best overall protocol.

6) For RF applications using a 64 kbit/s data rate, normal free-running protocol is probably the best protocol.

Reader determined protocols

If the reader does not send MUTE signals to transponders that were programmed for one of the FAST protocols, the protocol merely reverts to the equivalent normal protocol. Similarly, if the reader does not send ACK signals to transponders that were programmed for SLOW-DOWN or SWITCH-OFF, the protocol reverts to a FREE-RUNNING protocol. In this manner, the reader can determine the protocol that is used.

Note, however, that unless a transponder was specifically programmed for the free-running protocol, its GAP input must be pulled down. This happens automatically in low frequency inductive applications, where the GAP input is pulled down by the internal GAP detector diode. In RF applications, however, the GAP input will have to be pulled down explicitly.

Protocol saturation

As the number of transponders in a reader beam is increased, the number of collisions increase, and it takes longer to read all the tags. This process is not linear. To read twice as many transponders could take more than twice as long. This effect is called protocol *saturation*.

The normal free-running protocol saturates the easiest of all the protocols, because it does not have any means of reducing the transmitting population. The Fast protocols, on the other hand, are virtually immune against saturation, as they prevent collisions by muting all transponders except the transmitting one.

One way of delaying the onset of saturation, is to reduce the initial repeat rate (not data rate) at which transponders transmit their codes. This is done by increasing the maximum random delay between transmissions.

Figure 14 and 15 below show's reading times for some possible versions

Optimum repeat delay settings

The following table lists the optimum repeat delay settings for each of the protocols vx number of transponders in a group.

Protocol	Number of transponders			
	3	10	30	100
Free-running	1k	4k	16k	64k
Slow-down	1k	1k	4k	16k
Switch-off	1k	1k	4k	16k
Fast Free-running	256	1k	1k	4k
Fast Slow-down	256	256	1k	1k
Fast Switch-off	256	256	1k	1k

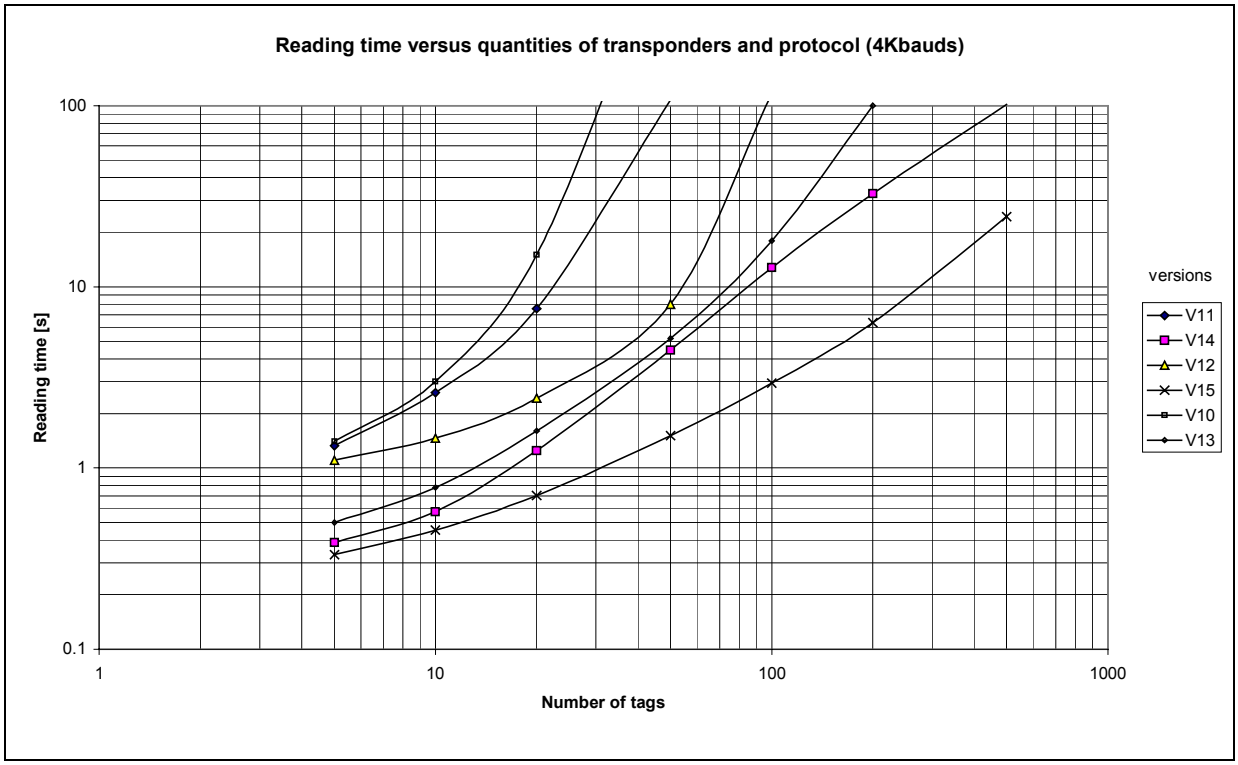

Fig. 14

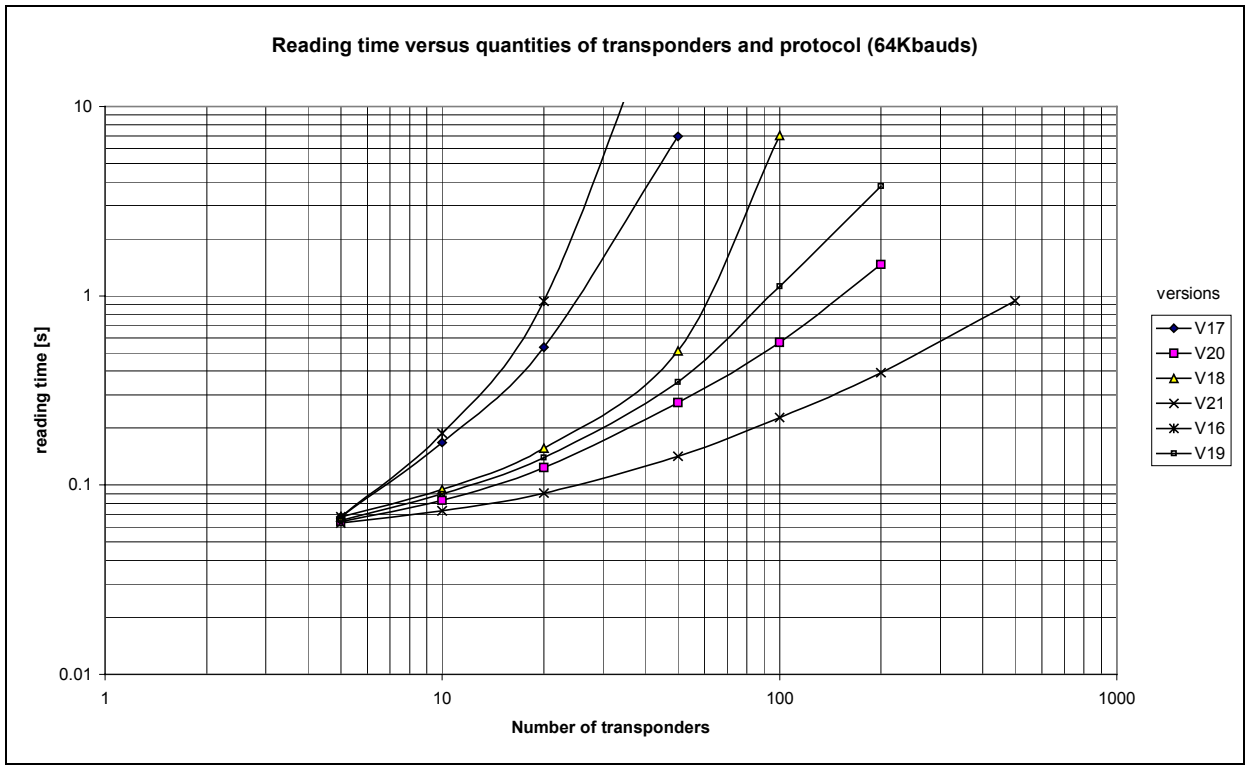

Fig. 15

Chip and Packaging Information

Chip size is 57 x 69 mil

Pad Location

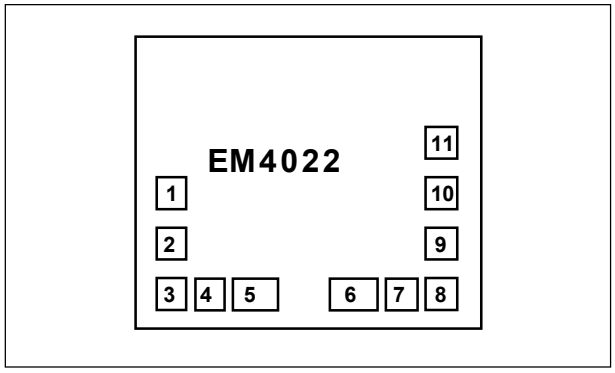

Fig. 16

Pad location table with reference on pad 3 center :

Pad N°	X [µm]	Y [µm]	size [µm]	Pad name	Function
1	0	417	98/98	XCLK	external test clock input
2	0	234	98/98	V_{DD}	positive supply
3	0	0	98/98	M	connection to antenna
4	125	0	98/98	M_{TST}	test output
5	228	0	175/98	COIL1	Coil terminal 1
6	1037	0	175/98	COIL2	Coil terminal 2
7	1200	-13	98/98	V_{SSTST}	negative test supply output
8	1324	1	98/98	V_{SS}	negative supply
9	1324	196	98/98	GAP	GAP input
10	1324	374	98/98	SI	Serial test data input (pull down)
11	1324	552	98/98	TMC	Test mode control (pull down)

Test inputs and outputs must be left open.

Ordering Information for samples

For other versions or other delivery form, please contact EM Microelectronic-Marin S.A. Please make sure to give complete part number when ordering (without spaces between letters).

Part Number	Control ROM [hex]	Data rate	Random Value	Protocol	Die Form & Thickness	Bumping	EM internal use only: Old version
EM4022 V10 WS11	302	4	Continuous	Free-Running	Sawn wafer, 11 mils	no bumps	010
EM4022 V11 WS11	328	4	4096	Slow down	Sawn wafer, 11 mils	no bumps	011
EM4022 V12 WS11	32C	4	4096	Switch off	Sawn wafer, 11 mils	no bumps	012
EM4022 V13 WS11	303	4	Continuous	Fast Free-Running	Sawn wafer, 11 mils	no bumps	013
EM4022 V14 WS11	321	4	1024	Fast Slow down	Sawn wafer, 11 mils	no bumps	014
EM4022 V15 WS11	325	4	1024	Fast Switch off	Sawn wafer, 11 mils	no bumps	015
EM4022 V16 WS11	202	64	Continuous	Free-Running	Sawn wafer, 11 mils	no bumps	016
EM4022 V17 WS11	228	64	4096	Slow down	Sawn wafer, 11 mils	no bumps	017
EM4022 V18 WS11	22C	64	4096	Switch off	Sawn wafer, 11 mils	no bumps	018
EM4022 V19 WS11	203	64	Continuous	Fast Free-Running	Sawn wafer, 11 mils	no bumps	019
EM4022 V20 WS11	229	64	4096	Fast Slow down	Sawn wafer, 11 mils	no bumps	020
EM4022 V21 WS11	220	64	4096	Fast Switch off	Sawn wafer, 11 mils	no bumps	021
EM4022 V%% WS11		custom	custom	custom	Sawn wafer, 11 mils	no bumps	%%%

For ICs to be used in mass production, the customer must define its options with the control ROM bit definition (page 9-10). Using this information, EM Microelectronic-Marin S.A. will define a complete new Part Number for ordering.

WARNING: Use of this product is subject to license from British Technology Group (BTG, www.btg-et.com)

Product Support

Check our Web Site under Products/RF Identification section.
Questions can be sent to cid@emmicroelectronic.com