Revision History

Revision 0.1 (Jan. 2012)

- First release.

1Gb (16M×4Bank×16) Double DATA RATE SDRAM

Features

- Internal Double-Date-Rate architecture with twice accesses per clock cycle.
- Single 2.5V ±0.2V Power Supply
- 2.5V SSTL-2 compatible I/O
- Burst Length (B/L) of 2, 4, 8
- CAS Latency: 3
- Bi-directional data strobe (DQS) for input and output data, active by both edges
- Data Mask (DM) for write data
- Sequential & Interleaved Burst type available
- Auto precharge option for each burst accesses
- DQS edge-aligned with data for Read cycles
- DQS center-aligned with data for Write cycles
- DLL aligns DQ & DQS transitions with CLK transition
- Auto Refresh and Self Refresh
- 8,192 Refresh Cycles / 64ms

Description

The EM42CM1684RTA is high speed Synchronous graphic RAM fabricated with ultra high performance CMOS process containing 1,073,741,824 bits which organized as 16Meg words x 4 banks by 16 bits.

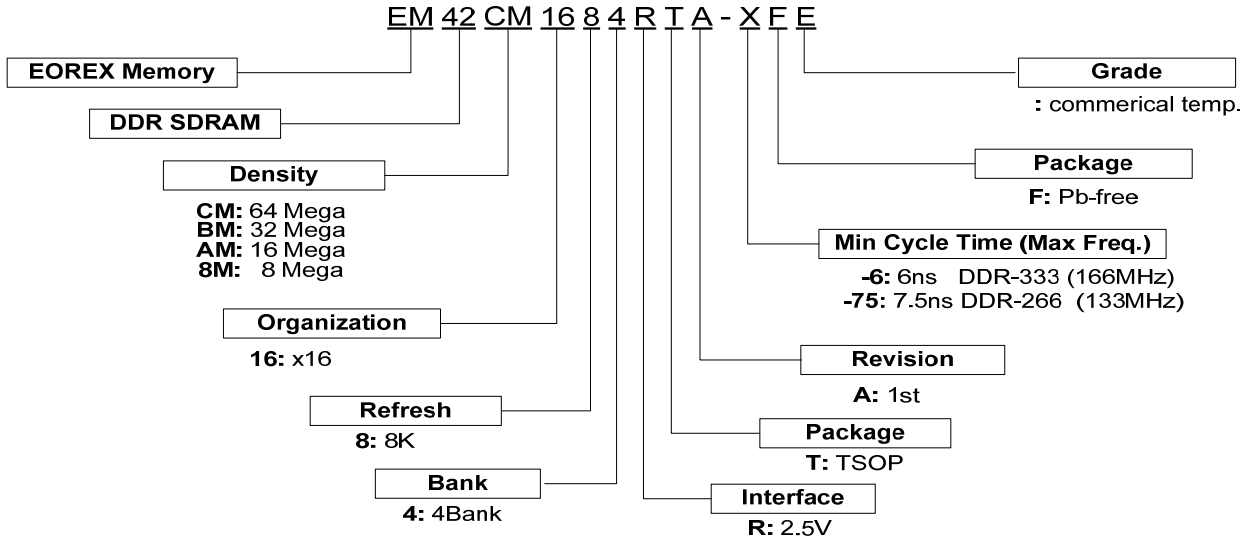
The 1Gb DDR SDRAM uses double data rate architecture to accomplish high-speed operation.

The data path internally prefetches multiple bits and transfers the data for both rising and falling edges of the system clock. It means the doubled data bandwidth can be achieved at the I/O pins.

Available package: TSOPII 66P 400mil.

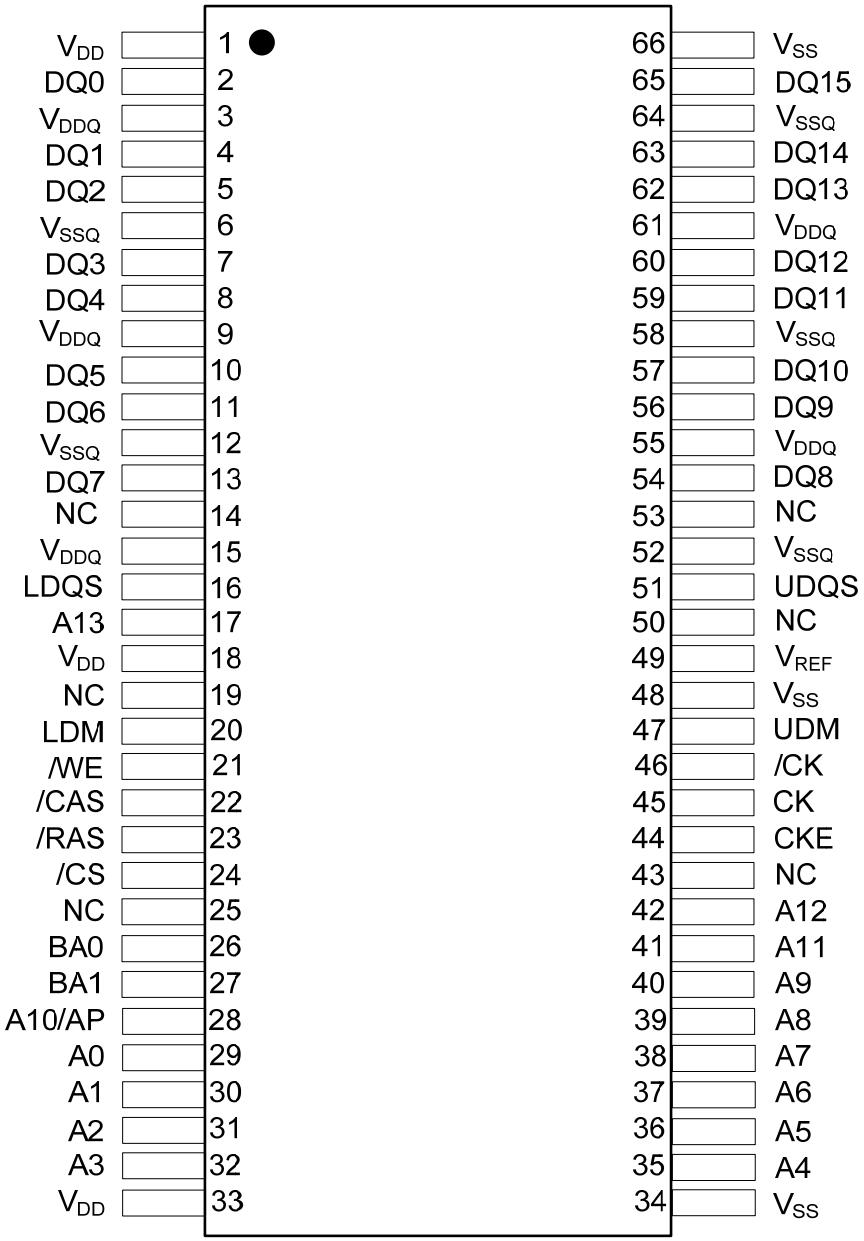
Ordering Information

Part No	Organization	Max. Freq	Package	Grade	Pb
EM42CM1684RTA-75F	64M X 16	133MHz @CL3-3-3	66pin TSOP(II)	Commercial	Free
EM42CM1684RTA-6F	64M X 16	166MHz @CL3-3-3	66pin TSOP(II)	Commercial	Free



* EOREX reserves the right to change products or specification without notice.

Pin Assignment



66pin TSOP-II

Pin Description (Simplified)

Pin	Name	Function
45,46	CLK,/CLK	**(System Clock)** Clock input active on the Positive rising edge except for DQ and DM are active on both edge of the DQS. CLK and /CLK are differential clock inputs.
24	/CS	**(Chip Select)** /CS enables the command decoder when"L" and disable the command decoder when "H". The new command are over-Looked when the command decoder is disabled but previous operation will still continue.
44	CKE	**(Clock Enable)** Activates the CLK when "H" and deactivates when "L". When deactivate the clock, CKE low signifies the power down or self refresh mode.
29~32,35~40 ,28,41,42,17	A0~A13	**(Address)** Row address (A0 to A13) and Column Address (CA0 to CA9) are multiplexed on the same pin. CA10 defines auto precharge at Column Address.
26, 27	BA0, BA1	**(Bank Address)** Selects which bank is to be active.
23	/RAS	**(Row Address Strobe)** Latches Row Addresses on the positive rising edge of the CLK with /RAS "L". Enables row access & pre-charge.
22	/CAS	**(Column Address Strobe)** Latches Column Addresses on the positive rising edge of the CLK with /CAS low. Enables column access.
21	/WE	**(Write Enable)** Latches Column Addresses on the positive rising edge of the CLK with /CAS low. Enables column access.
16/51	LDQS/UDQS	**(Data Input/Output)** Data Inputs and Outputs are synchronized with both edge of DQS.
20/47	LDM/UDM	**(Data Input/Output Mask)** DM controls data inputs. LDM corresponds to the data on DQ0~DQ7.UDM corresponds to the data on DQ8~DQ15.
2, 4, 5, 7, 8, 10, 11, 13, 54, 56, 57, 59, 60, 62, 63, 65	DQ0~DQ15	**(Data Input/Output)** Data inputs and outputs are multiplexed on the same pin.
1,18,33/ 34,48,66	V_{DD}/V_{SS}	**(Power Supply/Ground)** V_{DD} and V_{SS} are power supply pins for internal circuits.
3, 9, 15, 55.61/ 6, 12, 52, 58,64	V_{DDQ}/V_{SSQ}	**(Power Supply/Ground)** V_{DDQ} and V_{SSQ} are power supply pins for the output buffers.
14,19,25,43, 50,53	NC/RFU	**(No Connection/Reserved for Future Use)** This pin is recommended to be left No Connection on the device.
49	V_{REF}	**(Input)** SSTL-2 Reference voltage for input buffer.

Absolute Maximum Rating

Symbol	Item	Rating		Units
V_{IN}, V_{OUT}	Input, Output (I/O) Voltage	-0.5 ~ V_{DDQ} + 0.5		V
V_{IN}	Input Voltage	-1.0 ~ +3.6		
V_{DD}, V_{DDQ}	Power Supply Voltage	-1.0 ~ +3.6		V
T_{OP}	Operating Temperature Range	Commercial	0 ~ +70	°C
T_{STG}	Storage Temperature Range	-55 ~ +150		°C
P_D	Power Dissipation	1.6		W
I_{OS}	Short Circuit Current	50		mA

Note: Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (T_A=-0°C ~+70°C)

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Power Supply Voltage	2.3	2.5	2.7	V
V_{DDQ}	Power Supply Voltage (for I/O Buffer)	2.3	2.5	2.7	V
V_{REF}	I/O Logic high Voltage	0.49*V_{DDQ}	0.5*V_{DDQ}	0.51*V_{DDQ}	V
V_{TT}	I/O Termination Voltage	V_{REF}-0.04	-	V_{REF}+0.04	V
V_{IH}	Input Logic High Voltage	V_{REF}+0.15	-	V_{DDQ}+0.3	V
V_{IL}	Input Logic Low Voltage	-0.3	-	V_{REF}-0.15	V

Recommended DC Operating Conditions

(V_{DD}=2.5V±0.2V)

Symbol	Parameter	Test Conditions		Max.		Units
				-6	-75	
I_{DD1}	Operating Current ***(Note 1)***	Burst length=2, t_{RC}≥t_{RC}(min.), I_{OL}=0mA, One bank active		195	180	mA
I_{DD2P}	Precharge Standby Current in Power Down Mode	CKE≤V_{IL}(max.), t_{CK}=min		15	15	mA
I_{DD2N}	Precharge Standby Current in Non-power Down Mode (All banks idle)	CKE≥V_{IH}(min.), t_{CK}=min, /CS≥V_{IH}(min.), V_{IN}=V_{REF} Input signals are changed once per clock cycle		65	60	mA
I_{DD3P}	Active Standby Current in Power Down Mode	CKE≤V_{IL}(max.), t_{CK}=min One bank active, V_{IN}=V_{REF}		35	30	mA
I_{DD3N}	Active Standby Current in Non-power Down Mode	CKE≥V_{IH}(min.), t_{CK}=min, /CS≥V_{IH}(min.) Input signals are changed once per clock cycle		65	65	mA
I_{DD4}	Operating Current ***(Note 2)***	t_{CK} ≥ t_{CK}(min.), I_{OL}=0mA, One banks active, BL=2	READ	220	200	mA
			WRITE	230	210	
I_{DD5}	Refresh Current ***(Note 3)***	t_{RC}≥ t_{RFC} (min.), All banks active		340	330	mA
I_{DD6}	Self Refresh Current	CKE≤0.2V		9	9	mA
I_{DD7}	Operating current (Four Banks)	Four Banks interleaving, BL=4		525	485	mA

*All voltages referenced to V_{SS}.

Note 1: I_{DD1} depends on output loading and cycle rates.
Specified values are obtained with the output open.
Input signals are changed only one time during t_{CK} (min.)

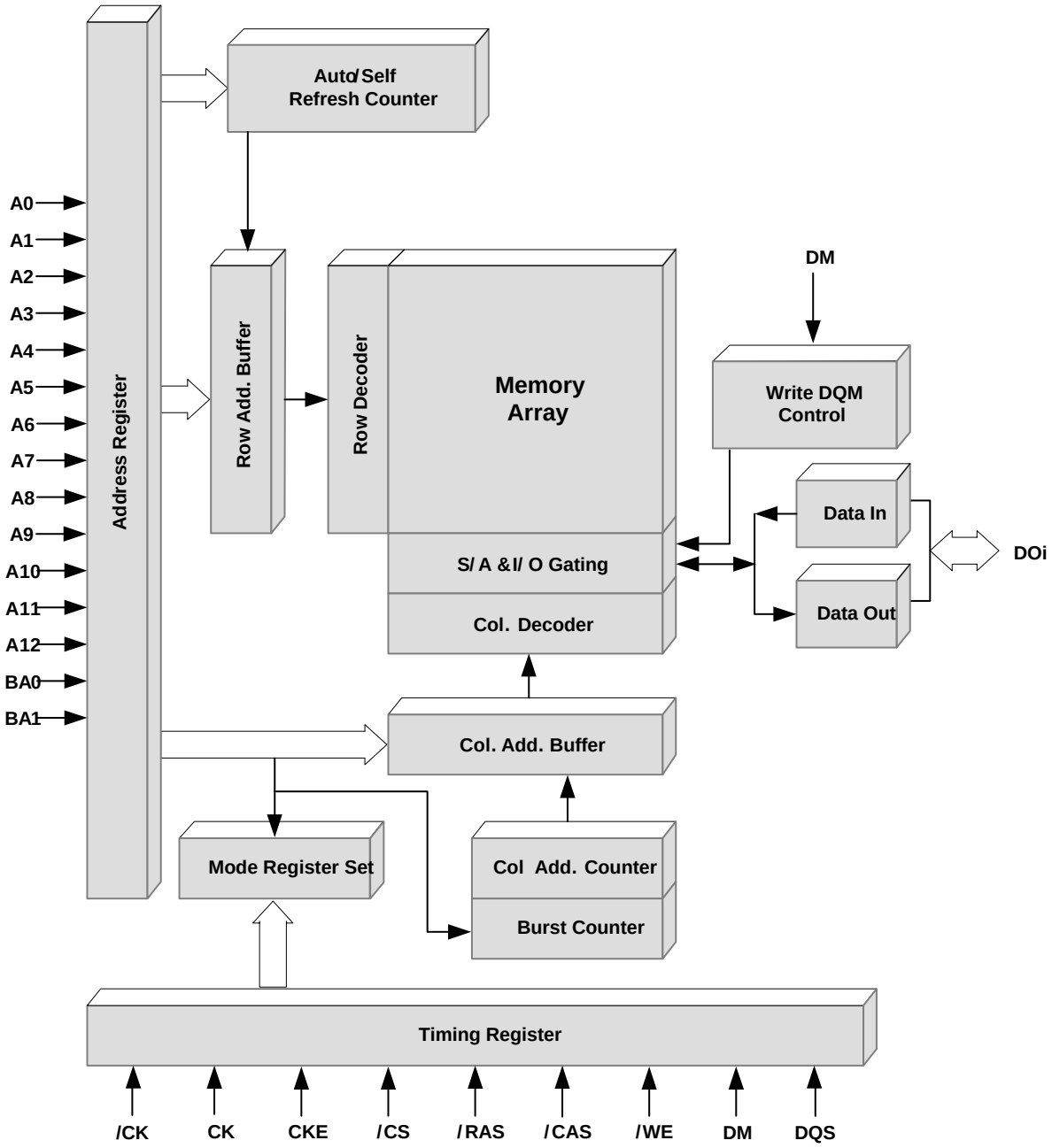
Note 2: I_{DD4} depends on output loading and cycle rates.
Specified values are obtained with the output open.
Input signals are changed only one time during t_{CK} (min.)

Note 3: Min. of t_{RFC} (Auto refresh Row Cycle Times) is shown at AC Characteristics.

Recommended DC Operating Conditions (Continued)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I_{IL}	Input Leakage Current	0≤V_I≤V_{DDQ}, V_{DDQ}=V_{DD} All other pins not under test=0V	-2	+2	uA
I_{OL}	Output Leakage Current	0≤V_O≤V_{DDQ}, D_{OUT} is disabled	-5	+5	uA
V_{OH}	High Level Output Voltage	I_{OUT} = -16.8mA	1.95	-	mA
V_{OL}	Low Level Output Voltage	I_{OUT} = +16.8mA	-	0.35	mA

Block Diagram



AC Operating Test Conditions

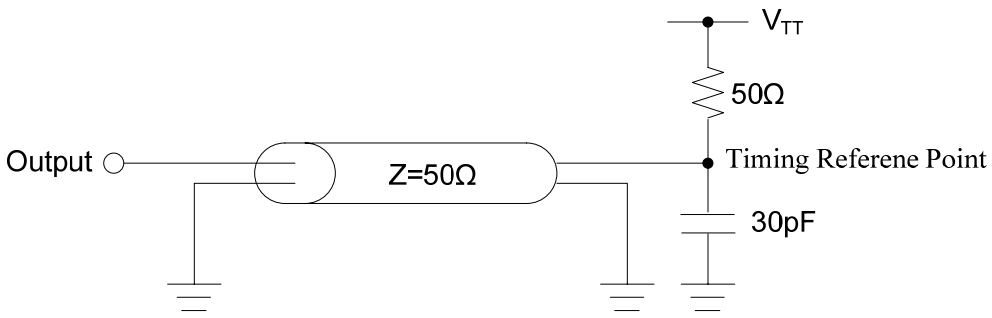
1. All voltages referenced to VSS.

2. Tests for AC timing, IDD, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

3. Outputs measured with equivalent load. Refer to the AC Output Load Circuit below.

4. AC timing and I_{DD} tests may use a V_{IL} to V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK, CK), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between V_{IL}(AC) and V_{IH}(AC).

5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input low (high) level.



AC Input Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
$V_{IH\ (AC)}$	Input (DQ,DQS &DM) High Voltage	V_{REF}+0.31	-	-	V
$V_{IL\ (AC)}$	Input (DQ,DQS &DM) Low Voltage	-	-	V_{REF}-0.31	V
$V_{ID\ (AC)}$	Input Differential (CK & /CK) Voltage	0.7	-	V_{DDQ}+0.6	V
$V_{IX\ (AC)}$	Input Crossing Point (CK & /CK)	0.5*V_{DDQ}-0.2	-	0.5*V_{DDQ}+0.2	V

AC Operating Test Characteristics

(V_{DD}=2.5V±0.2V)

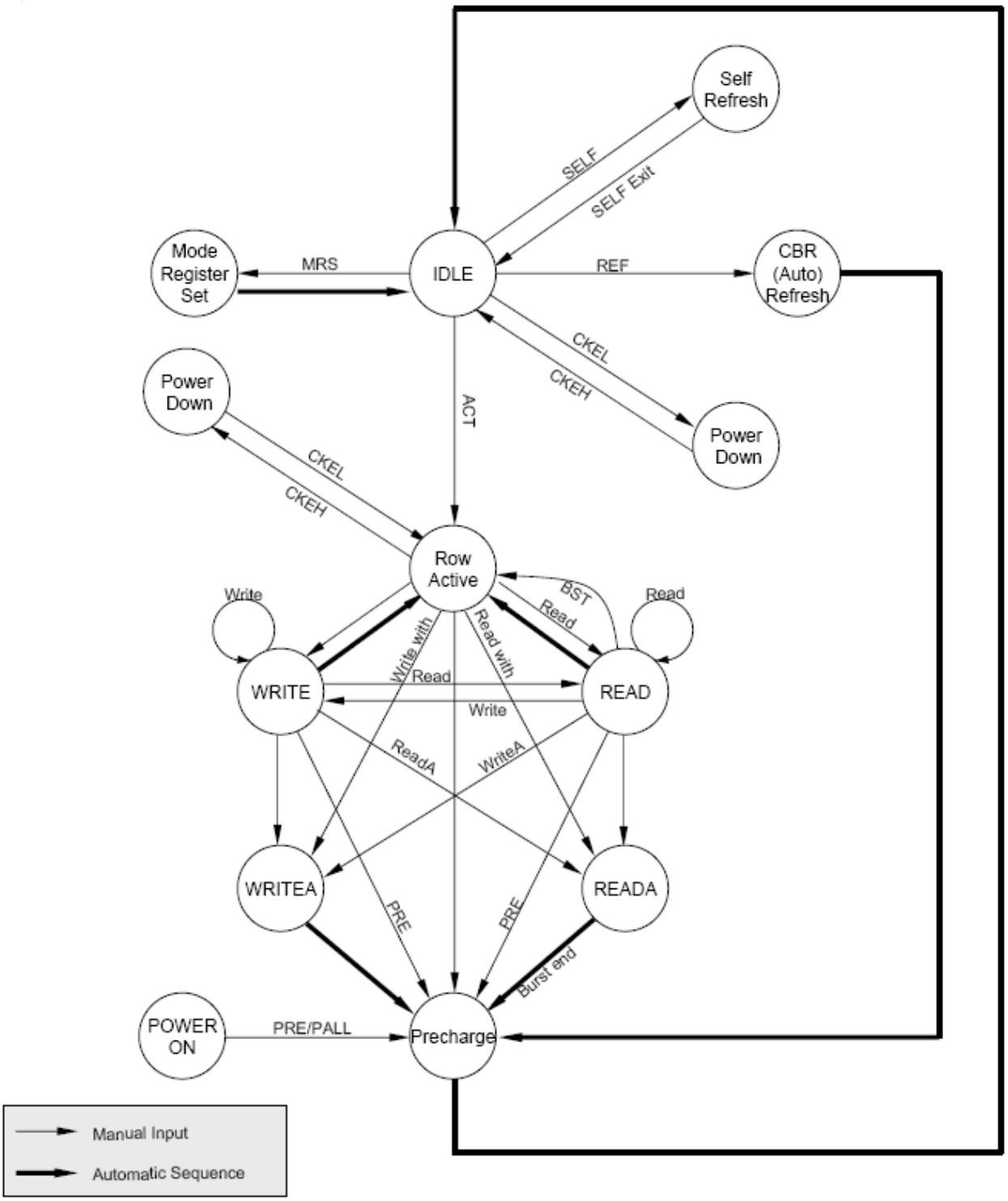
Symbol	Parameter		-6		-75		Units
			Min.	Max.	Min.	Max.	
t_{DQCK}	DQ output access from CLK,/CLK		-0.7	0.7	-0.75	0.75	ns
t_{DQSCK}	DQS output access from CLK,/CLK		-0.6	0.6	-0.75	0.75	ns
t_{CL},t_{CH}	CL low/high level width		0.45	0.55	0.45	0.55	t_{CK}
t_{CK}	Clock Cycle Time	CL=3	6	12	7.5	12	ns
t_{DH},t_{DS}	DQ and DM hold/setup time		0.45	-	0.5	-	ns
t_{DIPW}	DQ and DM input pulse width for each input		1.75	-	1.75	-	ns
t_{HZ},t_{LZ}	Data out high/low impedance time from CLK,/CLK		-0.7	0.7	-0.75	0.75	ns
t_{DQSQ}	DQS-DQ skew for associated DQ signal		-	0.4	-	0.5	ns
t_{DQSS}	Write command to first latching DQS transition		0.75	1.25	0.75	1.25	t_{CK}
t_{DSL},t_{DSH}	DQS input valid window		0.35	-	0.35	-	t_{CK}
t_{MRD}	Mode Register Set command cycle time		2	-	2	-	t_{CK}
t_{WPRES}	Write Preamble setup time		0	-	0	-	ns
t_{WPST}	Write Postamble		0.4	0.6	0.4	0.6	t_{CK}
t_{IH},t_{IS}	Address/control input hold/setup time (Slow)		0.8	-	1	-	ns
	Address/control input hold/setup time (Fast)		0.75	-	0.9	-	ns
t_{RPRE}	Read Preamble		0.9	1.1	0.9	1.1	t_{CK}
t_{DSH}	DQS falling edge from CLK rising, hold time		0.2	-	0.2	-	t_{CK}
t_{DSS}	DQS falling edge to CLK rising, setup time		0.2	-	0.2	-	t_{CK}

AC Operating Test Characteristics (Continued)

(V_{DD}=2.5V±0.2V)

Symbol	Parameter	-6		-75		Units
		Min.	Max.	Min.	Max.	
t_{RPST}	Read Postamble	0.4	0.6	0.4	0.6	t_{CK}
t_{RAS}	Active to Precharge command period	42	70k	45	120k	ns
t_{RC}	Active to Active command period	60	-	65	-	ns
t_{RFC}	Auto Refresh Row Cycle Time	72	-	75	-	ns
t_{RCD}	Active to Read or Write delay	18	-	20	-	ns
t_{RP}	Precharge command period	18	-	20	-	ns
t_{RRD}	Active bank A to B command period	12	-	15	-	ns
t_{RAP}	Active to READ with Auto Precharge command	18	-	20	-	ns
t_{WPRE}	DQS write Preamble	0.25	-	0.25	-	t_{CK}
t_{WR}	Write Recovery time	15	-	15	-	ns
t_{WTR}	Internal WRITE to READ command delay	1	-	1	-	t_{CK}
t_{XSNR}	Exit self Refresh to non-read command	75	-	75	-	ns
t_{XSRD}	Exit self Refresh to read command	200	-	200	-	t_{CK}
t_{REFI}	Average periodic refresh interval	-	7.8	-	7.8	us

Simplified State Diagram



1. Command Truth Table

Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA0, BA1	A10	A12~A0
		n-1	N							
Ignore Command	DESL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Burst Stop	BSTH	H	X	L	H	H	L	X	X	X
Read	READ	H	X	L	H	L	H	V	L	V
Read with Auto Pre-charge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with Auto Pre-charge	WRITA	H	X	L	H	L	L	V	H	V
Bank Activate	ACT	H	X	L	L	H	H	V	V	V
Pre-charge Select Bank	PRE	H	X	L	L	H	L	V	L	X
Pre-charge All Banks	PALL	H	X	L	L	H	L	X	H	X
Mode Register Set	MRS	H	X	L	L	L	L	OP Code		
Extended MRS	EMRS	H	X	L	L	L	L	OP Code		

H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

2. CKE Truth Table

Item	Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	Addr.
			n-1	n					
Idle	CBR Refresh Command	REF	H	H	L	L	L	H	X
Idle	Self Refresh Entry	SELF	H	L	L	L	L	H	X
Self Refresh	Self Refresh Exit	–	L	H	L	H	H	H	X
		–	L	H	H	X	X	X	X
Idle	Power Down Entry	–	H	L	X	X	X	X	X
Power Down	Power Down Exit	–	L	H	X	X	X	X	X

H = High level, L = Low level, X = High or Low level (Don't care)

3. Operative Command Table

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Idle	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA/CA/A10	READ/WRIT/BW	ILLEGAL ***(Note 1)***
	L	L	H	H	BA/RA	ACT	Bank active,Latch RA
	L	L	H	L	BA, A10	PRE/PREA	NOP***(Note 3)***
	L	L	L	H	X	REFA	Auto refresh***(Note 4)***
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode register
Row Active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA/CA/A10	READ/READA	Begin read,Latch CA, Determine auto-precharge
	L	H	L	L	BA/CA/A10	WRIT/WRITA	Begin write,Latch CA, Determine auto-precharge
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA/A10	PRE/PREA	Precharge/Precharge all
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Read	H	X	X	X	X	DESL	NOP(Continue burst to end)
	L	H	H	H	X	NOP	NOP(Continue burst to end)
	L	H	H	L	X	TERM	Terminal burst
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst,Latch CA, Begin new read, Determine Auto-precharge
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA, A10	PRE/PREA	Terminate burst, PrecharE
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Write	H	X	X	X	X	DESL	NOP(Continue burst to end)
	L	H	H	H	X	NOP	NOP(Continue burst to end)
	L	H	H	L	X	TERM	ILLEGAL
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst with DM="H",Latch CA,Begin read,Determine auto-precharge ***(Note 2)***
	L	H	L	L	BA/CA/A10	WRIT/WRITA	Terminate burst,Latch CA,Begin new write, Determine auto-precharge ***(Note 2)***
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA, A10	PRE/PREA	Terminate burst with DM="H", Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code,	MRS	ILLEGAL

3. Operative Command Table (Continued)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Read with AP	H	X	X	X	X	DESL	NOP(Continue burst to end)
	L	H	H	H	X	NOP	NOP(Continue burst to end)
	L	H	H	L	BA/CA/A10	TERM	ILLEGAL
	L	H	L	X	BA/RA	READ/WRITE	ILLEGAL ***(Note 1)***
	L	L	H	H	BA/A10	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	X	PRE/PREA	ILLEGAL ***(Note 1)***
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Write with AP	H	X	X	X	X	DESL	NOP(Continue burst to end)
	L	H	H	H	X	NOP	NOP(Continue burst to end)
	L	H	H	L	X	TERM	ILLEGAL
	L	H	L	X	BA/CA/A10	READ/WRITE	ILLEGAL ***(Note 1)***
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL ***(Note 1)***
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Pre-charging	H	X	X	X	X	DESL	NOP(idle after t_{RP})
	L	H	H	H	X	NOP	NOP(idle after t_{RP})
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA/CA/A10	READ/WRITE	ILLEGAL ***(Note 1)***
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA/A10	PRE/PREA	NOP(idle after t_{RP}) ***(Note 3)***
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Row Activating	H	X	X	X	X	DESL	NOP(Row active after t_{RCD})
	L	H	H	H	X	NOP	NOP(Row active after t_{RCD})
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA/CA/A10	READ/WRITE	ILLEGAL ***(Note 1)***
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL ***(Note 1)***
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

3. Operative Command Table (Continued)

Current State	/CS	/R	/C	/W	Addr.	Command	Action
Write Recovering	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TERM	NOP
	L	H	L	H	BA/CA/A10	READ	ILLEGAL ***(Note 1)***
	L	H	L	L	BA/CA/A10	WRIT/WRITA	New write, Determine AP
	L	L	H	H	BA/RA	ACT	ILLEGAL ***(Note 1)***
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL ***(Note 1)***
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
Refreshing	H	X	X	X	X	DESL	NOP(idle after t_{RP})
	L	H	H	H	X	NOP	NOP(idle after t_{RP})
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA/CA/A10	READ/WRIT	ILLEGAL
	L	L	H	H	BA/RA	ACT	ILLEGAL
	L	L	H	L	BA/A10	PRE/PREA	NOP(idle after t_{RP})
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Pre-charge

Note 1: ILLEGAL to bank in specified states;
Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.

Note 2: Must satisfy bus contention, bus turn around, and/or write recovery requirements.

Note 3: NOP to bank precharging or in idle state.May precharge bank indicated by BA.

Note 4: ILLEGAL of any bank is not idle.

4. Command Truth Table for CKE

Current State	CKE		/CS	/R	/C	/W	Addr.	Action
	n-1	n						
Self Refresh	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exist Self-Refresh
	L	H	L	H	H	H	X	Exist Self-Refresh
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP(Maintain self refresh)
Both bank precharge power down	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exist Power down
	L	H	L	H	H	H	X	Exist Power down
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP(Maintain Power down)
All Banks Idle	H	H	X	X	X	X	X	Refer to function true table
	H	L	H	X	X	X	X	Enter power down mode ***(Note 3)***
	H	L	L	H	H	H	X	Enter power down mode ***(Note 3)***
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	H	RA	Row active/Bank active
	H	L	L	L	L	H	X	Enter self-refresh ***(Note 3)***
	H	L	L	L	L	L	Op-Code	Mode register access
	H	L	L	L	L	L	Op-Code	Special mode register access
	L	X	X	X	X	X	X	Refer to current state
Any State Other than Listed above	H	H	X	X	X	X	X	Refer to command truth table

H = High level, L = Low level, X = High or Low level (Don't care)

Notes 1: After CKE's low to high transition to exist self refresh mode. And a time of t_{RC} (min) has to be elapse after CKE's low to high transition to issue a new command.

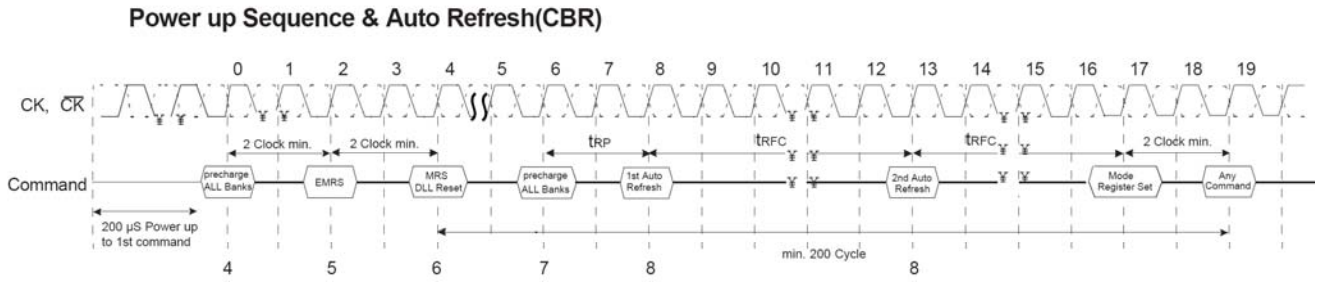
Notes 2: CKE low to high transition is asynchronous as if restarts internal clock.

Notes 3: Power down and self refresh can be entered only from the idle state of all banks.

The Sequence of Power-Up and Initialization

The following sequence is required for Power-Up and Initialization.

1. Apply power and attempt to maintain CKE at a low state (all other inputs may be undefined.)
- Apply VDD before or at the same time as VDDQ.
- Apply VDDQ before or at the same time as VTT & VREF.
2. Start clock and maintain stable condition for a minimum of 200us.
3. The minimum of 200us after stable power and clock (CLK, CLK), apply NOP & take CKE high.
4. Precharge all banks.
5. Issue EMRS to enable DLL.(To issue “DLL Enable” command, provide “Low” to A0, “High” to BA0 and “Low” to all of the rest address pins, A1~A11 and BA1)
6. Issue a mode register set command for “DLL reset”. The additional 200 cycles of clock input is required to lock the DLL. (To issue DLL reset command, provide “High” to A8 and “Low” to BA0)
7. Issue precharge commands for all banks of the device.
8. Issue 2 or more auto-refresh commands.
9. Issue a mode register set command to initialize device operation.



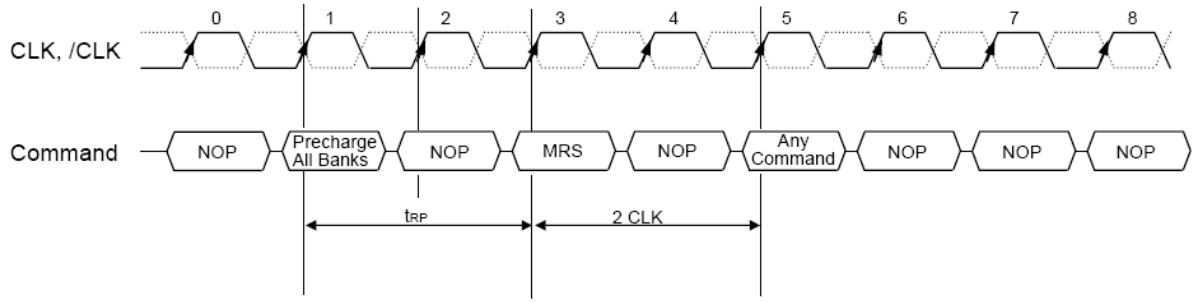
Note1 Every “DLL enable” command resets DLL. Therefore sequence 6 can be skipped during power up. Instead of it, the additional 200 cycles of clock input is required to lock the DLL after enabling DLL.

Mode Register Definition

Mode Register Set

The mode register stores the data for controlling the various operating modes of DDR SDRAM which contains addressing mode, burst length, /CAS latency, test mode, DLL reset and various vendor's specific opinions. The defaults value of the register is not defined, so the mode register must be written after EMRS setting for proper DDR SDRAM operation. The mode register is written by asserting low on /CS, /RAS, /CAS, /WE and BA0 (The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register.) The state of the address pins A0-A12 in the same cycle as /CS, /RAS, /CAS, /WE and BA0 going low is written in the mode register. Two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operating as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0-A2, addressing mode uses A3, /CAS latency (read latency from column address) uses A4-A6. A7 is used for test mode. A8 is used for DDR reset. A7 must be set to low for normal MRS operation.

MRS Cycle



Address input for Mode Register Set

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	MRS	RFU*				DLL	TM	CAS Latency			BT	Bust Length		

*RFU: Reserved for Future Use

An ~ A0	BA0
MRS cycle	0
EMRS	1

DLL Rest	A8
No	0
Yes	1

Mode	A7
Normal	0
Test	1

Burst Type	A3
Sequential	0
Interleave	1

CAS Latency	A6	A5	A4
Reserved	0	0	0
Reserved	0	0	1
Reserved	0	1	0
3	0	1	1
Reserve	1	0	0
Reserve	1	0	1
Reserve	1	1	0
Reserve	1	1	1

Burst Latency	A2	A1	A0
Reserve	0	0	0
2	0	0	1
4	0	1	0
8	0	1	1
Reserve	1	0	0
Reserve	1	0	1
Reserve	1	1	0
Reserve	1	1	1

Burst Type (A3)

Burst Length	A2	A1	A0	Sequential Addressing	Interleave Addressing
2	X	X	0	0 1	0 1
	X	X	0	1 0	1 0
4	X	0	0	0 1 2 3	0 1 2 3
	X	0	1	1 2 3 0	1 0 3 2
	X	1	0	2 3 0 1	2 3 0 1
	X	1	1	3 0 1 2	3 2 1 0
8	0	0	0	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
	0	0	1	1 2 3 4 5 6 7 0	1 0 3 2 5 4 7 6
	0	1	0	2 3 4 5 6 7 0 1	2 3 0 1 6 7 4 5
	0	1	1	3 4 5 6 7 0 1 2	3 2 1 0 7 6 5 4
	1	0	0	4 5 6 7 0 1 2 3	4 5 6 7 0 1 2 3
	1	0	1	5 6 7 0 1 2 3 4	5 4 7 6 1 0 3 2
	1	1	0	6 7 0 1 2 3 4 5	6 7 4 5 2 3 0 1
	1	1	1	7 0 1 2 3 4 5 6	7 6 5 4 3 2 1 0

*Page length is a function of I/O organization and column addressing

DLL Enable / Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disable the DLL for the purpose of debug or evaluation (upon existing Self Refresh Mode, the DLL is enable automatically.) Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

Output Drive Strength

The normal drive strength got all outputs is specified to be SSTL-2, Class II. Some vendors might also support a weak drive strength option, intended for lighter load and/or point to point environments.

Extended Mode Register Set (EMRS)

The Extended mode register stores the data enabling or disabling DLL. The value of the extended mode register is not defined, so the extended mode register must be written after power up for enabling or disabling DLL. The extended mode register is written by asserting low on /CS, /RAS, /CAS, /WE and high on BA0 (The DDR SDRAM should be in all bank precharge with CKE already prior to writing into the extended mode register.) The state of address pins A0-A10 and BA1 in the same cycle as /CS, /RAS, /CAS, and /WE going low is written in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. High on BA0 is used for EMRS. All the other address pins except A0 and BA0 must be set to low for proper EMRS operation.

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	MRS	RFU*										0	I/O	DLL

*RFU: Reserved for Future Use
Must be set to “0”

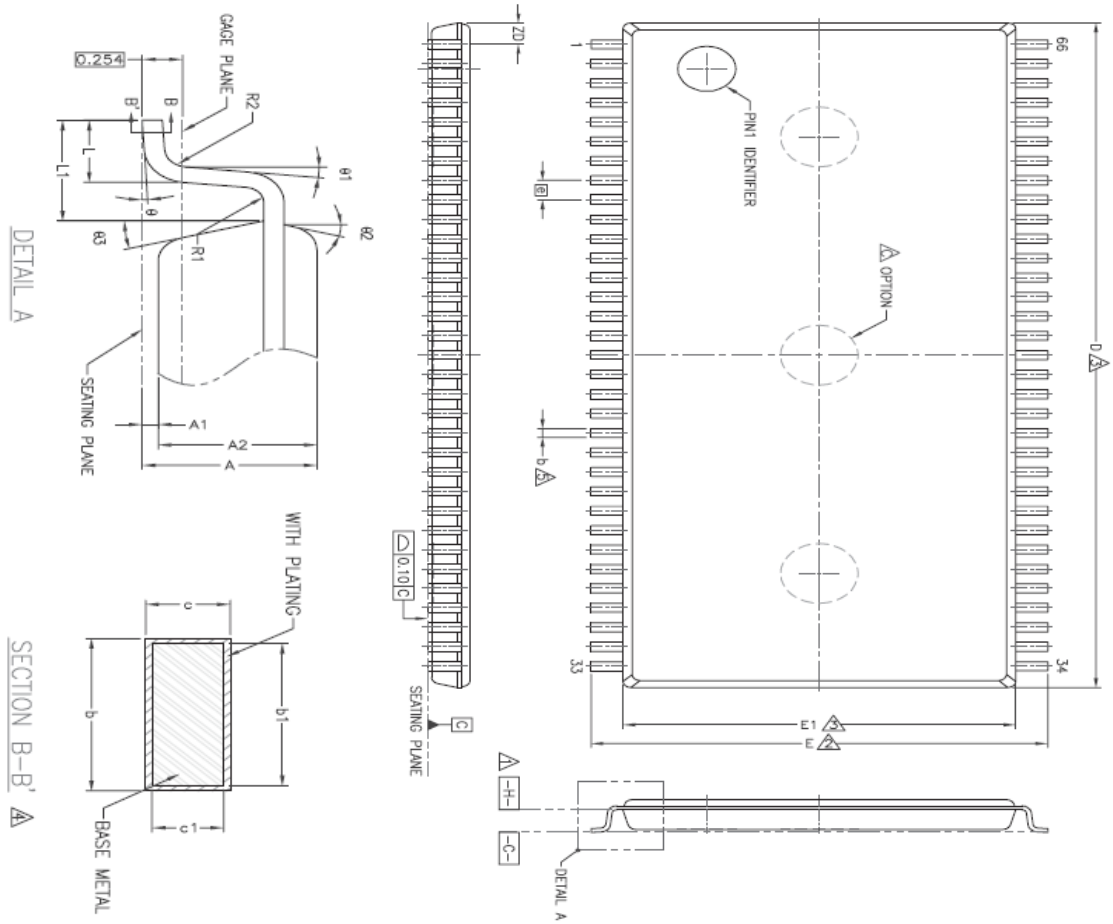
An ~ A0	BA0
MRS cycle	0
EMRS	1

I/O Strength	A1
Full	0
Half	1

DLL Enable	A0
Enable	0
Disable	1

Package Description

66-Pin Plastic TSOP-II (400mil)



Symbol	Dimension(mm)			Dimension(inch)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.2	-	-	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.22	-	0.38	0.009	-	0.015
b1	0.22	0.30	0.33	0.009	0.012	0.013
c	0.12	-	0.21	0.005	-	0.008
c1	0.10	0.127	0.16	0.004	0.005	0.006
D	22.22BSC			0.875BSC		
ZD	0.71REF			0.028REF		
E	11.76BSC			0.463BSC		
E1	10.16BSC			0.400BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.80REF			0.031REF		
e	0.65BSC			0.026BSC		
R1	0.12	-	-	0.005	-	-
R2	0.12	-	0.25	0.005	-	0.010

Symbol	MIN	NOM	MAX
θ	0	-	8
θ1	0	-	-
θ2	10	15	20
θ3	10	15	20

Note:
1. To be determined at seating plane -C-.
2. Datum plane -H- coincident with bottom of lead, where lead exits body.
3. Dimension D and E1 are determined at datum -H-.
   Dimension D does not include mold protrusions or gate burrs. Mold protrusions and gate burrs shall not exceed 0.15mm per side.
   Dimension E1 does not include interlead mold protrusions. Interlead mold protrusions shall not exceed 0.25mm per side.
4. These dimensions apply to the flat section of the lead between 0.10mm and 0.25mm from the lead tip.
5. Dimension b does not include dambar protrusion/intrusion.
6. Controlling dimension: millimeter.
7. Pin pitch refer to JEDEC STD MS-024, FC.