



## 512 bit Read/Write Contactless Identification Device

### Description

EM4469 is a CMOS integrated circuit intended for use in electronic Read/Write RF transponders.

The IC is powered by picking the energy from a continuous 125 kHz magnetic field via an external coil, which together with the integrated capacitor form a resonant circuit. The IC read out data from its internal EEPROM and sends it out by switching on and off a resistive load in parallel to the coil. Commands and EEPROM data updates can be executed by 100% AM modulation of the 125 kHz magnetic field.

There are several data rate and data encoding options available. Options are stored in EEPROM Configuration word. Read and write access to EEPROM can be protected by 32 bit password. All EEPROM words can be write protected by setting lock bits which transform them in read-only.

It contains factory programmed and locked 32 bit UID number, chip type and customer code.

### Typical Operating Configuration

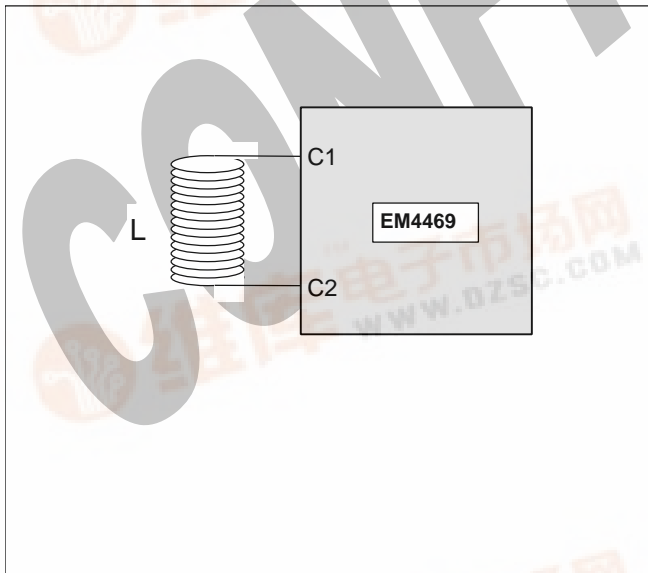


Fig. 1

### Features

- 512 bit EEPROM organised in 16 words of 32 bits
- 32 bit Password read and write protection
- 32 bit unique identification number (UID)
- 10 bit Customer code
- Lock feature convert EEPROM words in read only
- Multi-purpose encoding (Manchester, Biphase, Miller, PSK, FSK)
- Multi-purpose data rate from 1 up to 32 Kbaud
- Power-check for EEPROM write operation
- 100 to 150 kHz frequency range
- On-chip rectifier and voltage limiter
- No external supply buffer capacitor needed
- -40 to +85°C temperature range
- Very low Power consumption
- EM4469: trimmed resonant capacitor integrated on chip (330pF, 250pF or 75pF mask option)

### Applications

- Access Control
- Animal Identification
- Material Logistics



## Absolute Maximum Ratings

$V_{SS} = 0V$

Parameter	Symbol	Conditions
Input current on COIL1/COIL2	$I_{COIL}$	-30 to +30mA
Operating temperature range	$T_{OP}$	-40 to +85°C
Storage temperature range	$T_{STORE}$	-55 to +125°C
Electrostatic discharge to MIL-STD-883C method 3015	$V_{ESD}$	2000V

Table 1

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

## Handling Procedures

This device has built-in protection against high static voltages or electric fields. However due to the unique properties of this device, anti-static precautions should be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range.

## Operating Conditions

$V_{SS} = 0V$

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	$T_{OP}$	-40	+25	+85	°C
AC voltage on coil pins	$V_{COIL1}$			*	$V_{PP}$
Maximum coil current	$I_{COIL1}$	-10		10	mA
Frequency on coil pins	$F_{COIL1}$	100	125	150	kHz

Table 2

\*) Maximum voltage is defined by forcing 10mA on Coil1 – Coil2

## Electrical Characteristics

$V_{POS} = 2.0V$ ,  $V_{SS} = 0V$ ,  $f_{COIL1} = 125\text{ kHz}$  square wave,  $V_{COIL1} = 4V_{PP}$ ,  $T_{OP} = 25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply current in read mode	$I_{RD}$			1.8	3.0	$\mu\text{A}$
Supply current write mode	$I_{WR}$			25	40	$\mu\text{A}$
Modulator ON voltage drop	$V_{on1}$	$I_{(COIL2-COIL1)} = \pm 100\mu\text{A}$		2.2	2.8	V
		$I_{(COIL2-COIL1)} = \pm 5\text{mA}$		2.4	3.2	V
Limiter	$V_{LIM}$	$I_{(COIL2-COIL1)} = \pm 10\text{mA}$		8		V
POR level	$V_{POR}$	Rising edge		1.3		V
Clock extractor input min.	$V_{COIL1}$			1.4		$V_{PP}$
Resonance capacitor	$C_R$	330 pF option	320	330	340	pF
		250 pF option	245	250	255	pF
		75 pF option	70	75	80	pF
EEPROM data retention	$T_{RET}$	$T_{OP} = 55^\circ\text{C}$	10			years
EEPROM write cycles	$N_{CY}$	$V_{POS} = 3.0V$	100000			cycles

Table 3

**Note 1:** Data rate  $f_{RF}/64$ , Manchester code

**Note 2:** Based on 1000 hours at 150°C.

**Note 3:** applies only on EM4469 device

## Timing Characteristics

$V_{POS} = 2.0V$ ,  $V_{SS} = 0V$ ,  $f_{COIL1} = 125\text{ kHz}$  square wave,  $V_{COIL1} = 4V_{PP}$ ,  $T_{OP} = 25^\circ\text{C}$ ,

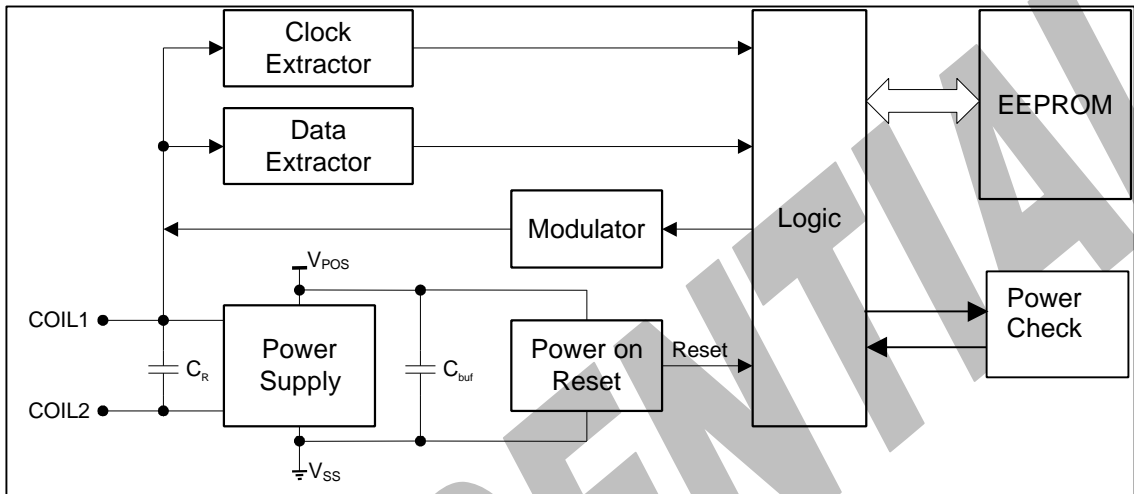
Data rate  $f_{RF}/64$ , Manchester code unless otherwise specified

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data Extractor timeout	$t_{MONO}$		20	30	40	$\mu\text{s}$
EEPROM programming time	$t_{Wee}$			6.7		ms
Power Check time	$t_{PC}$			512		$\mu\text{s}$
Initialisation after Write Word	$t_{INI}$			928		$\mu\text{s}$
Power-up initialisation	$t_{PU}$			2.5	3.0	ms
Processing Pause	$t_{PP}$			544		$\mu\text{s}$

Table 4



**Block Diagram**



**Functional Description**

The IC builds its power supply through an integrated rectifier. When it is placed in a magnetic field the DC internal voltage starts to increase.

As long the power supply is lower than the power on reset (POR) threshold, the circuit is in reset mode to prevent unreliable operation. In this mode the Modulator is off.

After the supply voltage cross the POR threshold, the circuit reads configuration word and then enters in default read mode according to configuration just read. During the configuration word readout the Modulator is also off.

While the IC is operating in Default Read mode it checks the coil signal to detect eventual command from reader. In the case reader field stops for a period longer than  $T_{MONO}$  it interrupts read mode and expects reader to send the command. In the case a valid command pattern is detected the command is executed. After execution of command the default read mode is entered.

**Block Description**

**Power Supply**

This block integrates an AC/DC converter, which extracts the DC power from the incident RF field. It will also acts as limiter, which clamps the voltage on coil terminals to avoid chip destruction in strong RF fields.

**Power On Reset (POR)**

When the EM4469 with its attached coil enters an electromagnetic field, the built in AC/DC converter will supply the chip. The DC voltage is monitored and a Reset signal is generated to initialise the logic. The Power On Reset is also provided in order to make sure that the chip will start issuing correct data. Hysteresis is provided to avoid improper operation at the limit level.

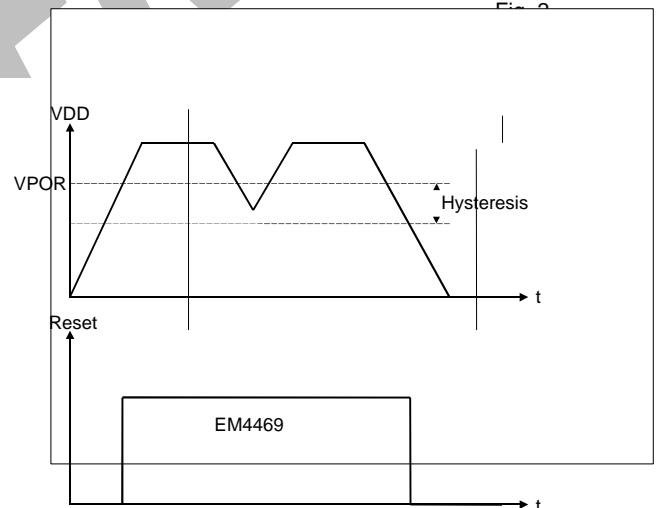


Fig. 3

**Clock Extractor**

The Clock extractor will generate a system clock with a frequency corresponding to the frequency of the RF field ( $f_{RF}$ ). The system clock is used by a sequencer to generate all internal timings.

**Data Extractor**

The transceiver generated field will be amplitude modulated (field stops) to transmit data to the EM4469. The Data extractor detects absence of signal on coil terminals for period longer than  $T_{MONO}$ .

**Modulator**

The Data Modulator is driven by Logic. When Modulator is switched ON it will draw a large current from both coil terminals, thus amplitude modulating the RF field.

**Power Check**

This block is used to check whether there is enough power available to securely write EEPROM.



### Logic

Logic is composed of several sub-blocks, which are described in the following text.

### Controller

Controller controls the state of the IC. Its main states are Power Off (power supply below POR level), Power-up Initialisation, Default Read, Command processing and Disabled state.

### Configuration register

At power-up when power supply level gets higher the POR threshold the content of EEPROM Configuration word is transferred in Configuration register to define default operating mode of the IC.

### Sequencer

It gets clock signal from Clock extractor and generates Data Rate clock and other timing signals needed for operation of other blocks. Data rate is defined by number 'n' stored in Configuration word.

### Encoder

Encoder encodes serial NRZ data before it is transmitted to Modulator. It has several options implemented to give different codes, which are frequently used in RFID (Manchester, Biphase, Miller, PSK, FSK).

### Command Decoder

Command Decoder observes output of Data Extractor. When a field stop is detected it puts Controller in Command Processing state and starts to decode data coming in.

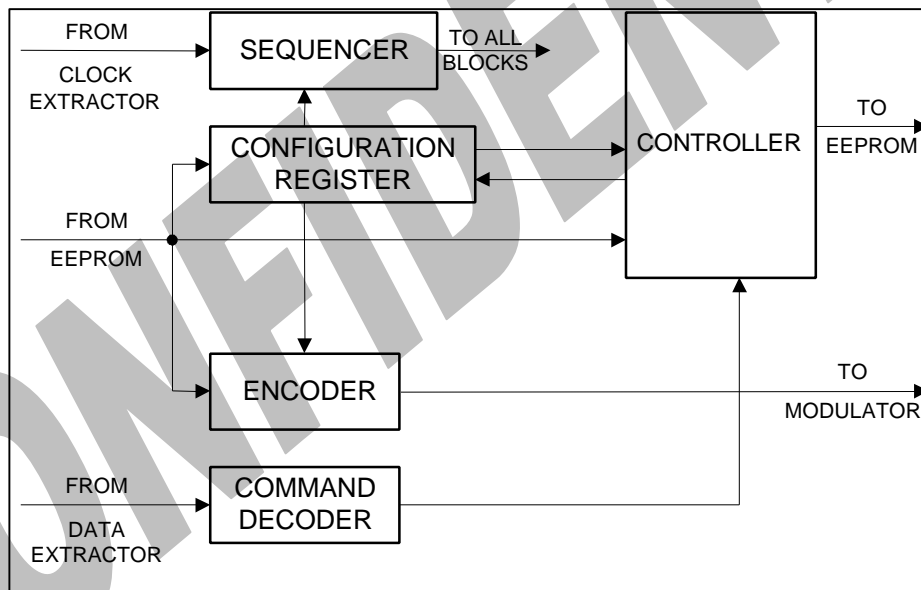


Fig.4

### EEPROM Organisation

The 512 bits of EEPROM are organised in 16 words of 32 bits.

The EEPROM words are numbered from 0 to 15, bits in a word are numbered from 0 to 31. The LSB first principle is always respected.

The 32 bits of EEPROM word are programmed with one Write Word Command.

The first two words are factory programmed Read Only words (words 0 and 1). They are assigned to Chip Type, Chip Version, Customer Code and Unique Identification Number (UID).

The next three words (words 2 to 4) are used to define device operation options (Housekeeping words). They consist of Password word, Protection word and Configuration word.

Words 5 to 15 are user free (352 user free bits).

Addr. (dec)	Description	Type	b <sub>0</sub> ,...	...,b <sub>31</sub>
0	Chip Type, Resonant Cap., Customer Code	RO	ct <sub>0</sub>	- ct <sub>31</sub>
1	UID	RO	uid <sub>0</sub>	- uid <sub>31</sub>
2	Password	WO	ps <sub>0</sub>	- ps <sub>31</sub>
3	Protection word	OTP	pr <sub>0</sub>	- pr <sub>31</sub>
4	Configuration word	RW	co <sub>0</sub>	- co <sub>31</sub>
5	User free	RW	us <sub>0</sub>	- us <sub>31</sub>
6	User free	RW	us <sub>0</sub>	- us <sub>31</sub>
7	User free	RW	us <sub>0</sub>	- us <sub>31</sub>
8	User free	RW	us <sub>0</sub>	- us <sub>31</sub>
9	User free	RW	us <sub>0</sub>	- us <sub>31</sub>
10	User free	RW	us <sub>0</sub>	- us <sub>31</sub>
11	User free	RW	us <sub>0</sub>	- us <sub>31</sub>
12	User free	RW	us <sub>0</sub>	- us <sub>31</sub>
13	User free	RW	us <sub>0</sub>	- us <sub>31</sub>
14	User free	RW	us <sub>0</sub>	- us <sub>31</sub>
15	User free	RW	us <sub>0</sub>	- us <sub>31</sub>



## Word types:

- RW: Reading and Writing possible
- RO: Read Only, changing content of this word is not possible
- WO: Write Only, reading of this word is not possible
- OTP: Bits of this word are One Time Programmable

Chip Type is a fix 4 bit number indicating member of the compatible family of chips. Resonant Capacitor is a fix 2 bit number indicating the value of integrated resonant capacitor. Customer Code is a 10 bit fixed code attributed to a customer. The other bits of word 0 are reserved for future use.

Word 1 contains 32 bit Unique Identification number (UID), which can not be changed by user.

The 32 bit Password word has to be sent in Login command to enable password protected operations. The Password word can not be read out by Read Word command.

The Protection word protects EEPROM words from being written. Every EEPROM word is protected by a pair of bits in Protection word. Once this bit pair is set to 11 the word cannot be written (it becomes read-only).

The Configuration word defines operating options: Data rate, Encoder, Last default read word (LWR), use of Password and some other options are defined in this word.

## Organisation of Word 0 Chip Type

Bits  $ct_1$  to  $ct_4$  of word 0 are indicating member of the compatible family of chips.

$ct_1, \dots, ct_4$	Chip Type
0100	EM4469

## Resonant Capacitor

Bits  $ct_5$  and  $ct_6$  are used to indicate resonant capacitor value.

$ct_5, ct_6$	Resonant cap
00	no resonant capacitor
10	75 pF
01	250 pF
11	330 pF

## Customer Code

Bits  $ct_9$  to  $ct_{18}$  are attributed to Customer code. Every customer can ask to get its own customer code. Default Customer code is 1000000000, where the leftmost bit is  $ct_9$ .

Bits  $ct_0$ ,  $ct_7$ ,  $ct_8$  and  $ct_{19} - ct_{31}$  are reserved for future use and are set to 0.

## Organisation of Configuration Word

Configuration word is used to define device operating mode.

### $co_0 - co_5$ : Data rate

Bits  $co_0 - co_5$  define a binary number 'n' where  $co_0$  is LSB and  $co_5$  is MSB. Data rate is defined as  $f_{RF}/2^{(n+1)}$ , where  $n \geq 1$ . The lowest data possible is therefore  $f_{RF}/128$  and the highest  $f_{RF}/4$ .

### $co_6 - co_9$ : Encoder

$co_6 - co_9$	Encoder
0000	no encoding (NRZ)
1000	Manchester
0100	Biphase
1100	Miller
1010	PSK2
0110	PSK3
0001	FSK
other	not used

### $co_{10}, co_{11}$ : PSK carrier frequency

$co_{10}, co_{11}$	PSK CF
00	$f_{RF}/2$
10	$f_{RF}/4$
01	$f_{RF}/8$
11	not used

### $co_{12}, co_{13}$ : Not used

### $co_{14} - co_{17}$ : Last default read word (LWR)

Bits  $co_{14} - co_{17}$  contain the binary word address of last word read in default read.  $co_{17}$  is MSB and  $co_{14}$  is LSB. Please note that valid range is only from 5 to 15.

### $co_{18}$ : Read login

In case this bit is set to logic 1 the reading of all words except RO words 0 and 1 by using Read Word command is protected. In order to read any of these words using Read Word command a Login Flag has to be set.

### $co_{19}$ : Read Housekeeping login

In case this bit is set to logic 1 the reading of all Housekeeping words by using Read Word command is protected. In order to read any Housekeeping word using Read Word command a Login Flag has to be set. Of course Password (word 2) can not be read since reading of this word is never possible.





**CO20: Write login**

In case this bit is set to logic 1 the EEPROM programming by using Write Word command is protected. In order to write any word using Write Word command a Login Flag has to be set.

**CO21: Write Housekeeping login**

In case this bit is set to logic 1 the programming of Housekeeping words by using Write Word command is protected. In order to write any Housekeeping word using Write Word command a Login Flag has to be set. Please note that writing to Password word is always protected by password.

**CO22: Read After Write**

In the case this bit is set to logic 1 the word just written by Write Word command is read before EM4469 transitions back in Default Read mode.

Please note that since reading from Password word is not possible this is the only possibility to read back the password just written.

**CO23: Disable**

In case this bit is set to logic 1 Disable command is accepted.

**CO24: RTF**

In case this bit is set to logic 1 there is no modulation in Default Read, EM4469 operates in Reader Talk First (RTF) mode. In this mode communication is done only using commands.

**CO25 - CO31: Reserved for future use**

**Organisation of Protection Word**

The Protection word protects EEPROM words from being written.

The bits in protection word are one time programmable (OTP) which means that once they have been set to 1 they can not be reset to 0 any more.

Every EEPROM word is protected by a bit pair in Protection word. State 00 of the pair means that the word is not protected, state 11 means write protection. 01 and 10 states are not allowed. Due to the OTP feature of bits in Protection word a word once protected becomes read only and can not be reverted back to RW. Please note that it is possible to protect the Protection word itself, in that case the protection system is locked and cannot be changed any more.

<b>Bit</b>	pr <sub>0</sub>	pr <sub>1</sub>	pr <sub>2</sub>	pr <sub>3</sub>		pr <sub>30</sub>	pr <sub>31</sub>
<b>Word</b>	W <sub>0</sub>		W <sub>1</sub>			W <sub>15</sub>	

Table above presents the location of bit pair protecting a certain word. Bits pr<sub>0</sub> and pr<sub>1</sub> protect word 0, bits pr<sub>2</sub> and pr<sub>3</sub> word 1 and so on.

The protection bits of RO words 0 and 1 are already factory programmed to 1.

**EEPROM Delivery State**

As already mentioned above, in all cases the words 0 and 1 are factory programmed and locked.

In the case a Customer code is attributed, the content of other words can be personalised according to customer wish.

In case of default configuration with Customer code 1 Password, Configuration word and user free words are all set to 0, the protection bits of RO words 0 and 1 are of course factory programmed to 1, other protection bits are also set to 0.

Register name	LSB.. ..MSB	Comments
Customer code	1000000000	
Data rate	011111	RF/64 (2Kbaud)
Encoder	1000	Manchester
PSK carrier frequency	00	f <sub>RF</sub> /2 (not used in this case)
Last default read word	1111	Last word read is at address 15
Read Login	0	No login required
Read Housekeeping login	0	No login required
Write login	0	No login required
Write Housekeeping login	0	No login required
Read After Write	0	No read after write
Disable	0	Disable command is not accepted
RTF	0	TTF mode (modulation active)
All reserved and unused bits	0	

**Default Read**

After the supply voltage crosses the POR threshold, the circuit enters Power-up Initialisation in which it reads Configuration word and then transitions in Default Read mode according to configuration just read.

In Default Read mode the chip will continuously send data starting from word 5 and finishing with word LWR. After sending last bit (31) of word LWR readout continues without interruption with first bit of word 5. In the case word 5 is set as LWR only word 5 is repeated.

**Forward Link Communication (Reader to Tag)**

As already mentioned commands can be send from reader to tag by initiating a command while chip is in Default read. The communication is done by using 100% modulation of reader field (also called field stops or OOK).

The first field stop initialise Command mode. Since it can happen while modulator switch is OFF it needs to be long enough to stop oscillation on coil terminals for at least T<sub>MONO</sub>.



## EM4050 Code (figure 5)

At reception of the first field stop, the chip stops immediately the reading and expects then another bit "0" to switch to receive mode. The transceiver and the chip are now synchronised and further data is sent with a bit rate of 32 periods of the RF field.

The EM4469 turns "ON" its modulator at the beginning of each frame of 32 clock periods corresponding to one bit. To send a logic "1" bit, the transceiver continues to send clocks without modulation. After 16 clocks, the modulation device is turned "OFF" allowing recharge of the internal supply capacitor. To send a logic "0" bit, the transceiver stops sending clocks (100% modulation) during the first half of a bit period (first 16 periods with modulation device ON). In order to correctly detect the field "OFF" the transceiver must wait that modulation

device switch ON before turning "OFF" the field. It is recommended to turn "OFF" the field after 4 clocks of the bit period, the minimum requirement is 1. In the recommended case the field is stopped from clock 5 to 16 of the bit period, and then turned "ON" again for the remaining 16 periods.

While the transceiver is sending data to the transponder, two different modulations will be observed on both coils. During the first 16 clocks of a bit period, the EM4469 is switching "ON" its modulation device causing a modulation of the RF field. This modulation can also be observed on the transceiver's coil. To send a bit "0" the transceiver will switch "OFF" the field, and this 100% modulation will be observed on the transponder coil.

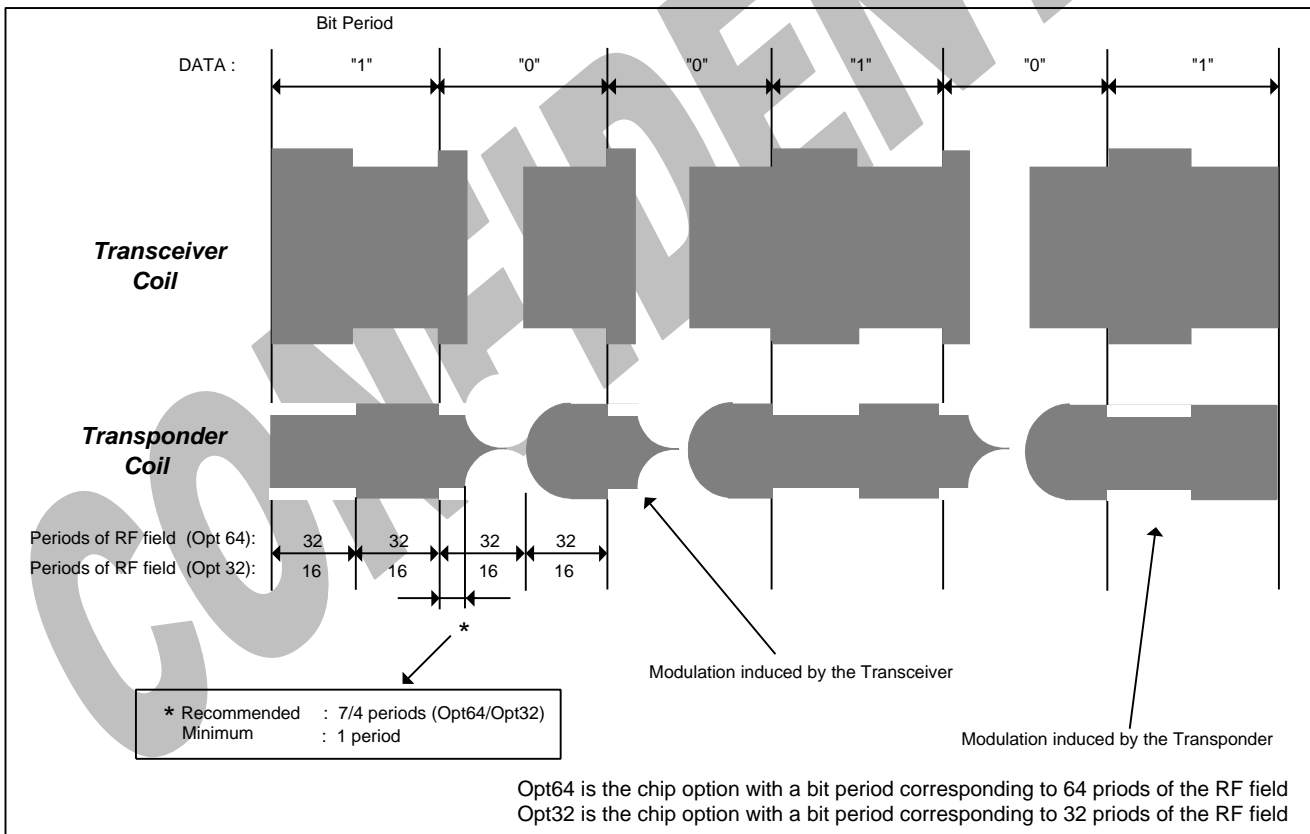


Fig.5

## Commands

Command structure:

All commands start by 3 bit command code, followed by command arguments. Possible command arguments are a word address and a 32 bit data field.

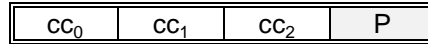
The 3 bit command code is terminated by an even parity bit.

The address field contains 4 bit address, two bits at 0 reserved for future extension and an even parity bit.

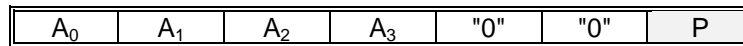
The 32 bit data field has an even parity bit inserted every 8 data bits, data is terminated with 8 column parity bits and a 0. The figures below represent the organisation of command fields.



### Command code structure:



### Address structure:



### Data structure:

D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	P <sub>0</sub>
D <sub>8</sub>	D <sub>9</sub>	D <sub>10</sub>	D <sub>11</sub>	D <sub>12</sub>	D <sub>13</sub>	D <sub>14</sub>	D <sub>15</sub>	P <sub>1</sub>
D <sub>16</sub>	D <sub>17</sub>	D <sub>18</sub>	D <sub>19</sub>	D <sub>20</sub>	D <sub>21</sub>	D <sub>22</sub>	D <sub>23</sub>	P <sub>2</sub>
D <sub>24</sub>	D <sub>25</sub>	D <sub>26</sub>	D <sub>27</sub>	D <sub>28</sub>	D <sub>29</sub>	D <sub>30</sub>	D <sub>31</sub>	P <sub>3</sub>
PC <sub>0</sub>	PC <sub>1</sub>	PC <sub>2</sub>	PC <sub>3</sub>	PC <sub>4</sub>	PC <sub>5</sub>	PC <sub>6</sub>	PC <sub>7</sub>	"0"

There are four commands implemented:

Login, Write Word, Read Word and Disable.

CC <sub>0</sub> - CC <sub>2</sub>	P	Command
001	1	Login
010	1	Write Word
100	1	Read Word
101	0	Disable

### Login Command

Sending login command is necessary before sending any password protected command. In Login command a 32 bit password including parity bits is sent as command parameter. The 32 bit password is sent according to Data structure defined above (45 bits including parity). In the case the parity bits are correct and 32 bit password sent matches with content of word 2 a login flag is set.

Login flag is set until next power-up, which means that Login command has to be sent only once after power up to enable execution of password protected commands.

In case Login command is successfully processed IC responds with preamble pattern (00001010) and returns in Default Read mode.

In case the Login is not accepted (wrong password or error in parity) a pattern 00000001 is sent and IC returns in Default Read mode.

### Write Word Command

In Write Word command first the 4 bit word address is sent followed by 32 bit data. In the case command is correctly processed IC first checks if the login flag is set (for the case writing is password protected), if addressed word is not write protected and if there is enough power to write EEPROM. In case all these conditions are fulfilled and there is no parity error EEPROM is written. After EEPROM is written the Configuration word is reloaded from EEPROM, a preamble pattern (00001010) is sent and chip returns in Default Read mode.

Loading of Configuration word is useful for the case the Configuration word has just been changed so that new settings are loaded.

In the case a Read-after-write bit is set the word just written is sent after the preamble pattern. Response is equivalent to the response of Read Word command.

In case the Write Word command is not accepted (error in parity or at least one of the checks failed) a pattern 00000001 is sent and IC returns in Default Read mode.

### Read Word Command

In read word command the four bit word address is sent as command parameter. In the case command is correctly processed IC first checks if the login flag is set in the case reading is password protected. In case readout is authorised a preamble pattern (00001010) followed by content of 32 bit word is sent. Please note that the 32 bit data is sent in Command data structure format (45 bits including parity bits) which is not the same as in Default Read where only the data from EEPROM is read.

In case the Read Word command is not accepted (parity error, password protection or reading from address 2) a pattern 00000001 is sent and IC returns in Default Read mode.

### Disable Command

Disable command is accepted in the case Disable bit of configuration word is set to 1.

In Disable command an all-1 data field is sent as command parameter (45 bits including parity bits, where parity bits are all 0). Command structure is therefore similar to Login command.

When this command is detected chip stops all operations until next power-up.

In case the Disable command is not accepted (Disable bit set to 0, parity error or some other data then all-1) a pattern 00000001 is sent and IC returns in Default Read mode.

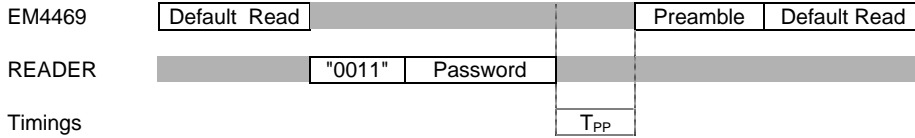
### Error during Command Detection

In case a command code which is not supported or a command parity bit error are detected the IC exits command processing and returns in Default Read mode without sending any message.

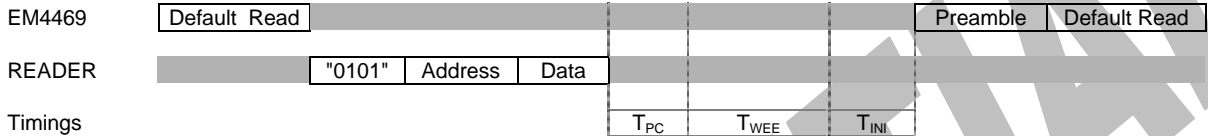




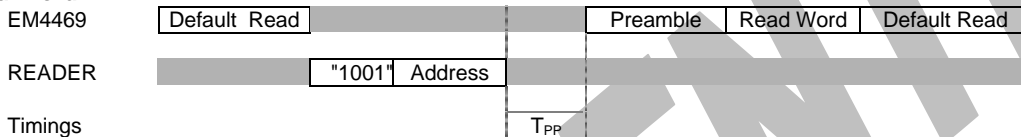
### Login



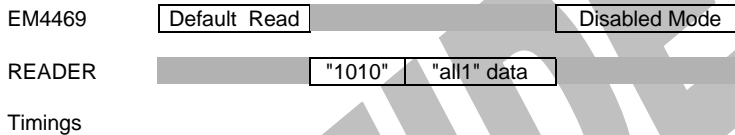
### Write Word



### Read Word



### Disable



### Return Link Encoder (Tag to Reader)

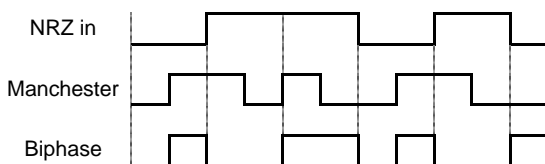
As described before the NRZ data coming from EEPROM pass in read mode (Default read or answer to Read Word command) through Encoder before it is transferred to Modulator. The logic 1 (high) means Modulator is on.

#### Manchester Code:

In Manchester coding there is a transition from High to Low or from Low to High in the middle of bit period. When logic 0 is transmitted first half of bit period the output is Low and second half of bit period it is High. When logic 1 is transmitted first half of bit period the output is High and second half of bit period it is Low.

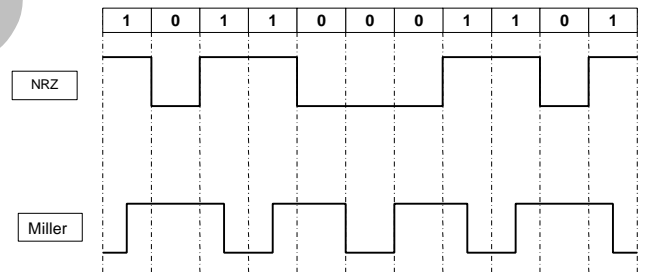
#### Biphase Code

In Biphase coding there is a transition from High to Low or from Low to High at the beginning of each bit period. In the case logic 0 is transmitted there is additional transition in the middle of bit period. In case logic 1 is transmitted there is no transition in the middle of bit period.



#### Miller Code

Advantage of Miller code is that minimum pulse duration is one bit period. See figure below for example of Miller code. In the case logic 1 is transmitted there is a transition in middle of bit period. In case a single 0 is transmitted there is no transition, in case of more zeros there are transitions in beginning of bit period starting with second zero.



#### PSK Codes

There are two types of PSK codes implemented. The PSK subcarrier frequency can also be defined ( $f_{RF}/2$ ,  $f_{RF}/4$  and  $f_{RF}/8$  are implemented). For correct operation of PSK codes the selected data rate has to be an integer multiple of PSK subcarrier frequency.

- PSK2: Phase change on bit clock when input high
- PSK3: Phase change on rising edge of input

#### FSK Code:

In case logic 0 is present on the input a signal with frequency  $f_{RF}/5$  is transmitted to output. In case logic 1 is present on the input a signal with frequency  $f_{RF}/8$  is transmitted to output.

Code	Logic 1	Logic 0
FSK	$f_{RF}/8$	$f_{RF}/5$

#### Examples of Settings

EM H4001, H4002, H4100 ver. 01:

Data rate:  $f_{RF}/64$   
Encoder: Manchester  
LWR: 6 (64 bits)

ISO11785 FDX-B

Data rate:  $f_{RF}/32$   
Encoder: Biphase  
LWR: 8 (128 bits)



**Package Information**

**Dimensions of PCB and CID version**

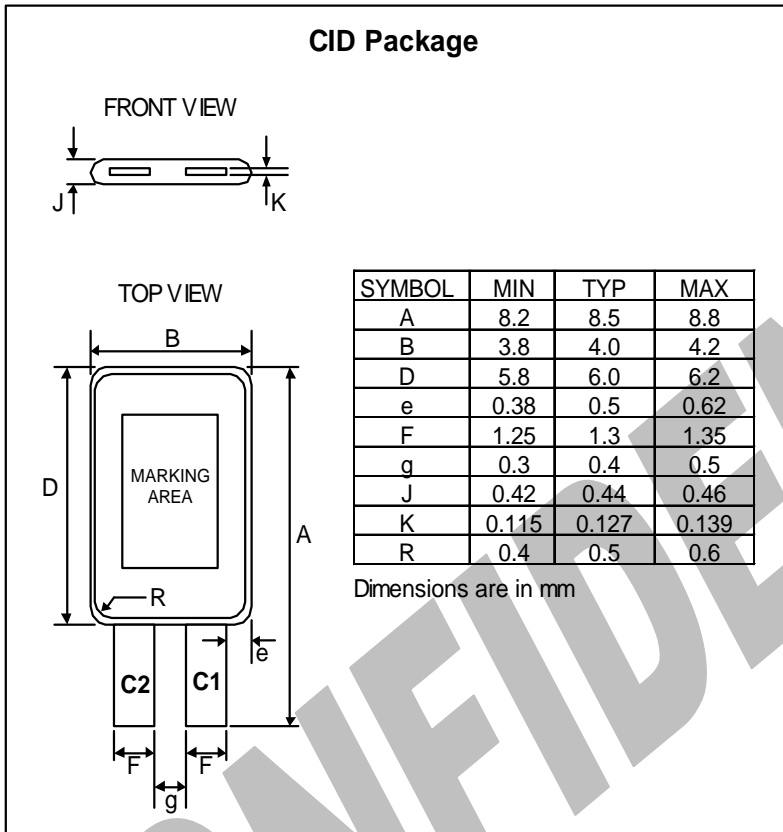


Fig. 6

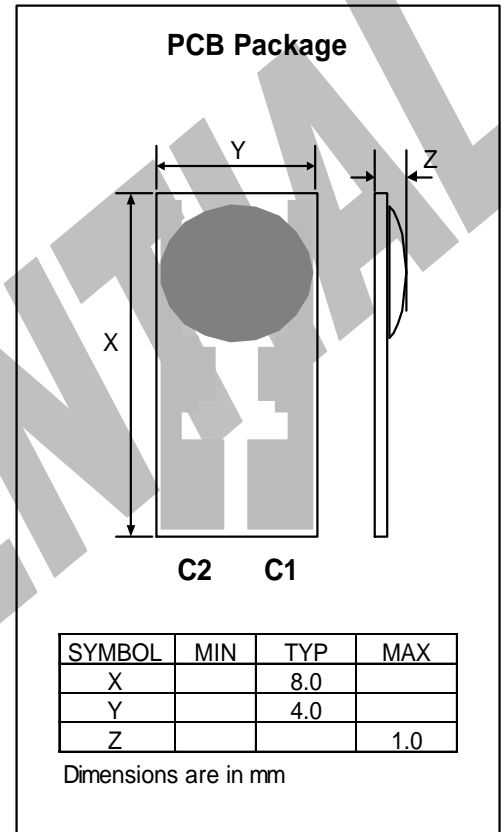


Fig. 7

**Pad Location**

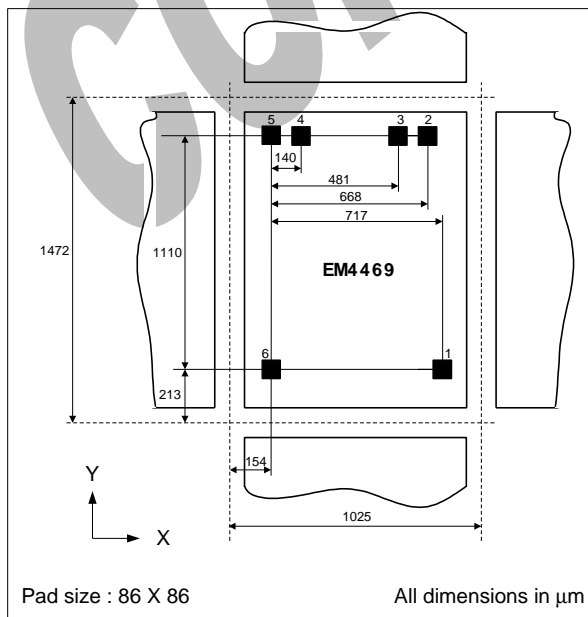


Fig. 8

**Pad Description**

Pad	Name	Function
1	Coil 1	Coil connection 1
2	Vpos	Internal supply voltage
3	Test_o	Test output
4	Test_i	Test input
5	Vss	Internal supply ground
6	Coil 2	Coil connection 2

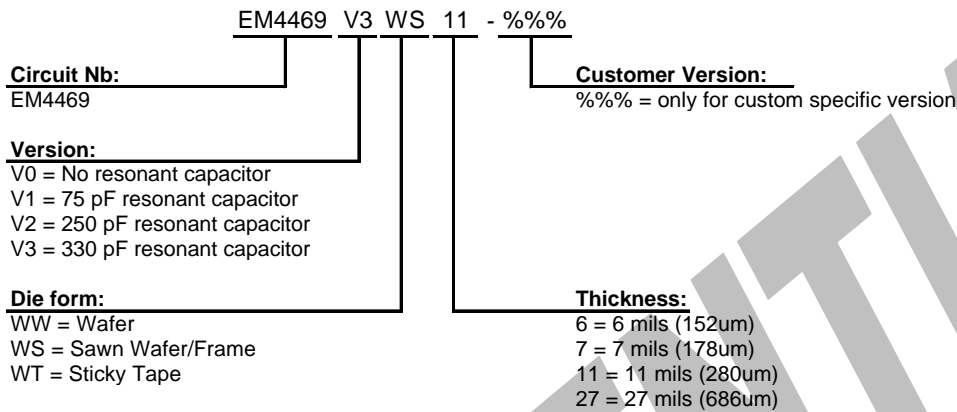


# Preliminary EM4469

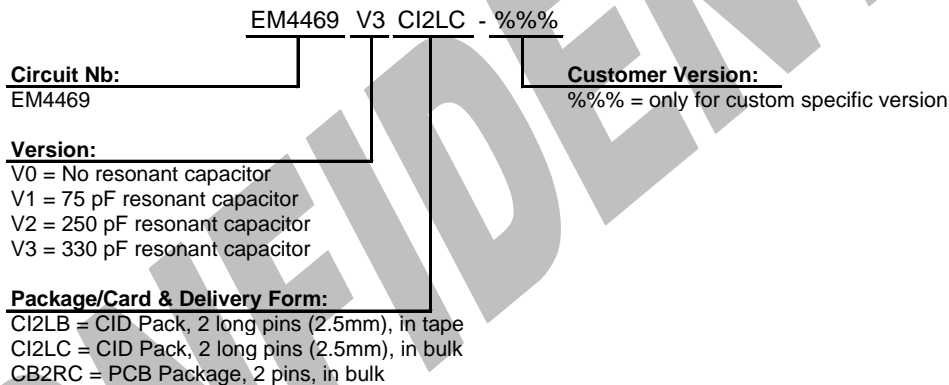
## Ordering Information

These charts shows general offering; for detailed Part Number to order, please see the table "Standard Versions" below.

### Die Form



### Packaged Devices



### Remarks:

- For ordering please use table of "Standard Version" table below.
- For specifications of Delivery Form, including gold bumps, tape and bulk, as well as possible other delivery form or packages, please contact EM Microelectronic-Marín S.A.

### Standard Versions & Samples:

For samples please order exclusively:

Part Number	Capacitor option	Package	Delivery Form
EM4469V3CI2LC	330pF	CID package, 2 pins (length 2.5mm)	bulk
EM4469V3CB2RC	330pF	PCB Package, 2 pins	bulk

The versions below are considered standards and should be readily available. For other versions or other delivery form, please contact EM Microelectronic-Marín S.A.

Part Number	Capacitor option	Package/Die Form	Delivery Form
EM4469V3CB2RC	330pF	PCB Package, 2 pins	bulk
EM4469V3CI2LC	330pF	CID package, 2 pins (length 2.5mm)	bulk
EM4469V3CI2LB	330pF	CID package, 2 pins (length 2.5mm)	tape
EM4469VXXXX-%%%		custom	custom

EM Microelectronic-Marín SA cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in an EM Microelectronic-Marín SA product. EM Microelectronic-Marín SA reserves the right to change the circuitry and specifications without notice at any time. You are strongly urged to ensure that the information given has not been superseded by a more up-to-date version.