2A Sink/Source Bus Termination Regulator

General Description

The EM5049 performs ultra low drop voltage and fast response linear regulator specifically designed to provide termination voltage for DDR memory system. This device works with dual supplies, a control input for the control circuitry and a power input for providing current to output and designed to source/sink up to 2A output current. Output voltage is regulated to track the 1/2 reference voltage within 15mV variation.

The other features include soft start, current limit protection, Power-On-Reset function, and over temperature protection. The EM5049 is available in DFN3X3 package.

Ordering Information

Part Number	Package	Remark
EM5049VT	DFN3X3-10L	

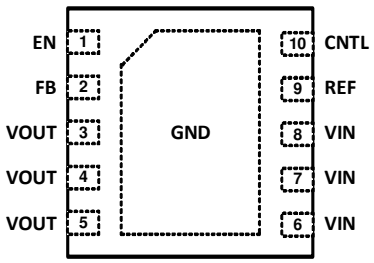
Features

- Termination Voltage for DDRII/DDRIII Memory System
- Stable with Output Ceramic Capacitor
- Excellent Line Regulation
- Excellent Load Regulation
- Output Voltage is Adjustable
- 2A Output Source/Sink Current
- Bidirectional Current Limit Protection
- Over Temperature Protection
- RoHS Compliant and 100% Lead (Pb)-Free

Applications

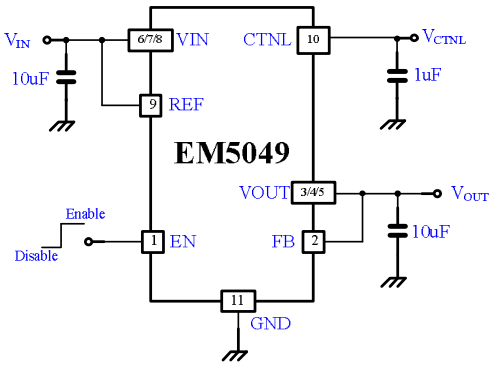
- DDRII/DDRIII Memory Systems
- Notebook & Netbook
- Graphics Card & MB
- Low Voltage Logic Supplies
- SMPS Post Regulators
- Set Top Boxes , Digital TVS , Printers
- Active Termination Buses

Pin Configuration



DFN3x3-10L

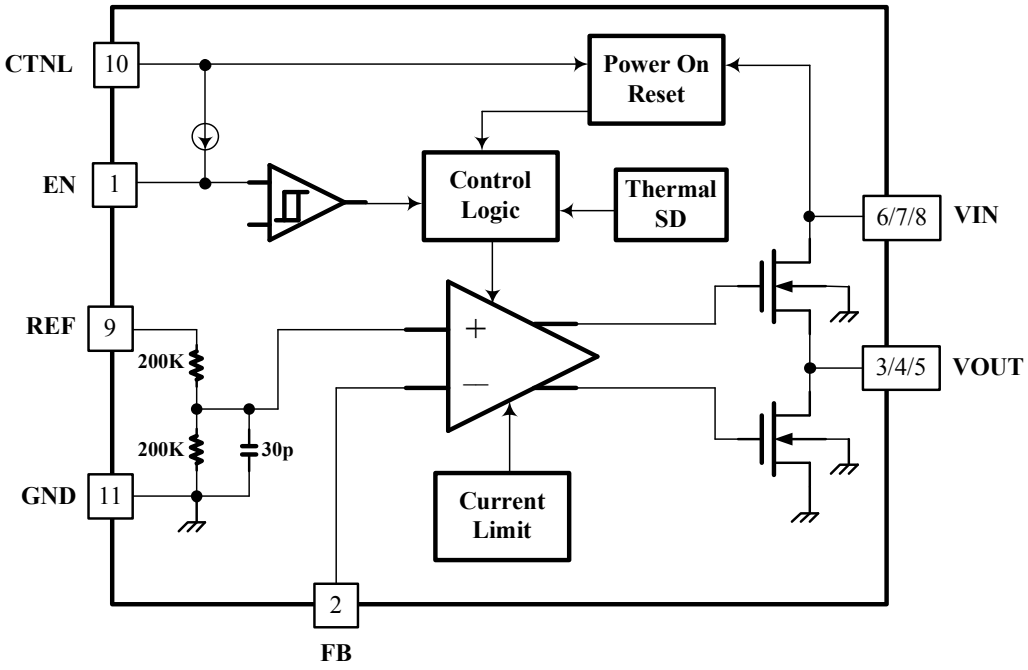
Typical Application Circuit



Pin Assignment

Pin Name	Pin No.	Pin Function
EN	1	**Enable.** Active high control pin. If this pin is floating, an internal pull high current source (3uA typical) will enable the regulator. Pulling the pin below 0.4V turns the regulator off.
FB	2	**Feedback.** The inverting input pin of error amplifier.
VOUT	3,4,5	**Output Voltage.** VOUT is power output pin. Minimum 10uF low ESR ceramic capacitor is required at this pin for stabilizing VOUT voltage.
VIN	6,7,8	**Input Voltage.** This is the drain input to the power device that supplies current to the output pin. Minimum 10uF low ESR ceramic capacitor is recommended at this pin.
REF	9	**Reference Voltage Input.** This pin is the non-inverting input of the error amplifier. The FB voltage is regulated to track the 1/2 reference voltage input.
CNTL	10	**Supply Input for Control Circuit.** CNTL provides supply voltage to the control circuitry and driver for the pass transistor. The driving capability of output current is proportioned to the V_{CNTL}.
GND	11	**GND**

Function Block Diagram



Absolute Maximum Ratings (Note1)

- V_{IN} ---------- -0.3V to +6.0V
- V_{CNTL} ---------- -0.3V to +6.0V
- Other Pins---------- -0.3V to (V_{CNTL}+0.3V)
- Power Dissipation, P_D @ T_A = 25°C, DFN3X3 ---------- 1.67W
- Package Thermal Resistance, Θ_{JA}, DFN3X3 (Note 2)---------- 60°C/W
- Junction Temperature---------- 150°C
- Lead Temperature (Soldering, 10 sec.)---------- 260°C
- Storage Temperature ---------- –65°C to 150°C
- ESD susceptibility (Note3)
  HBM (Human Body Mode)---------- 2KV
  MM (Machine Mode)---------- 200V

Recommended Operating Conditions (Note4)

- Control Voltage, V_{CNTL} ---------- +4.5V to +5.5V
- Supply Input Voltage, V_{IN} ---------- +1V to V_{CNTL}
- Junction Temperature ---------- –40°C to 125°C
- Ambient Temperature ---------- –40°C to 85°C

Electrical Characteristics

V_{CNTL}= 5V, V_{IN}= 1.8V, V_{REFEN}= 0.9V, T_A=25℃, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input CNTL Section						
Control Input Voltage	V_{CNTL}		4.5	-	5.5	V
POR Threshold	V_{PORTH}	V_{CNTL} rising	-	3.6	-	V
POR Hysteresis	V_{PORHYS}		-	0.2	-	V
CNTL Operation Current	I_{CNTL}	I_{OUT}=0A	-	0.7	2	mA
Shutdown Current	I_{SD}	V_{REFEN}=0V	-	20	35	uA
Output Voltage						
Output Offset Voltage	V_{OS}	I_{OUT}=0A	-15	-	15	mV
Load Regulation	ΔV_{LOAD}	I_{OUT} =±2A	-15	-	15	mV
EN Shutdown						
Enable High Level	V_{EN}		1.4	-	-	V
Disable Low Level	V_{SD}		-	-	0.4	V
EN pull-high current	I_{EN}	V_{EN}=GND		3		uA
Internal Soft Start Time	T_{SS}	V_{OUT} 10%~90%	0.1	0.2	0.4	mS
Protection						
OCP Threshold Level	I_{OCP}	Source / Sink	2.1	3.0	4.2	A
Output Short Circuit Current	I_{SC}	Source / Sink	-	1.5	-	A
Thermal Shutdown Temperature	T_{SD}	V_{EN}=V_{IN} , I_{OUT}=0A	-	160	-	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	V_{EN}=V_{IN} , I_{OUT}=0A	-	30	-	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A=25°C on a 4-layers high effective thermal conductivity test board with minimum copper area of JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

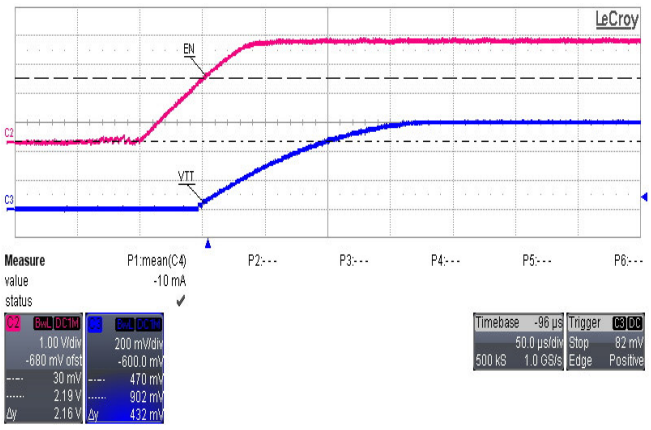
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

V_{CNTL}=5V；C_{IN}=C_{OUT}=10uF

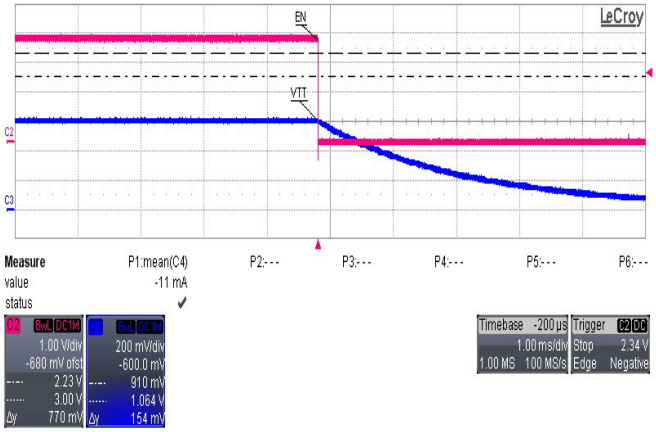
Power On from V_{IN}

V_{IN}=1.2V；V_{OUT}=0.6V



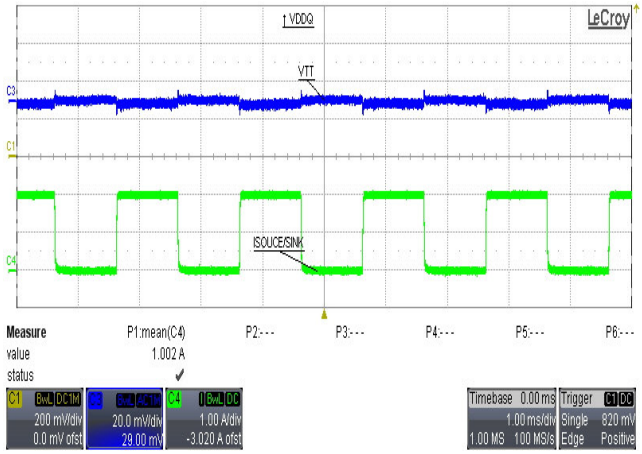
Power Off from V_{IN}

V_{IN}=1.2V；V_{OUT}=0.6V



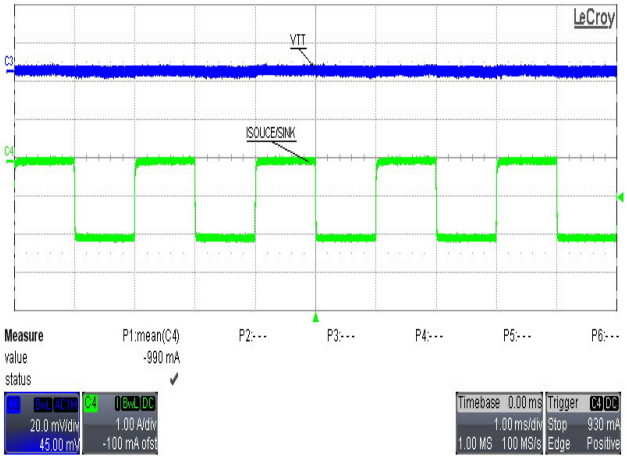
Load Transient for Source Current

V_{IN}=1.2V；V_{OUT}=0.6V



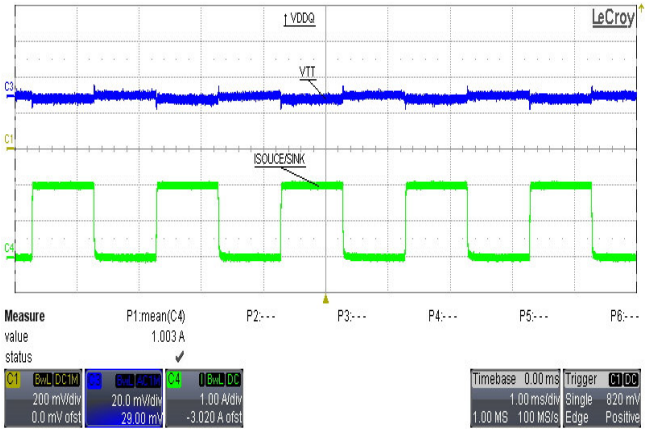
Load Transient for Sink Current

V_{IN}=1.2V；V_{OUT}=0.6V



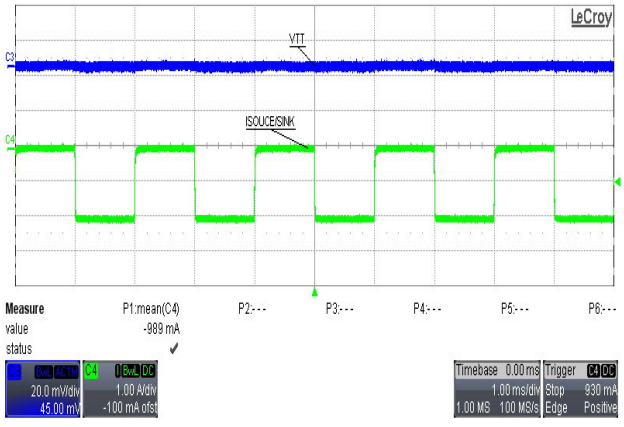
Load Transient For Source Current

V_{IN}=1.5V；V_{OUT}=0.75V



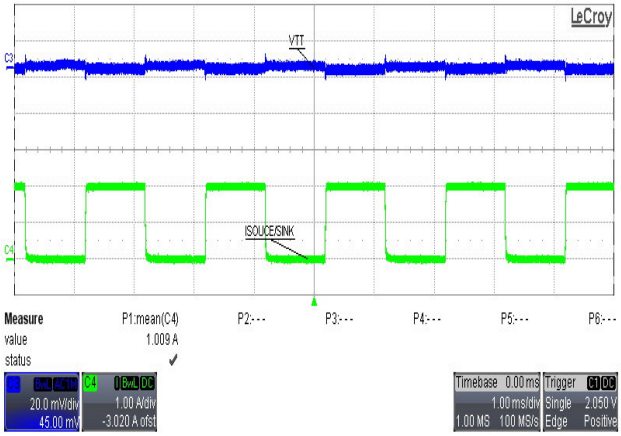
Load Transient for Sink Current

V_{IN}=1.5V；V_{OUT}=0.75V



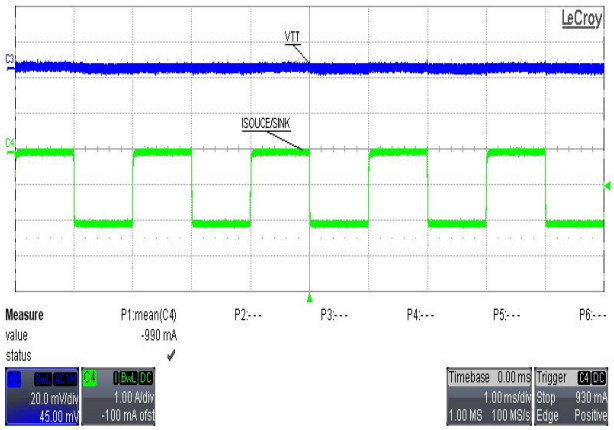
Load Transient for Source Current

V_{IN}=1.8V；V_{OUT}=0.9V

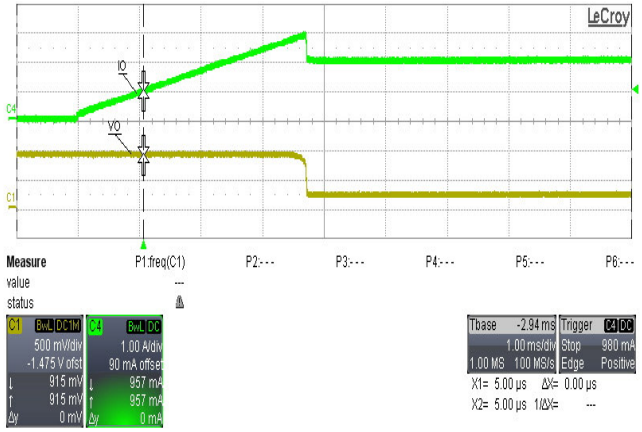


Load Transient for Sink Current

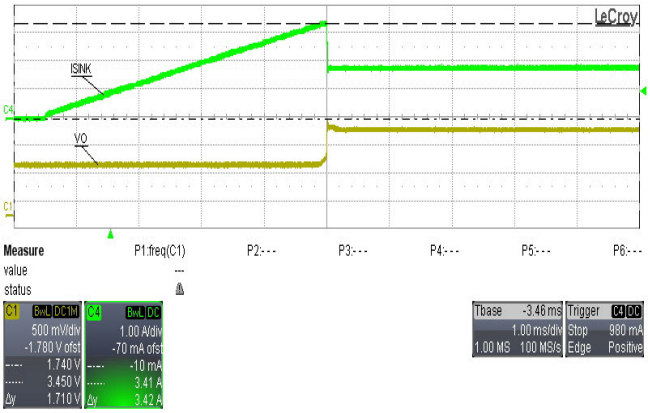
V_{IN}=1.8V；V_{OUT}=0.9V



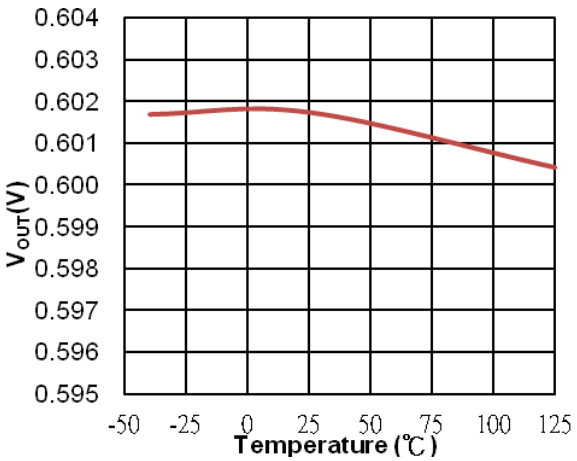
OCP for Source Current



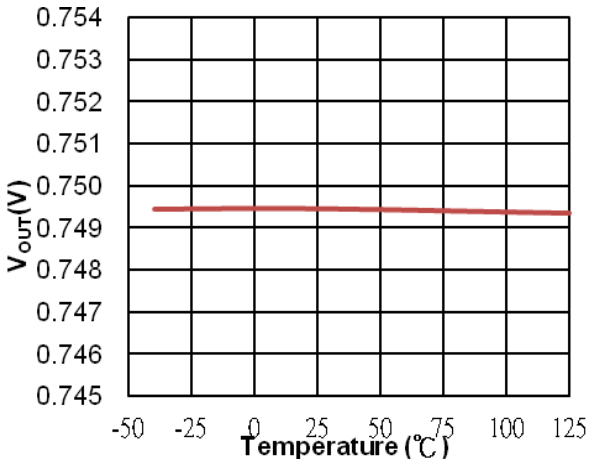
OCP for Sink Current



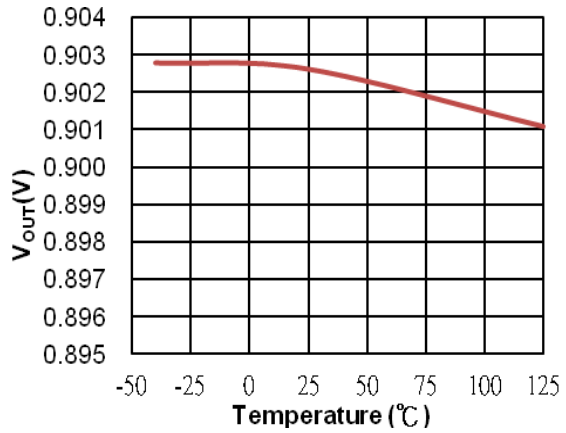
V_{OUT}@0.6V vs. Temperature



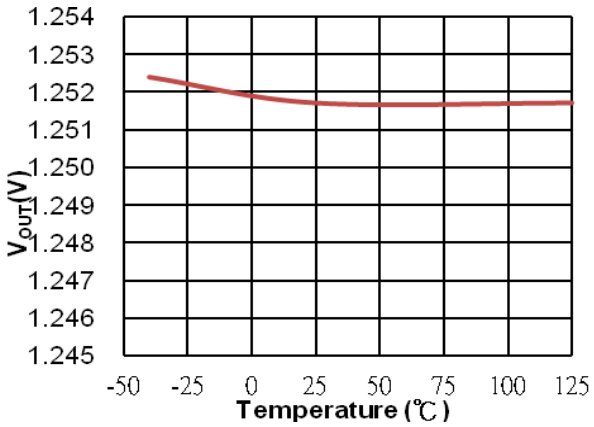
V_{OUT}@0.75V vs. Temperature



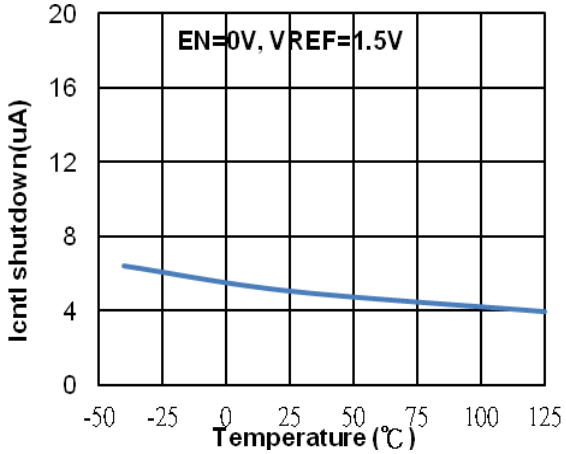
V_{OUT}@0.9V vs. Temperature



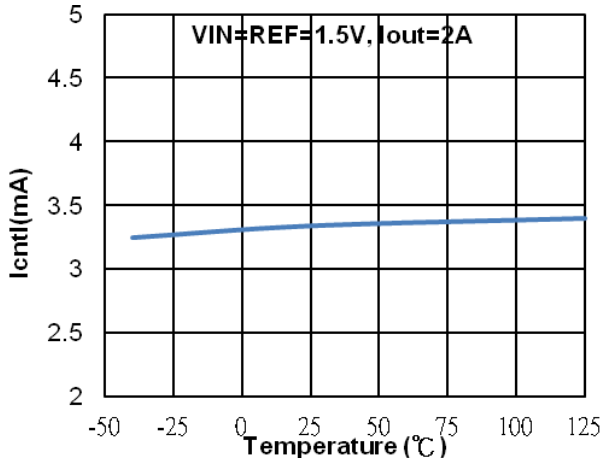
V_{OUT}@1.25V vs. Temperature



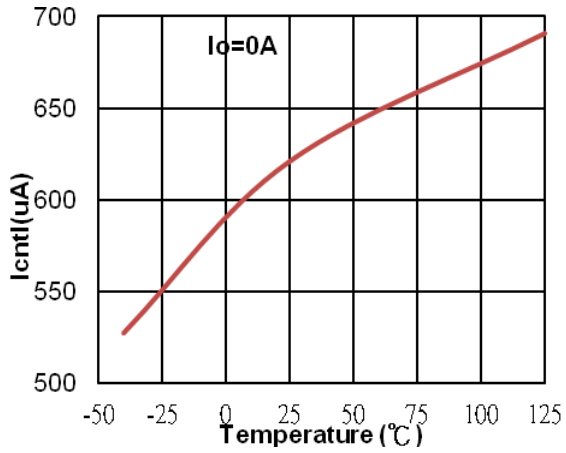
CNTL Shutdown current vs. Temperature



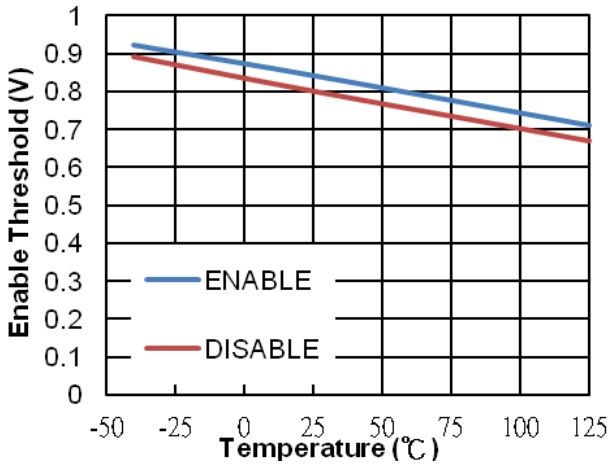
CNTL Current vs. Temperature



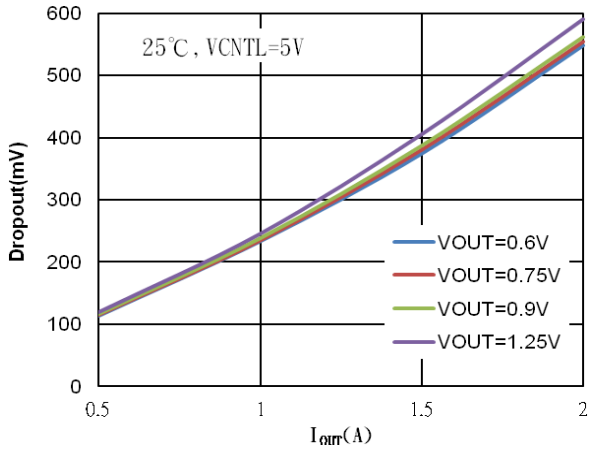
No Load CNTL Current vs. Temperature



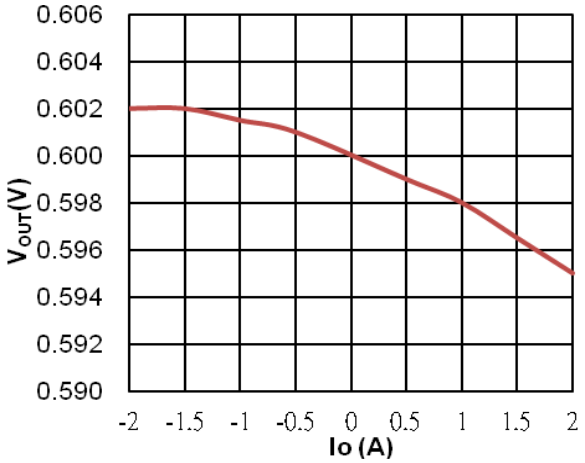
Enable Threshold vs. Temperature



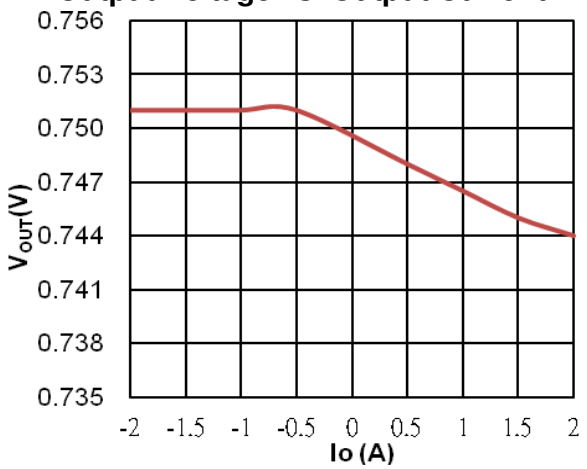
Vo Dropout Voltage vs. Output Current



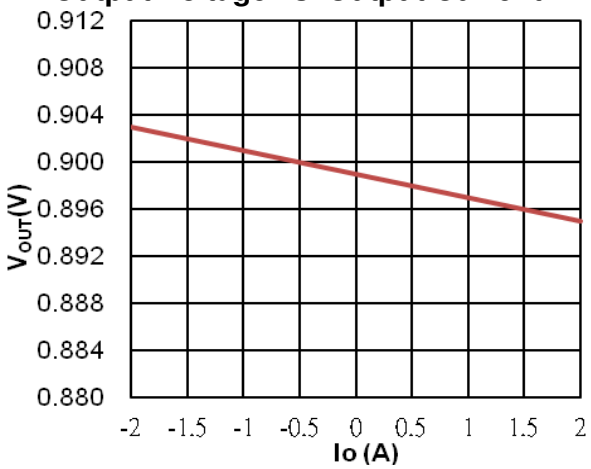
Output Voltage vs. Output Current



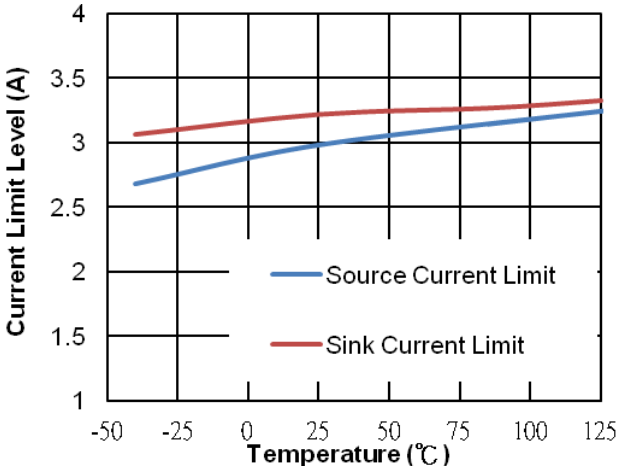
Output Voltage vs. Output Current



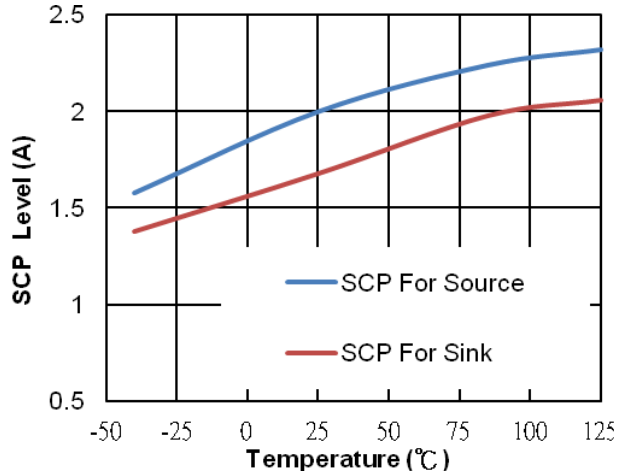
Output Voltage vs. Output Current



Source/Sink Current Limit vs. Temperature



Short protection for Source/Sink vs. Temperature



Functional Description

VO Source/Sink Regulator

The EM5049 integrates a high-performance, high current linear regulator that is capable of both sourcing and sinking current. This regulator employs a fast response so that small ceramic capacitor can be used. To achieve tight regulation with minimum effect of trace resistance, the FB pin should be connected to the positive terminal of the output capacitor.

Reference Input

The output voltage is regulated to track the 1/2 reference voltage at REF pin within ±15mV at all conditions .

Shutdown Control Function

When EN is driven high, the EM5049 Vo regulator begins normal operation. When EN is driven low, VO is discharged to GND through an internal sinking MOSFET.

POR – Power ON Reset

To let EM5049 start to operation, CNTL voltage must be higher than its POR voltage even when REF voltage is pulled higher than enable high voltage. Typical POR voltage is 3.6V.

Over Current Limit Function

EM5049 features over current limiting function as well as output short circuit current fold back function. Typically, before the thermal protection is triggered, EM5049 can limit its output current to 3.0A (TYP). When output voltage is decreased, the limiting current level also decreases. When VOUT is short to GND, or VOUT voltage is zero, the output current level is limited to 1.5A, typically.

Input and Output Capacitor Selection

For CNTL pin, a 1uF ceramic capacitor is enough for bypass the supply of CNTL to GND. For VIN pin, 10uF or larger ceramic capacitor is required to provide bypass path in transient current demand. VOUT pin is also recommended to have 10uF or larger ceramic capacitor to be stable and reduce the VOUT voltage dip when fast loading transient is happened.

Power Dissipation

The maximum power depends on some conditions, including of thermal impedance, PCB layout, airflow, and so on. The maximum power dissipation can be calculated by the formula as below

$P_{D(max)}=(T_{J(max)}-T_A) / \theta_{JA}$

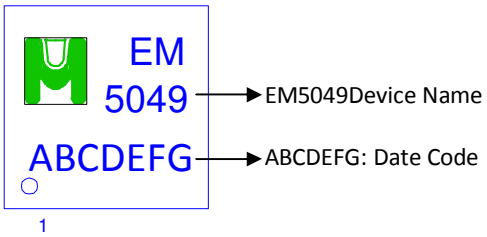
$T_{J(max)}$ is the maximum, junction temperature; θ_{JA} is the thermal impedance from junction to ambient. The thermal impedance θ_{JA} of exposed DFN3X3-10L is package design and PCB design dependent. The thermal impedance can be reduced by increasing the copper area under the exposed pad of the DFN3X3-10L package. So, to let the copper area as large as possible is helpful for the thermal performance of the DFN3X3-10L package.

For recommended specification of EM5049, the maximum junction temperature is 125 degree C. The θ_{JA} of exposed DFN3X3-10L is 60°C/W on the standard JEDEC 51-7(4 layers, 2S2P, copper 2 oz) thermal test board. The maximum power dissipation (at 25°C ambient, on the minimum exposed pad layout) can be calculated as below:

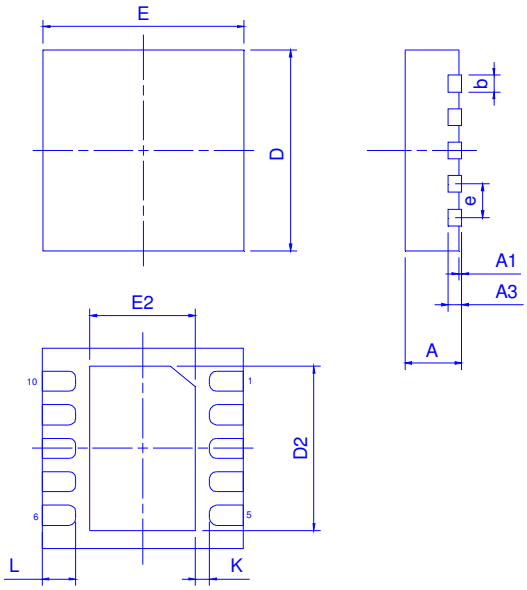
$P_{D(max\ at\ 25°C)}=(125°C–25°C)/(60°C/W) = 1.67W$

Marking Information

Device Name: EM5049VT for DFN3X3-10L



Outline Drawing



Dimension in mm

Dimension	A	A1	A3	b	D	E	D2	E2	e	L	K
Min.	0.7	0.00		0.18			2.20	1.40		0.30	0.20
Typ.	0.75	0.02	0.2	0.25	3.0	3.0			0.50	0.40	
Max.	0.80	0.05		0.30			2.70	1.75		0.50	