3A Low Dropout LDO

General Description

EM5103 is a 3A low dropout linear regulator designed for low dropout and high current applications. This device works with dual supplies, a control input for the control circuitry and a power input as low as 1.2V for providing current to output. It features 3A output current and ultra-low-drop output voltage as well as full protection functions. V_{OUT} can be as low as 0.8V.

Ordering Information

Part Number	Package	Remark
EM5103GE	PSOP-8 Lead-Free	
EM5103VT	DFN3X3-10L Lead-Free	

Features

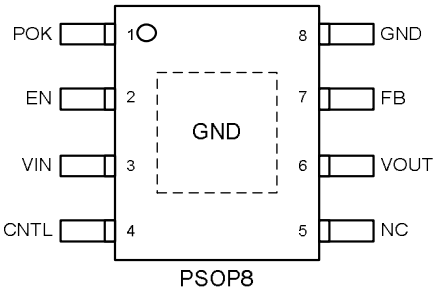
- V_{IN} Range 1.2V to 5.5V
- V_{OUT} is Adjustable (0.8V Min)
- Excellent Line Regulation
- Excellent Load Regulation
- 3A Guaranteed Output Current*
- 300mV @ 3A Dropout Voltage
- OTP and OCP Functions
- Very Low On-Resistance
- Enable & Power good Signal

*Check thermal design information.

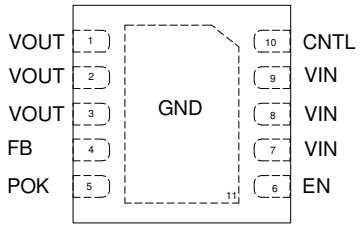
Applications

- Notebook & Netbook
- Graphic Cards & MB
- Low Voltage Logic Supplies
- Chipset Supplies
- Server System
- SMPS Post Regulators

Pin Configuration



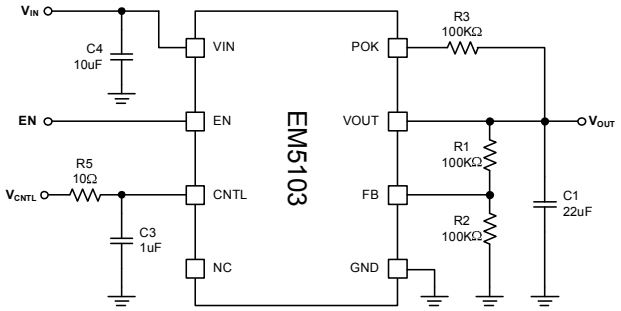
PSOP8



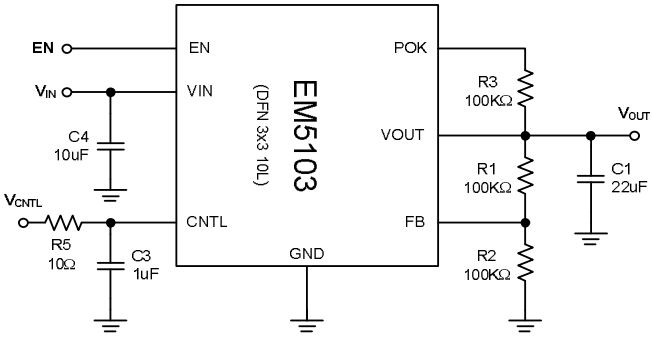
DFN3x3-10L

Typical Application Circuit

PSOP8



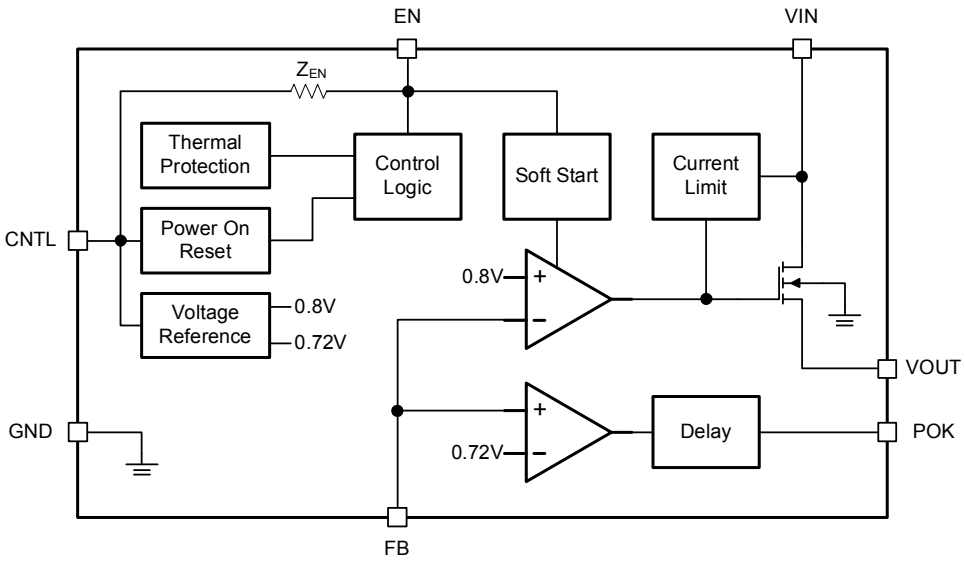
DFN3X3-10L



Pin Assignment

Pin Name	Pin No.		Pin Function
	PSOP8	DFN3X3-10L	
POK	1	5	**Power OK Indication.** POK is an open-drain output. An external pull high resistor connected to this pin is required.
EN	2	6	**Enable Input.** Pulling the pin below 0.4V turns the regulator off
VIN	3	7,8,9	**Input Voltage.** This is the drain input to the power device that supplies current to the output pin. V_{IN} cannot be forced higher than $V_{CNTL.}$
CNTL	4	10	**Supply Input for Control Circuit.** CNTL provides supply voltage to the control circuitry and driver for the pass transistor. The driving capability of output current is proportioned to the V_{CNTL}. For the device to regulate, the voltage on this pin must be at least 2.0V greater than the output voltage, and no less than V_{CNTL_MIN}.
NC	5	-	**No Connection inside chip.**
VOUT	6	1,2,3	**Output Voltage.** V_{OUT} is power output pin. An internal pull low resistance exists when the device is disabled. Minimum 22uF low ESR ceramic holding capacitor is required at this pin for stabilizing V_{OUT} voltage.
FB	7	4	**Feedback Voltage.** FB is the inverting input to the error amplifier. A resistor divider from the output to GND is used to set the regulation voltage as V_{OUT} = (1 + R1/R2) x 0.8V (V). This pin has high impedance and should be kept from noisy source to guarantee stable operation.
GND	8	11	**Ground.**

Function Block Diagram



Absolute Maximum Ratings (Note1)

- V_{IN} ---------- -0.3V to +6V
- V_{CNTL} (Note 1) ---------- -0.3V to +6V
- Other Pins ---------- -0.3V to (V_{CNTL}+0.3V)
- Package Thermal Resistance,θ_{JA},
  - PSOP8 (Note 2) ---------- 75°C/W
  - DFN3X3-10L ---------- 60°C/W
- Power Dissipation, PD @ TA = 25°C,
  - PSOP8 (Note 3) ---------- 1.9W
  - DFN3X3-10L ---------- 1.67W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature ---------- -65°C to +150°C
- ESD susceptibility (Note4)
- HBM (Human Body Mode) ---------- 2KV
- MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note5)

- Supply Input Voltage, V_{IN} ---------- 1.0V to V_{CNTL}
- Control Voltage, V_{CNTL} ---------- 3.0V to 5.5V
- Junction Temperature ---------- -40°C to 125°C
- Ambient Temperature ---------- -40°C to 85°C

Electrical Characteristics

V_{CNTL}=5V, T_A=25°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input Section						
Control Input Voltage	V_{CNTL}	V_{OUT}= V_{REF}	3.0	-	5.5	V
POR Threshold	$V_{CNTLRTH}$		-	2.7	-	V
POR Hysteresis	$V_{CNTLHYS}$		-	0.2	-	V
Power Input Voltage	V_{IN}	V_{OUT}=V_{REF}	1.0	-	V_{CNTL}	V
Control Input Current in Shutdown	I_{CNTL_SD}	V_{IN}=V_{CNTL}=5V, I_{OUT}=0A,V_{EN}=0V	-	10	30	uA
Quiescent Current	I_Q	V_{IN}=V_{CNTL}=V_{EN}=5V, I_{OUT}=0A, V_{OUT}=V_{REF}	-	0.9	1.5	mA
Feedback						
Reference Voltage	V_{REF}	V_{IN}=V_{CNTL}=V_{EN}=5V, I_{OUT}=0A, V_{OUT}=V_{REF}	0.788	0.8	0.812	V
Feedback Input Current	I_{FB}		-	5	-	nA
V_{IN} Line Regulation	$V_{REF(LINE)}$	1.2V<V_{IN}<5V, V_{CNTL}=V_{EN}=5V, I_{OUT}=0A, V_{OUT}=V_{REF}	-	0.01	0.1	%/V
Load Regulation (Note 6)	$V_{REF(LOAD)}$	10mA<I_{OUT}<3A, V_{IN}=V_{CNTL}=V_{EN}=5V, V_{OUT}=V_{REF}	-	0.8	1.5	%/A
Load Regulation over Temperature	$V_{REF(TOTAL)}$	10mA<I_{OUT}<3A, V_{IN}=V_{CNTL}=V_{EN}=5V, V_{OUT}=V_{REF}, -40°C<T_j<125 °C by design	-	-	3	%

Dropout Voltage (Note 7)	V_{DROP}	I_{OUT}=2A, V_{CNTL}=V_{EN}=5V, V_{OUT}= V_{REF}	-	200	240	mV
		I_{OUT}=3A, V_{CNTL}=V_{EN}=5V, V_{OUT}=V_{REF}	-	300	360	mV
Output Voltage	V_{OUT}		0.8	-	V_{CNTL}-2	V
V_{OUT} Pull Low Resistance		V_{IN}=V_{CNTL}=5V, V_{EN}=0V	-	70	-	Ω
Enable						
Enable High Level	V_{EN}		1.4	-	-	V
Disable Low Level	V_{SD}		-	-	0.4	V
Enable Source Current	I_{EN}	V_{CNTL}=5V, V_{EN}=0V	-	7	18	μA
Enable Input Impedance	Z_{EN}		-	700	-	KΩ
Output Voltage Ramp Up Time			1.5	2.5	4.5	ms
PWROK						
FB Power OK Threshold	V_{POKTH}	V_{IN}=V_{CNTL}=V_{EN}=5V, I_{OUT}=0A, V_{OUT}=V_{REF}	-	90	-	%
Power OK Hysteresis	V_{POKHYS}	V_{IN}=V_{CNTL}=V_{EN}=5V, I_{OUT}=0A, V_{OUT}=V_{REF}	-	8	-	%
POK Delay Time		From V_{OUT}>90% to POK rising	0.5	1.0	2.0	ms
Over Current Protection						
OCP Threshold Level	I_{OCP}	V_{IN}=V_{CNTL}=V_{EN}=5V, V_{OUT}=V_{REF}	3.2	4.0	-	A
Output Short Circuit Current	I_{SC}	V_{IN}=V_{CNTL}=V_{EN}=5V, V_{OUT}=0V	1.5	2.5	-	A
Thermal Protection						
Thermal Shutdown Temperature	T_{SD}	V_{IN}=V_{CNTL}=V_{EN}=5V, I_{OUT}=0A, V_{OUT}=V_{REF}	-	160	-	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	V_{IN}=V_{CNTL}=V_{EN}=5V, I_{OUT}=0A, V_{OUT}=V_{REF}	-	30	-	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A=25°C on a 4-layers high effective thermal conductivity test board with minimum copper area of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the expose pad for PSOP-8 package.

Note 3. θ_{JA} PSOP-8 packages is 52°C /W on JEDEC 51-7 (4 layers,2S2P) thermal test board with 50mm^2 copper area.

Note 4. Devices are ESD sensitive. Handling precaution is recommended.

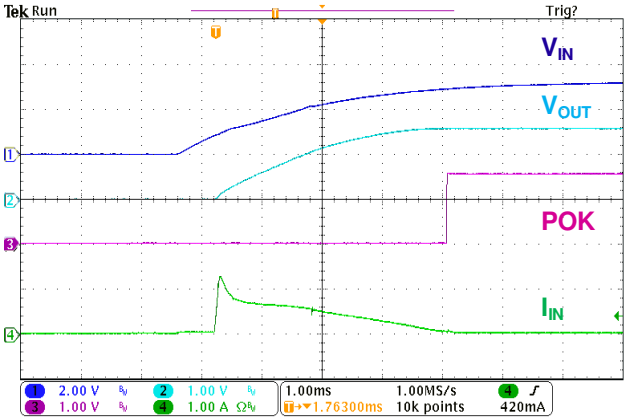
Note 5. The device is not guaranteed to function outside its operating conditions.

Note 6. Load regulation is measured by a current pulse with 50Hz frequency and 10% duty cycle.

Note 7. The dropout voltage is defined as (V_{IN}-V_{OUT}), which is measured when V_{OUT} equal to ($V_{OUT,(NORMAL)}$-100mV).

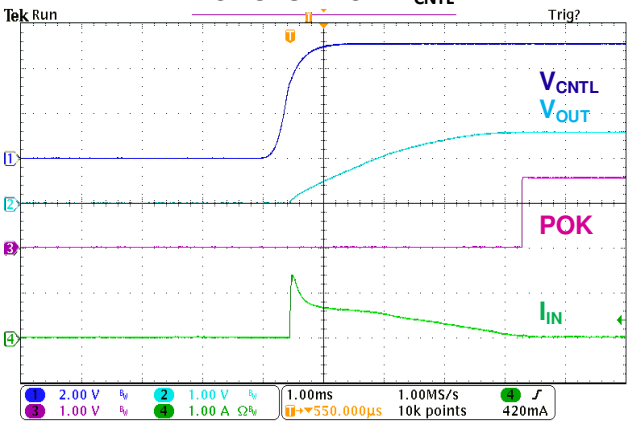
Typical Operating Characteristics

Power On from V_{IN}



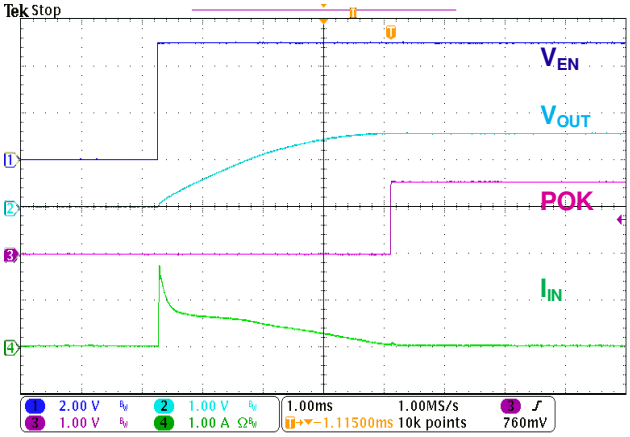
V_{CNTL}=5V，V_{IN}=3.3V，C_{OUT}=1000uF，No Load.

Power On from V_{CNTL}



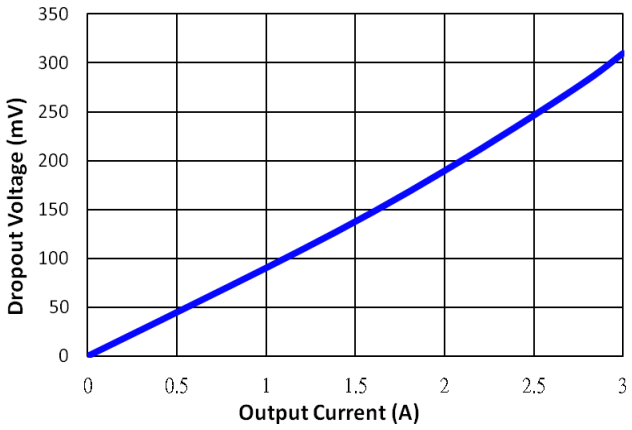
V_{CNTL}=5V，V_{IN}=3.3V，C_{OUT}=1000uF，No Load.

Turn On from EN



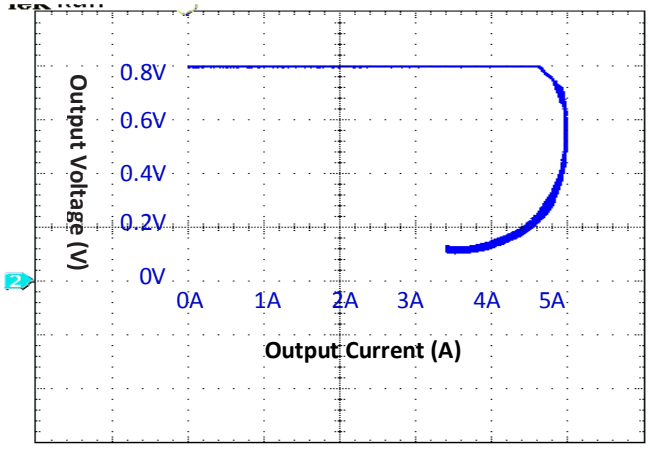
V_{CNTL}=5V，V_{IN}=3.3V，C_{OUT}=1000uF，No Load.

Dropout Voltage vs. Output Current



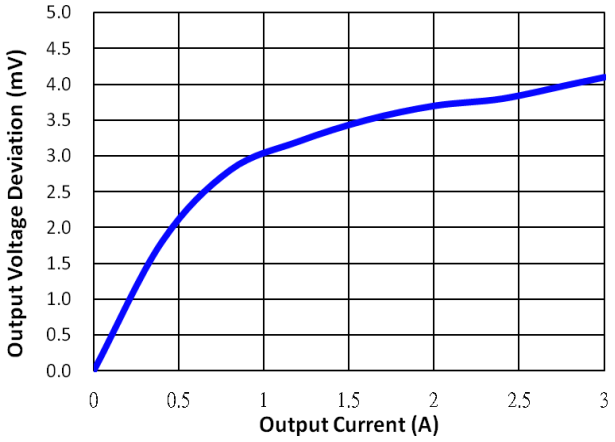
V_{CNTL}=5V，V_{OUT}=1.6V.

Output Short Circuit



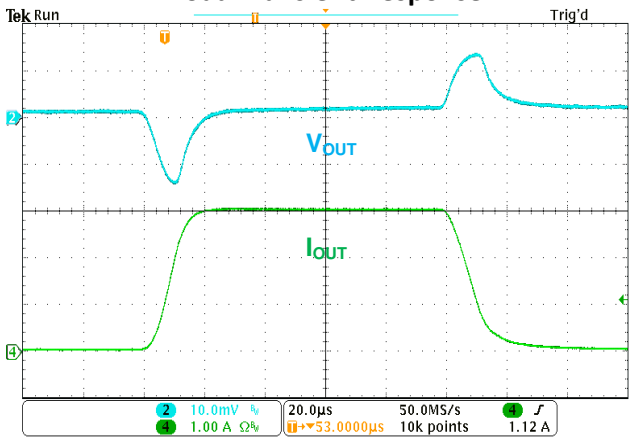
V_{IN}=V_{CNTL}=5V，V_{OUT}=V_{REF}.

Output Voltage vs. Output Current



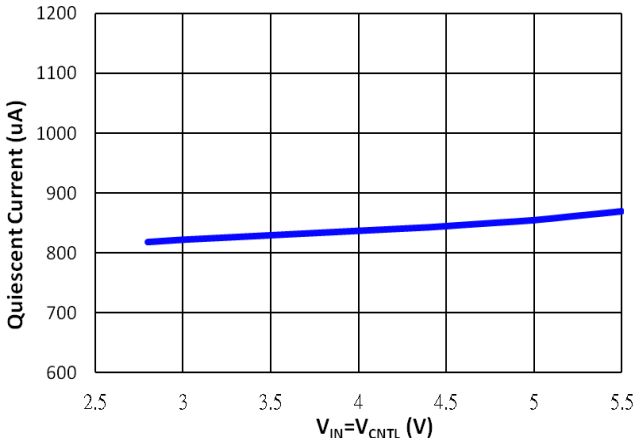
V_{IN}=V_{CNTL}=5V，V_{OUT}=1.0V.

Load Transient Response



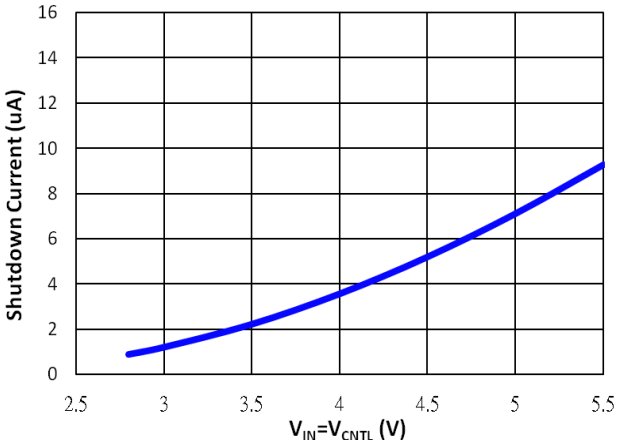
V_{CNTL}=5V，V_{IN}=3.3V，C_{OUT}=22uF.

Quiescent Current vs. Input Voltage



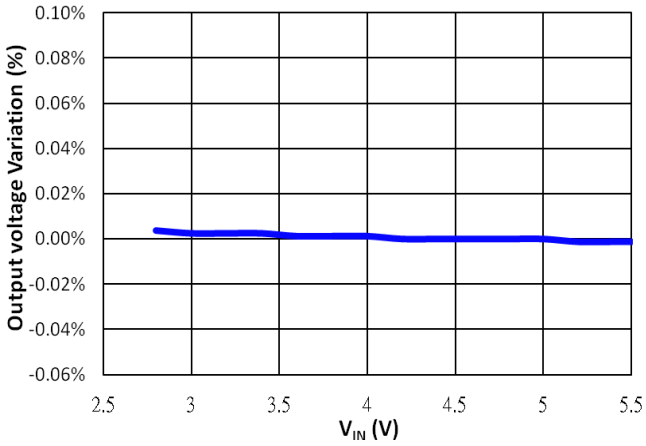
V_{OUT}=V_{REF}.

Shutdown Current vs. Input Voltage



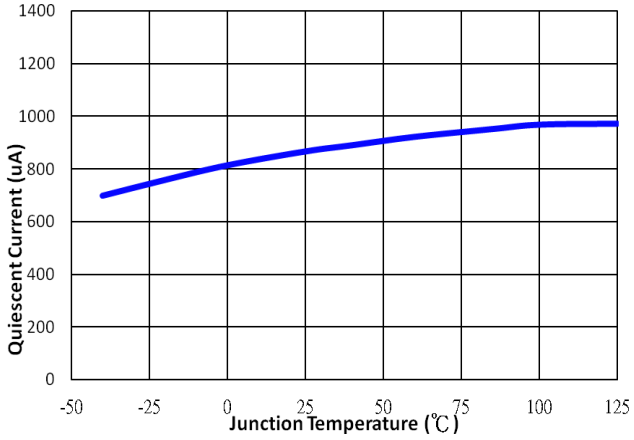
V_{OUT}=V_{REF}

Line Regulation



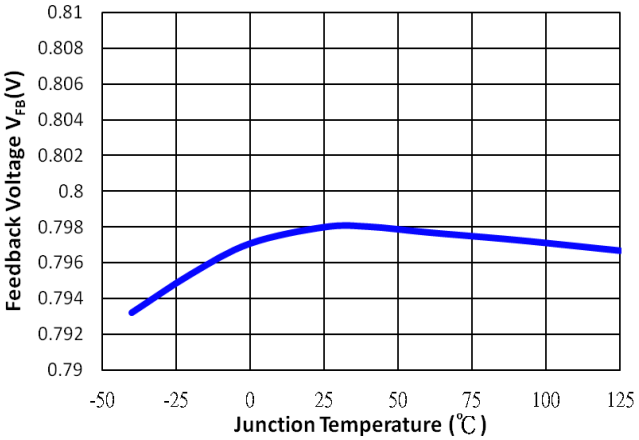
V_{CNTL}=5V，V_{OUT}=V_{REF}.

Quiescent Current vs. Temperature

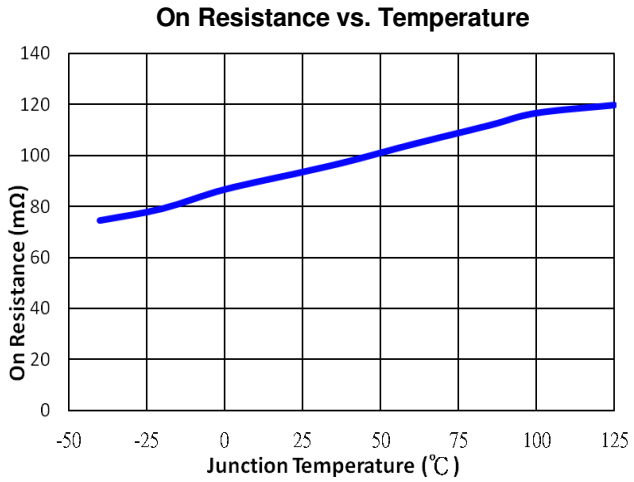


V_{IN}=V_{CNTL}=5V，V_{OUT}=V_{REF}.

FB Voltage vs. Temperature



V_{IN}=V_{CNTL}=5V，V_{OUT}=V_{REF}.



V_{CNTL}=5V，V_{OUT}=1.6V.

Functional Description

Enable Function

EM5103 is enabled if the voltage of the EN pin is greater than 1.4V. If the voltage of the EN pin is less than 0.4V, the IC will be disabled. The quiescent current can be decreased to be less than 10uA typically.

POR – Power ON Reset

To let EM5103 start to operation, CNTL voltage must be higher than its POR voltage even when EN voltage is pulled higher than enable high voltage. Typical POR voltage is 2.7V.

VOUT Voltage Adjustment

The VOUT voltage of EM5103 can be adjusted by external voltage divider. Refer to typical application circuit, VOUT voltage is calculated by the following equation,

V_{OUT} = (1 + R1/R2) x 0.8V

Over Current Limit Function

EM5103 features over current limiting function as well as output short circuit current fold back function. Typically, before the thermal protection is triggered, EM5103 can limit its output current to 4.0A. When output voltage is decreased, the limiting current level also decreases. When VOUT is short to GND, or VOUT voltage is zero, the output current level is limited to 2.5A, typically.

Input and Output Capacitor Selection

For CNTL pin, a 1uF ceramic capacitor is enough for bypass the supply of CNTL to GND. For VIN pin, 10uF or larger ceramic capacitor is required to provide bypass path in transient current demand. VOUT pin is also recommended to have 22uF or larger ceramic capacitor to be stable and reduce the VOUT voltage dip when fast loading transient is happened. A feed-forward capacitor can be placed between VOUT and FB pin to speed up the transient response, optionally.

Power Dissipation

The max power depends on some conditions, including of thermal impedance, PCB layout, airflow, and so on. The max power dissipation can be calculated by the formula as below

$P_{D(max)}=(T_{J(max)}-T_A) / \theta_{JA}$

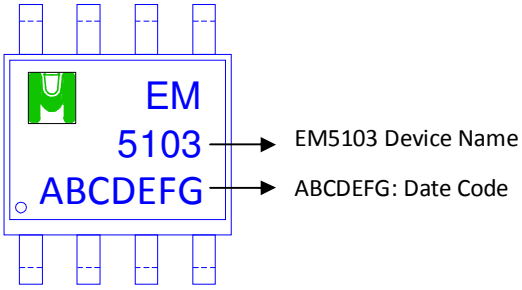
$T_{J(max)}$ is the max junction temperature; θ_{JA} is the thermal impedance from junction to ambient. The thermal impedance θ_{JA} of exposed SOP-8 is package design and PCB design dependent. The thermal impedance can be reduced by increasing the copper area under the exposed pad of the SOP-8 package. So, to let the copper area as large as possible is helpful for the thermal performance of the exposed SOP-8 package.

For recommended specification of EM5103, the max junction temperature is 125 degree C. The θ_{JA} of exposed SOP-8 is 75°C/W on the standard JEDEC 51-7(4 layers, 2S2P, copper 2 oz) thermal test board. The max power dissipation (at 25°C ambient, on the min exposed pad layout) can be calculated as below:

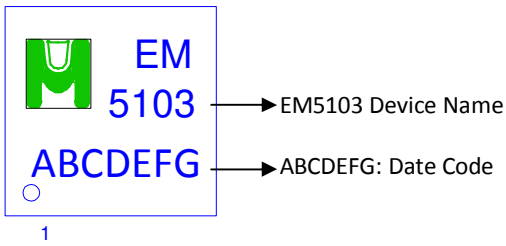
$P_{D(max\ at\ 25°C)}$=(125°C–25°C)/(75°C/W) = 1.33W

Ordering & Marking Information

Device Name: EM5103GE for PSOP-8

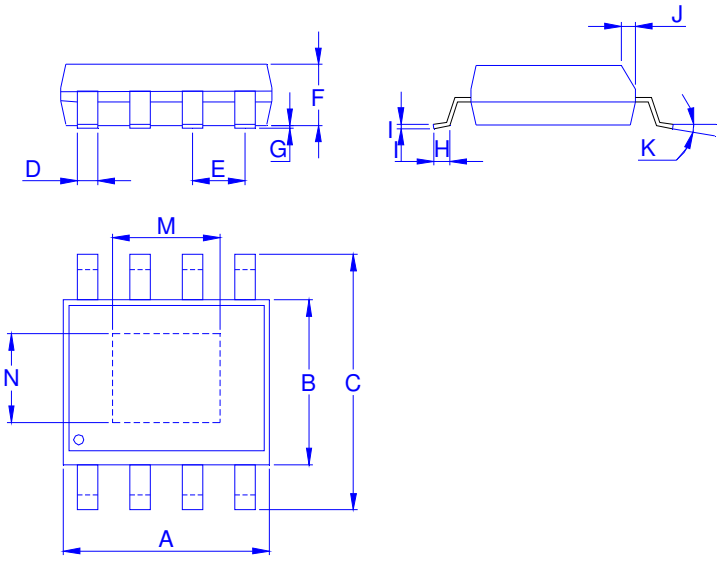


Device Name: EM5103VT for DFN3X3-10L



Outline Drawing

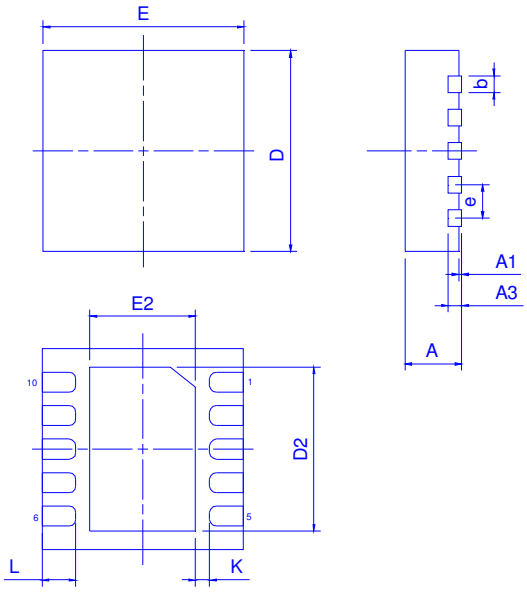
SOP-8 EP



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K	M	N
Min.	4.70	3.70	5.80	0.33		1.20	0.02	0.40	0.19	0.25	0°	1.94	1.94
Typ.					1.27								
Max.	5.10	4.10	6.20	0.51		1.62	0.15	0.83	0.26	0.50	8°	2.49	2.49

DFN3X3-10L



Dimension in mm

Dimension	A	A1	A3	b	D	E	D2	E2	e	L	K
Min.	0.7	0.00		0.18			2.20	1.40		0.30	0.20
Typ.	0.75	0.02	0.2	0.25	3.0	3.0			0.50	0.40	
Max.	0.80	0.05		0.30			2.70	1.75		0.50	