NanoAmp Solutions, Inc.
1982 Zanker Road, San Jose, CA 95112
ph: 408-573-8878, FAX: 408-573-8877
www.nanoamp.com

EM512D16

512Kx16 bit Ultra-Low Power Asynchronous Static RAM

Overview

The EM512D16 is an integrated memory device containing a low power 8 Mbit Static Random Access Memory organized as 524,288 words by 16 bits. The base design is the same as NanoAmp's standard low voltage version, EM512W16. The device is fabricated using NanoAmp's advanced CMOS process and high-speed/ultra low-power/ low-voltage circuit technology. The device pinout is compatible with other standard 512K x 16 SRAMs. The device is designed such that a creative user can improve system power and performance parameters through use of it's unique page mode operation.

FIGURE 1: Pin Configuration

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	CE2
B	I/O_8	$\overline{UB}$	A_3	A_4	$\overline{CE1}$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SS}	I/O_{11}	A_{17}	A_7	I/O_3	V_{CC}
E	V_{CCQ}	I/O_{12}	NC	A_{16}	I/O_4	V_{SS}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	A_{18}	A_8	A_9	A_{10}	A_{11}	NC

48 Pin BGA (top)

Features

- **Dual Voltage for Optimum Performance:**
  Vccq - 2.3 to 3.6 Volts
  Vcc - 1.7 to 2.2 Volts
- **Extended Temperature Range:**
  -40 to +85 ^{o}C
- **Fast Cycle Time:**
  Random Access < 70 ns
  Page Mode < 25 ns
- **Very Low Operating Current:**
  I_{CC} < 5 mA typical at 2V, 10 Mhz
- **Very Low Standby Current:**
  I_{SB} < 2 uA @ 55 ^{o}C
- **16 Word Fast Page-Mode Operation**
- **48-Pin BGA or Known Good Die available**

TABLE 1: Pin Descriptions

Pin Name	Pin Function
A_0-A_{18}	Address Inputs
$\overline{WE}$	Write Enable Input
CE1, CE2	Chip Enable Inputs
$\overline{OE}$	Output Enable Input
$\overline{UB}$	Upper Byte Enable Input
LB	Lower Byte Enable Input
I/O_0-I/O_{15}	Data Inputs/Outputs
V_{CC}	Power
V_{CCQ}	Power I/O pins only
V_{SS}	Ground
NC	Not Connected

FIGURE 1: Typical Operating Envelope (Serial R/W Mix)

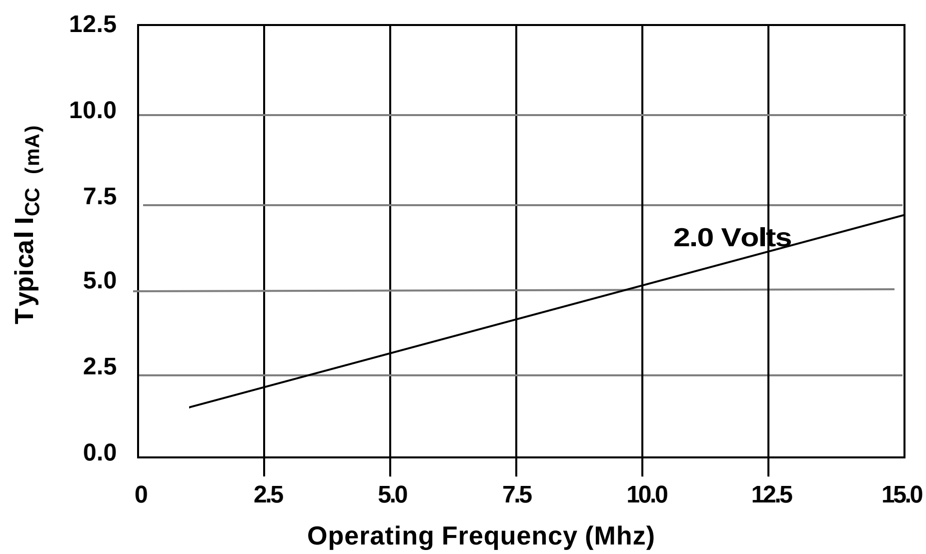


FIGURE 3: Functional Block Diagram

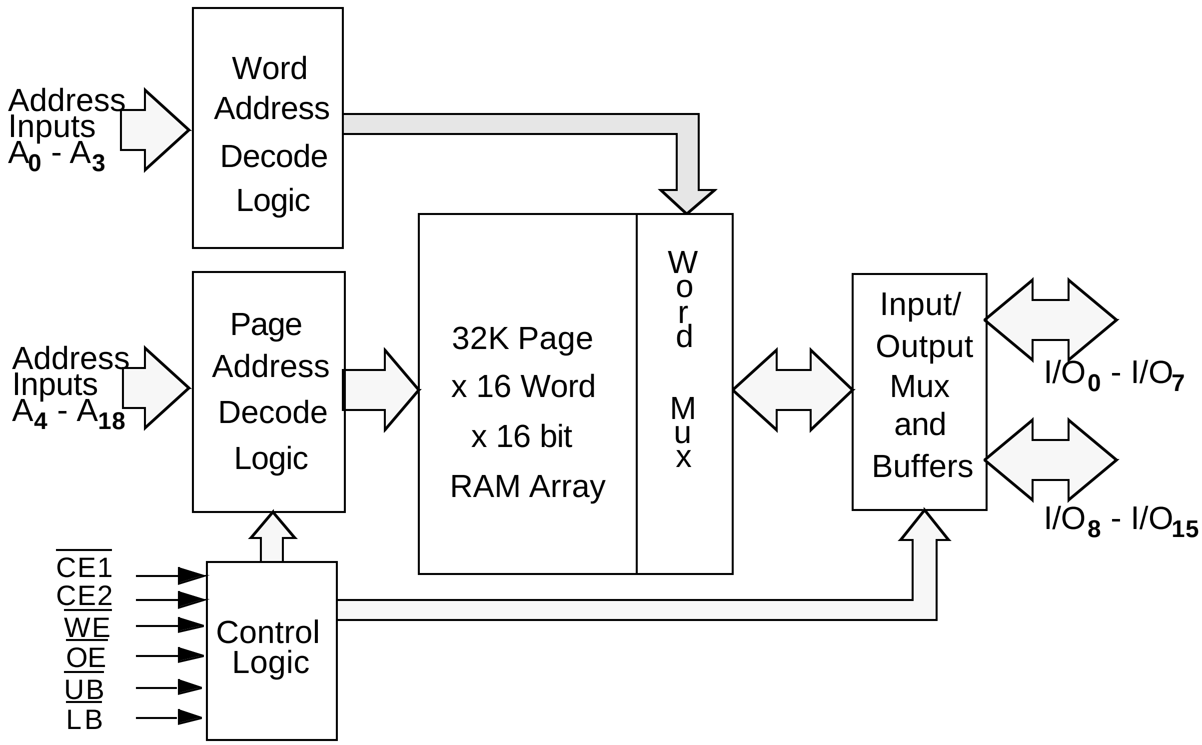


TABLE 2: Functional Description

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	I/O_0 - I/O_{15} [1]	MODE	POWER
H	X	X	X	X	X	High Z	Standby[2]	Standby
X	L	X	X	X	X	High Z	Standby[2]	Standby
X	X	X	X	H	H	High Z	Standby[2]	Standby
L	H	L	X[3]	L[1]	L[1]	Data In	Write[3]	Active
L	H	H	L	L[1]	L[1]	Data Out	Read	Active
L	H	H	H	L[1]	L[1]	High Z	Active	Active

1. When $\overline{UB}$ and $\overline{LB}$ are in select mode (low), I/O_0 - I/O_{15} are affected as shown. When $\overline{LB}$ only is in the select mode only I/O_0 - IO_7 are affected as shown. When $\overline{UB}$ is in the select mode only I/O_8 - I/O_{15} are affected as shown. If both $\overline{UB}$ and $\overline{LB}$ are in the deselect mode (high), the chip is in a standby mode.
2. When the device is in standby mode, control inputs ($\overline{WE}$, $\overline{OE}$, $\overline{UB}$, and $\overline{LB}$), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.
3. When $\overline{WE}$ is invoked, the $\overline{OE}$ input is internally disabled and has no effect on the circuit.

TABLE 3: Capacitance*

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0V$, f = 1 MHz, $T_A = 25^oC$		8	pF
I/O Capacitance	$C_{I/O}$	$V_{IN} = 0V$, f = 1 MHz, $T_A = 25^oC$		8	pF

Note: These parameters are verified in device characterization and are not 100% tested

TABLE 4: Absolute Maximum Ratings*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.3 to V_{CC}+0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.3 to 3.0	V
Storage Temperature	T_{STG}	–40 to 125	^oC
Operating Temperature	T_A	–-40 to +85	^oC

* Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 5: Operating Characteristics (Over specified Temperature Range)

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		1.7		2.2	V
Supply Voltage I/O Only	V_{CCQ}		2.3		3.6	V
Minimum Data Retention Voltage	V_{DR}	Chip Disabled (Note 2)	1.2			V
Input High Voltage	V_{IH}		0.7V_{CC}		V_{CC}+0.5	V
Input Low Voltage	V_{IL}		–0.5		0.3V_{CC}	V
Output High Voltage	V_{OH}	I_{OH} = 0.2mA	V_{CC}–0.2			V
Output Low Voltage	V_{OL}	I_{OL} = -0.2mA			0.2	V
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}			0.5	uA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH} or Chip Disabled			0.5	uA
Read/Write Operating Supply Current @ 1 uS Cycle Time	I_{CC1}	VCC=2.2 V, V_{IN}=V_{IH} or V_{IL} Chip Enabled, IOL = 0			2.0	mA
Random Access Operating Supply Current @ 70 nS Cycle Time	I_{CC2}	VCC=2.2 V, V_{IN}=V_{IH} or V_{IL} Chip Enabled, IOL = 0			15.0	mA
Page Mode Operating Supply Current @ 25 nS Cycle Time	I_{CC2}	VCC=2.2 V, V_{IN}=V_{IH} or V_{IL} Chip Enabled, IOL = 0			7.0	mA
Read/Write Quiescent Operating Supply Current (Note 2)	I_{CC3}	V_{IN} = V_{CC} or 0V Chip Enabled, IOL = 0 f = 0, t_A= 85^{o}C, VCC = 3.6 V			2.0	mA
Operating Standby Current (Note 2)	I_{SB1}	V_{IN} = V_{CC} or 0V Chip Disabled t_A= 55^{o}C, VCC = 2.2 V			2	uA
Maximum Standby Current (Note 2)	I_{SB2}	V_{IN} = V_{CC} or 0V Chip Disabled t_A= 85^{o}C, VCC = 2.2 V			20	uA
Maximum Data Retention Current (Note 2)	I_{DR}	Vcc = 1.2V, V_{IN} = V_{CC} or 0 Chip Disabled, t_A= 85^{o}C			5	uA

1. This device assumes a standby mode if the chip is disabled ($\overline{CE1}$ high or CE2 low). It will also go into a standby mode whenever if both $\overline{UB}$ and $\overline{LB}$ are high. In order to achieve low standby current all inputs must be within 0.2 volts of either VCC or VSS.
2. The Chip is Disabled when $\overline{CE1}$ is high or CE2 is low. The Chip is Enabled when $\overline{CE1}$ is low and CE2 is high.

TABLE 6: Timing Test Conditions

Item	
Input Pulse Level	0.1V_{CC} to 0.9 V_{CC}
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	0.5 V_{CC}
Operating Temperature	-40 to +85^{o}C

TABLE 7: Timing

Item	Symbol	V_{CCQ} = 2.3 - 3.6 V		V_{CCQ} = 2.7 - 3.6 V		Units
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	85		70		ns
Address Access Time (Random Access)	t_{AA}		85		70	ns
Address Access Time (Word Mode)	t_{AAW}		85		70	ns
Chip Enable to Valid Output	t_{CO}		85		70	ns
Output Enable to Valid Output	t_{OE}		30		25	ns
Byte Select to Valid Output	t_{LB}, t_{UB}		85		70	ns
Chip Enable to Low-Z output	t_{LZ}	10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
Byte Select to Low-Z Output	t_{LBZ}, t_{UBZ}	10		10		ns
Chip Disable to High-Z Output	t_{HZ}	0	20	0	20	ns
Output Disable to High-Z Output	t_{OHZ}	0	20	0	20	ns
Byte Select Disable to High-Z Output	t_{LBHZ}, t_{UBHZ}	0	20	0	20	ns
Output Hold from Address Change	t_{OH}	10		10		ns
Write Cycle Time	t_{WC}	85		70		ns
Chip Enable to End of Write	t_{CW}	50		50		ns
Address Valid to End of Write	t_{AW}	40		40		ns
Byte Select to End of Write	t_{LBW}, t_{UBW}	50		50		ns
Write Pulse Width	t_{WP}	40		40		ns
Address Setup Time	t_{AS}	0		0		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to High-Z Output	t_{WHZ}		20		20	ns
Data to Write Time Overlap	t_{DW}	40		40		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Low-Z Output	t_{OW}	5		5		ns

FIGURE 4: Timing of Read Cycle (1) ($\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$)

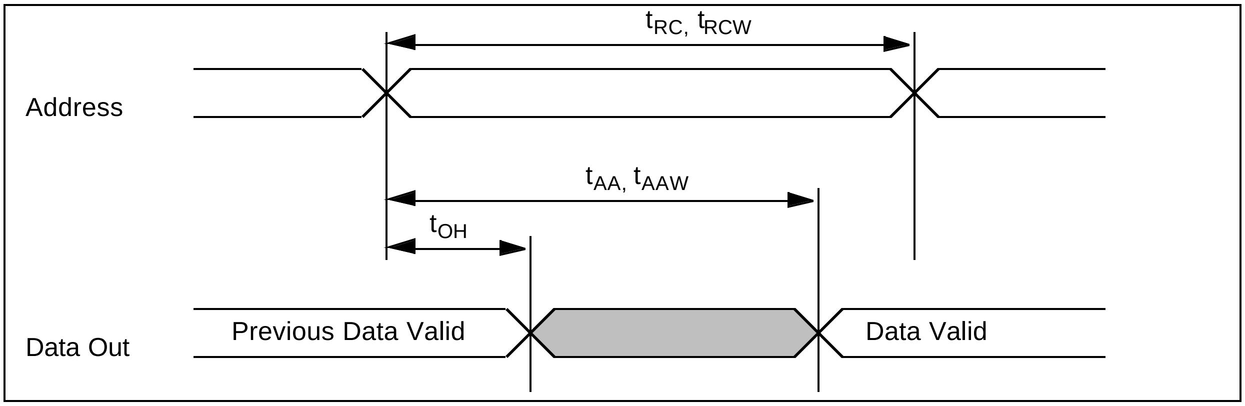


FIGURE 5: Timing Waveform of Read Cycle (2) ($\overline{WE} = V_{IH}$)

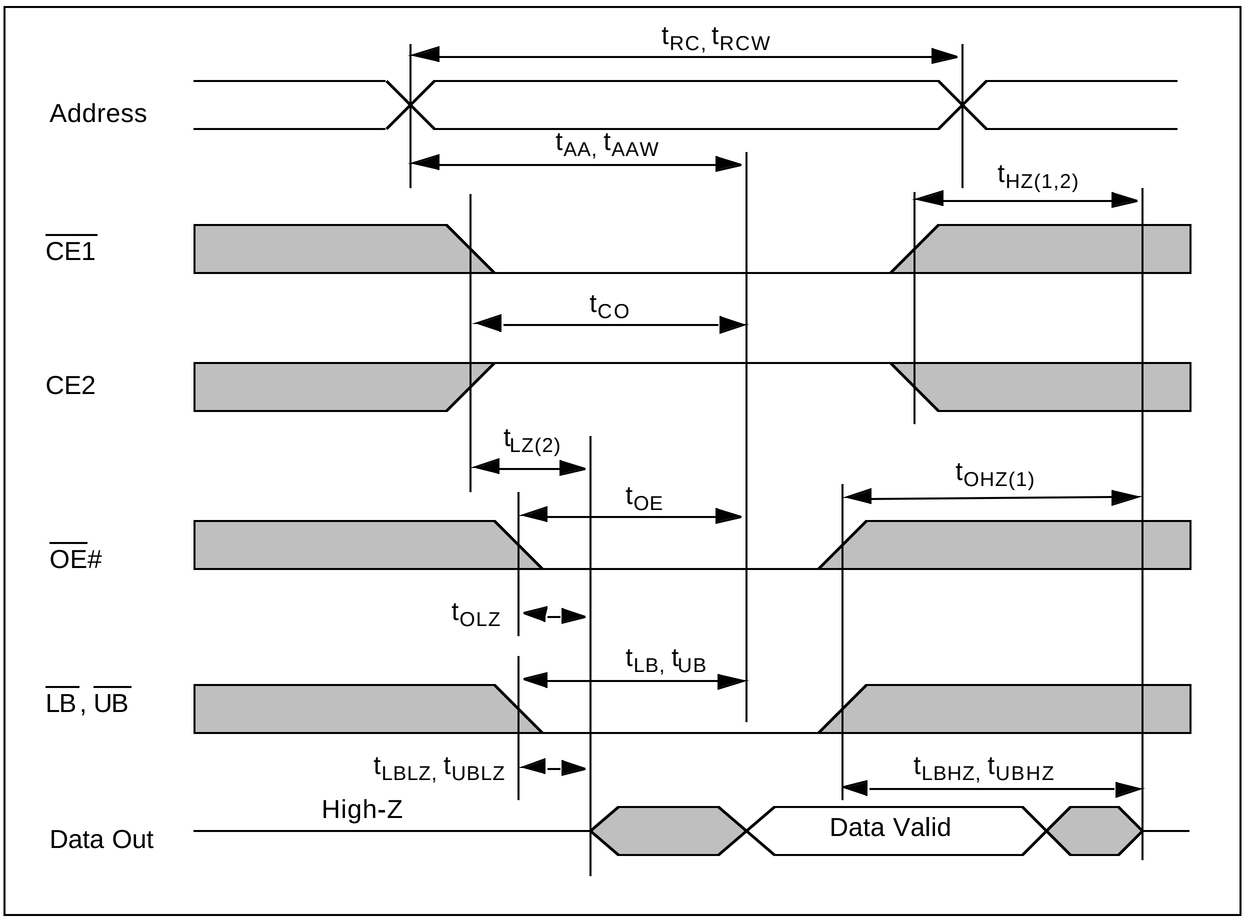


FIGURE 6: Timing Waveform of Page Mode Read Cycle ($\overline{WE}$ = V_{IH})

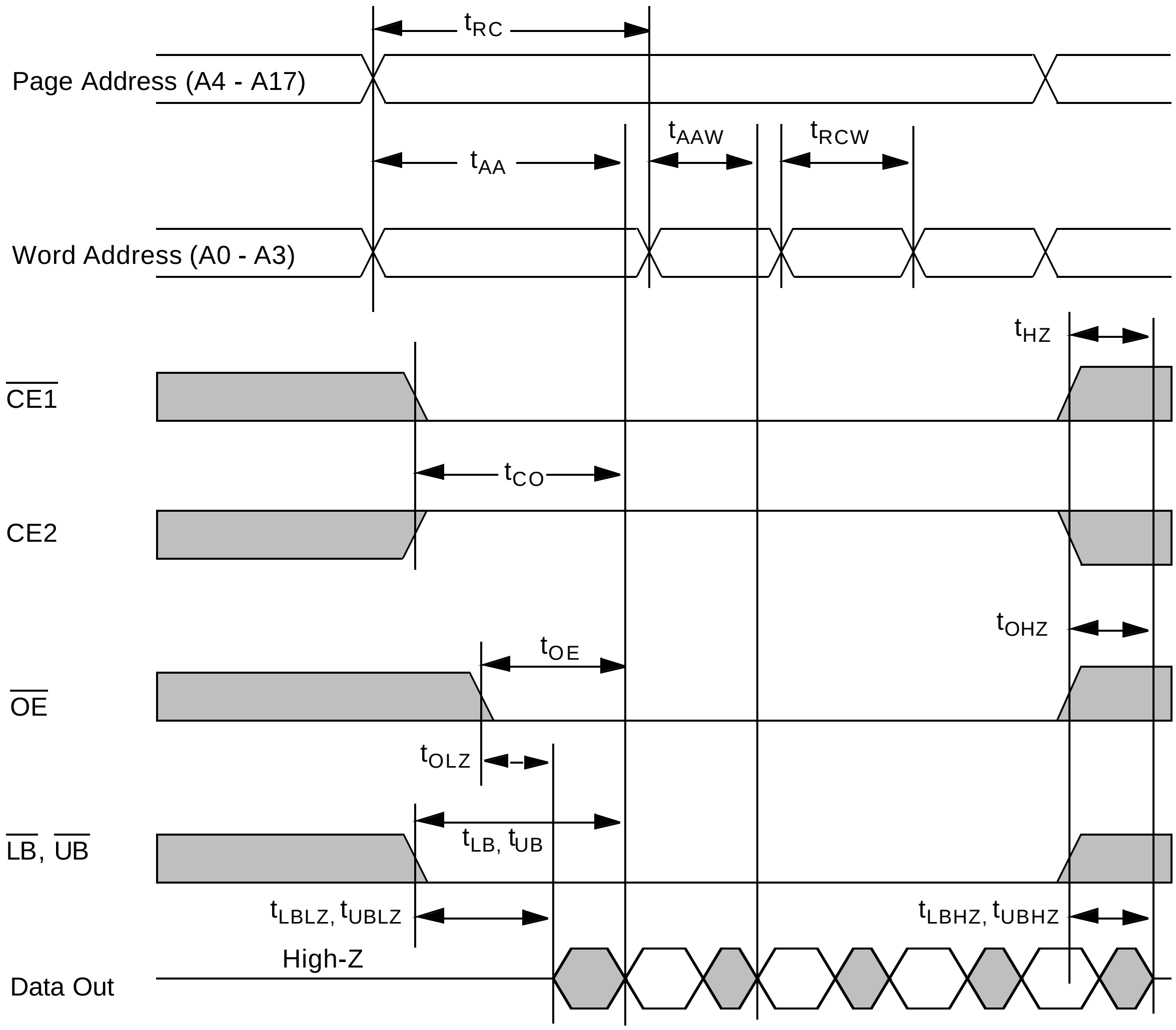


FIGURE 7: Timing Waveform of Write Cycle (1) ($\overline{WE}$ control)

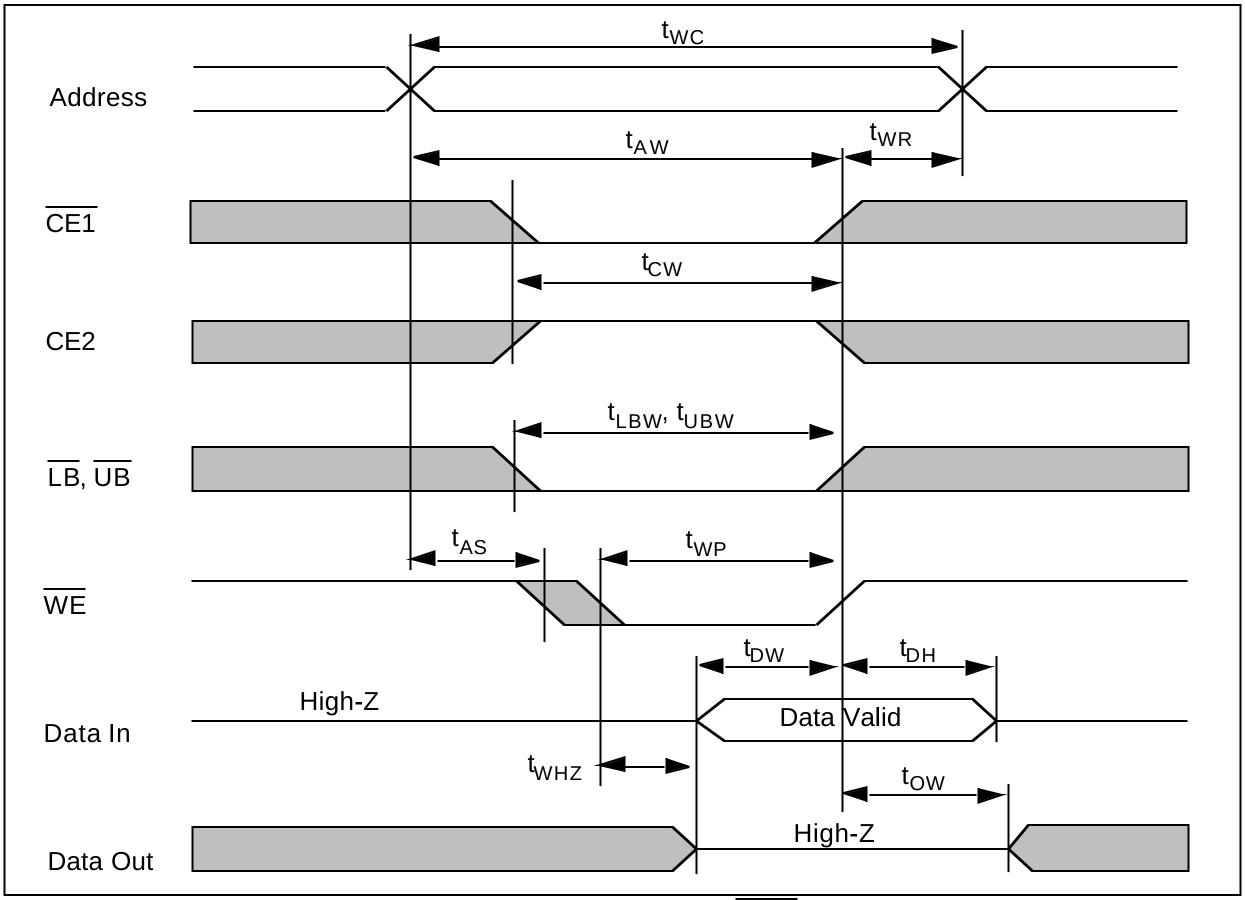


FIGURE 8: Timing Waveform of Write Cycle (2) ($\overline{CE1}$ Control)

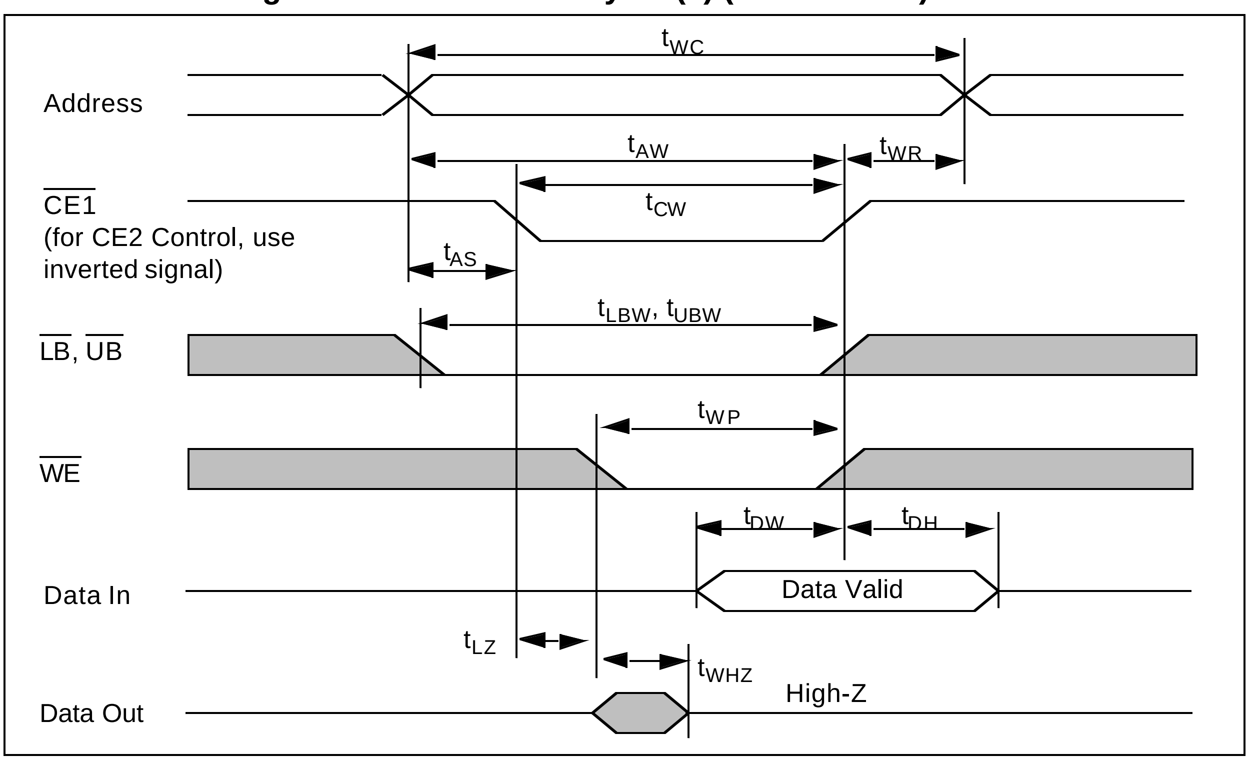
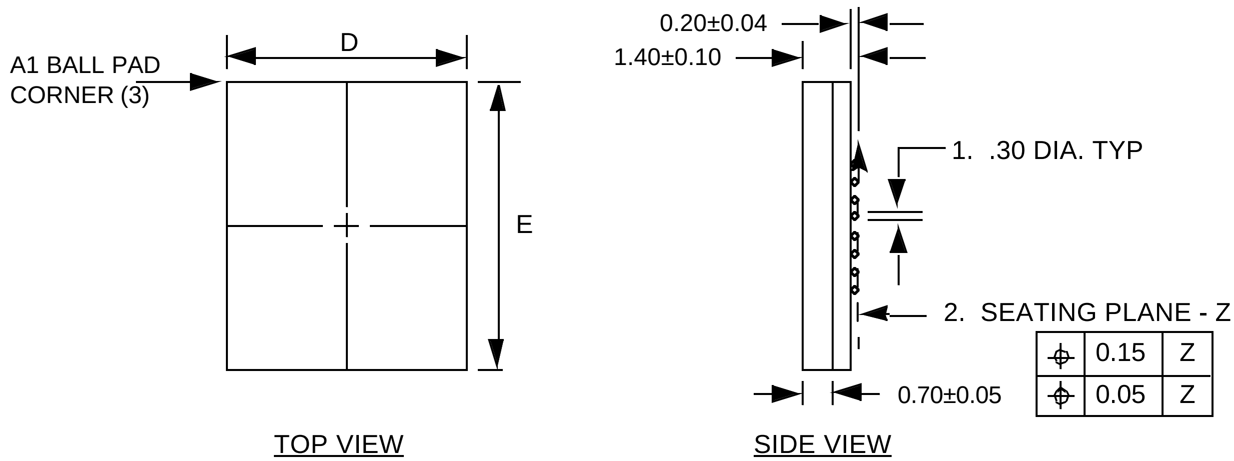
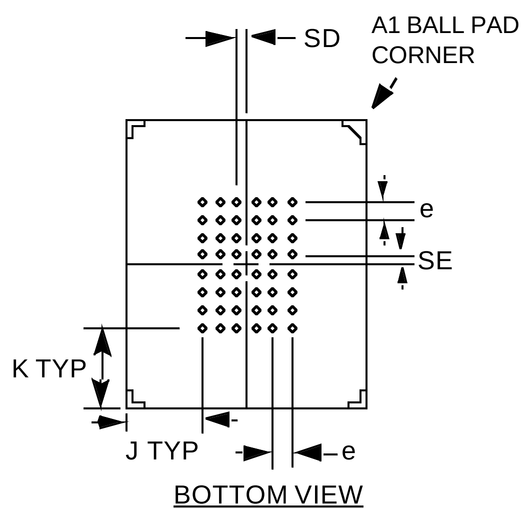


FIGURE 9: BALL GRID ARRAY PACKAGING





1. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER. PARALLEL TO PRIMARY Z.

2. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

3. A1 BALL PAD CORNER I.D. TO BE MARKED BY INK.

TABLE 8: Dimensions (mm)

D	E	e = 0.75				BALL MATRIX TYPE
		SD	SE	J	K	
8.0	10.0	0.375	0.375	2.125	2.375	FULL

TABLE 9: Revision History

Revision	Date	Change Description
A	Jan. 1, 2001	Initial Advance Release
B	Mar 2001	Deleted TSOP references